



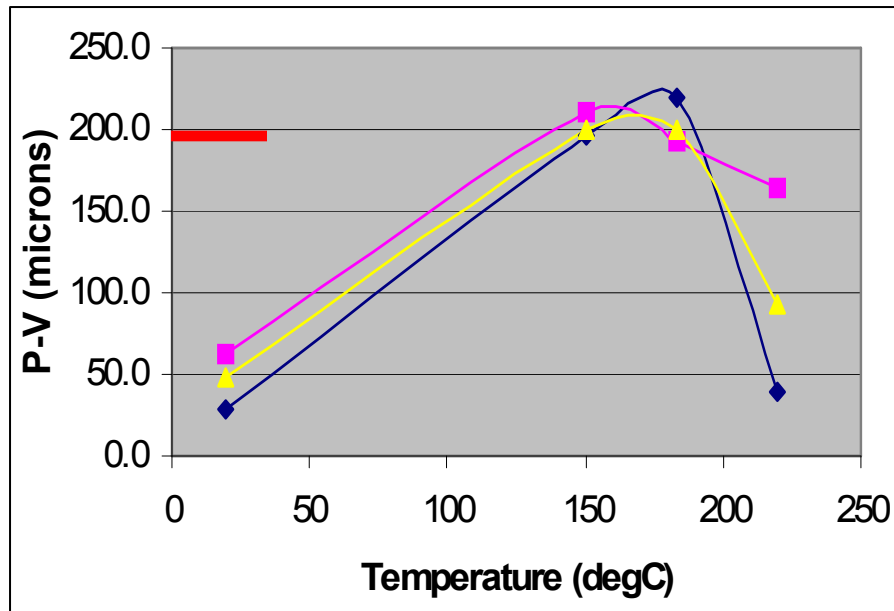
Implementing High Temperature Coplanarity Requirements for Components and PWBs



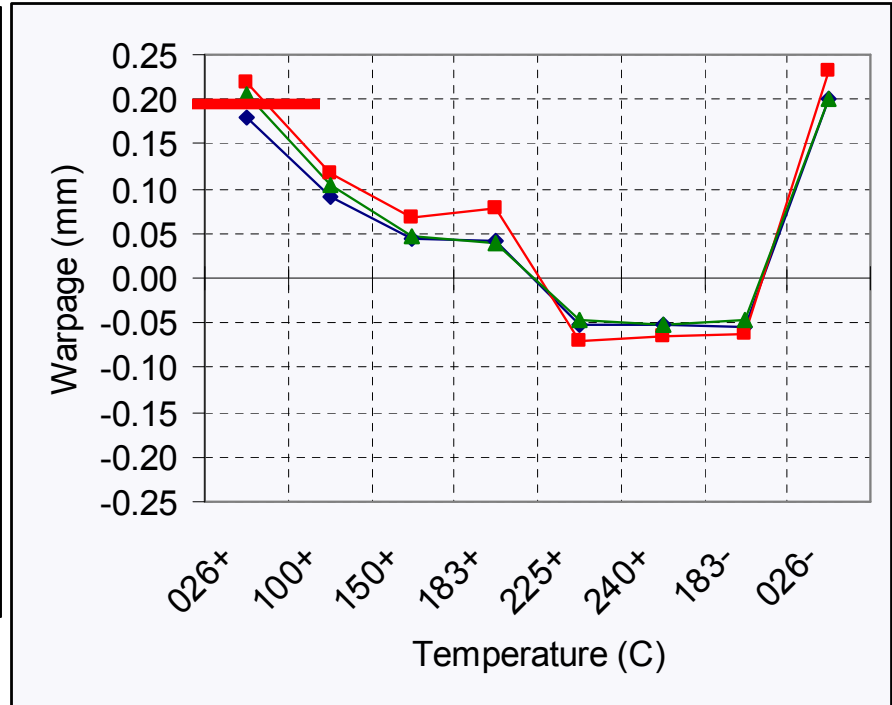
Current Status:

- Coplanarity and flatness requirements have been included in JEP95 and other industry documents to ensure that components surface mount properly
- Previously coplanarity and flatness measurements were limited to room temperature
- Correlation between room temperature requirements and SMT quality are limited

Shortcoming: Limited to Room Temperature

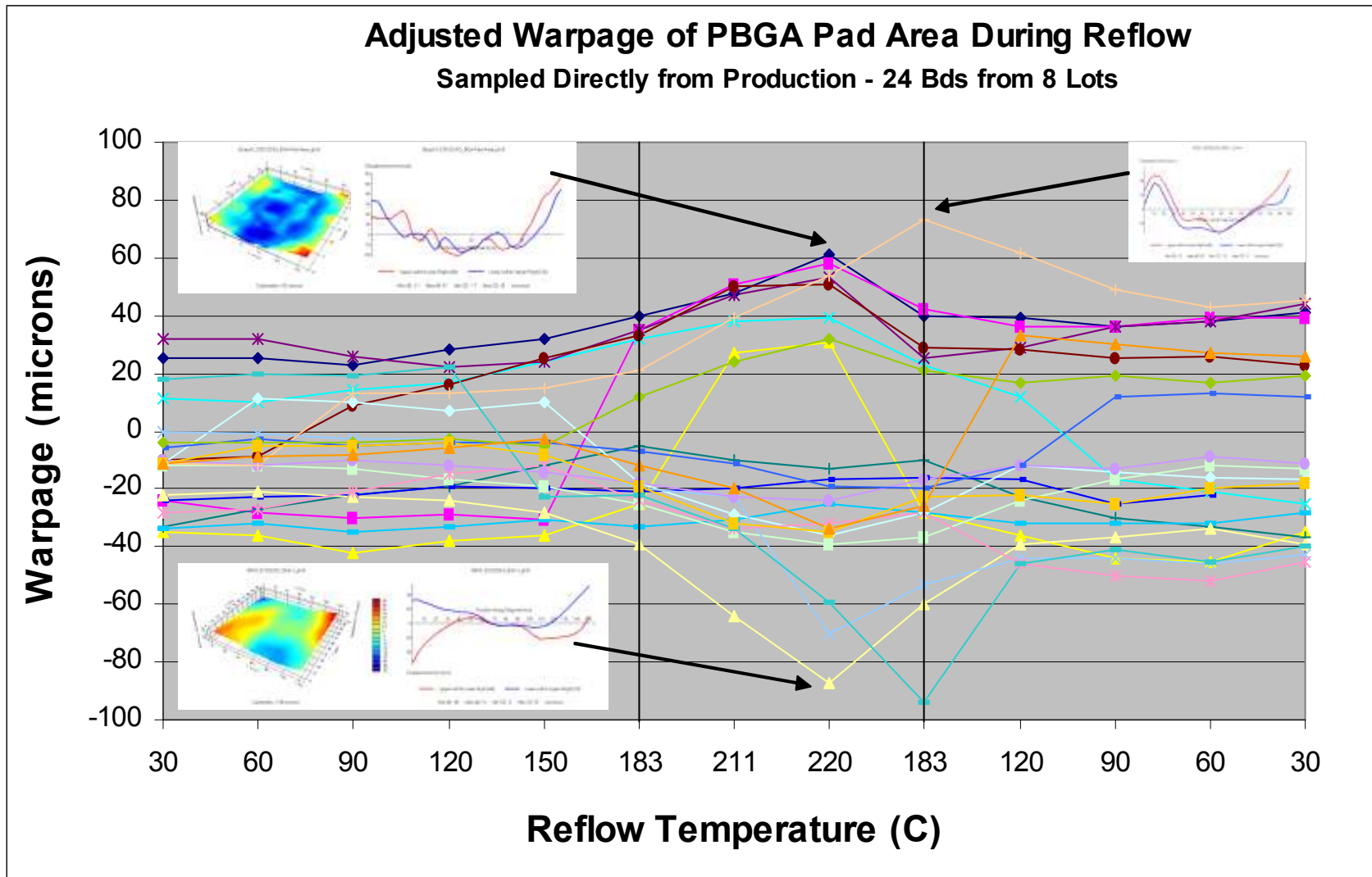


- PBGA package, meets current JEDEC requirements
- Does not surface mount, very high yield loss



- Large FCBGA development package, does not meet current JEDEC requirement
- No SMT yield loss in LVM production, no reliability impact

Boards Warp Too, In Complex Ways



Acknowledgment: Mike Varnau Proposed



Problem Statement:

- Since current specifications do not reference SMT temperature, they:
 - Do not assure high quality SMT
 - Increase costs to meet room temperature coplanarity for stiffeners, heat spreaders etc.
 - Are stifling innovation in high density packaging
- Current specs also do not explicitly reconcile board and component requirements
- New methods are needed that:
 - Reference the SMT temperature
 - Give a means to monitor at room temperature for HVM that recognizes individual package behavior
 - Explicitly divide the total “joint formation budget” between the component and board



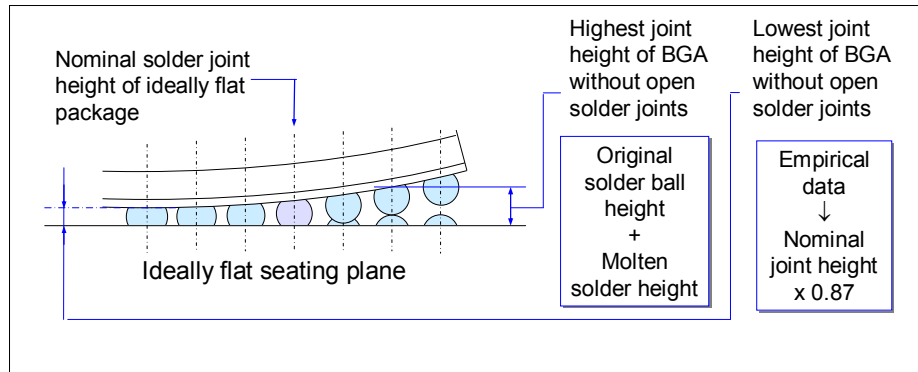
JEITA ED7306 Method:

“Measurements methods of package warpage at elevated temperature and the maximum permissible warpage”

- Spec defines methods for measuring the warpage of packages at high temperature, similar to JEDEC B112
 - Allows for ball removal, moisture, and bake
 - Defines a conventions for sign and warpage definition
 - Allows for shadow moire or laser reflection
 - Requires data at room, melt, peak, solidus, and room on return
 - Temperature gradient through package should be less than 10° C
- Comparison to B112 given in appendix

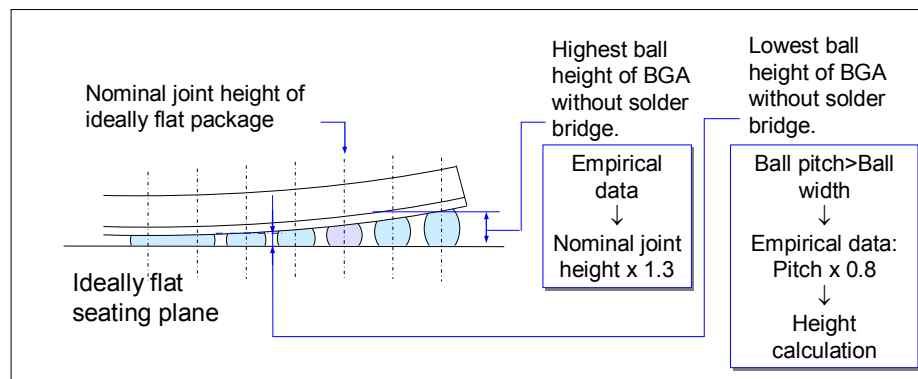
JEITA Warpage Derivation

The maximum relative displacement is defined as the difference between the highest and the lowest solder joint heights of BGA package mounted on the ideally flat seating plane, where none of solder joints are open.



Explanatory Fig. 1— Calculation of the maximum relative displacement immune from open solder joints.

The maximum relative displacement is defined as the difference between the highest and the lowest joint heights of BGA package mounted on the ideally flat seating plane, where none of solder joints bridge.



NOTE Constants of the calculations are obtained from the experiment and used for simplicity.

Explanatory Fig. 2 — Calculation of the maximum relative displacement immune from solder ball bridges

- Arguments are primarily geometrically based, supplemented by experimental data
- Both opens and bridging are considered
- Allowable warpage divided 80-20 between component and board

osed

Ack: JEITA

JEITA Maximum Warpage

Explanatory Table 1— Maximum permissible package warpage for BGA and FBGA Unit: mm

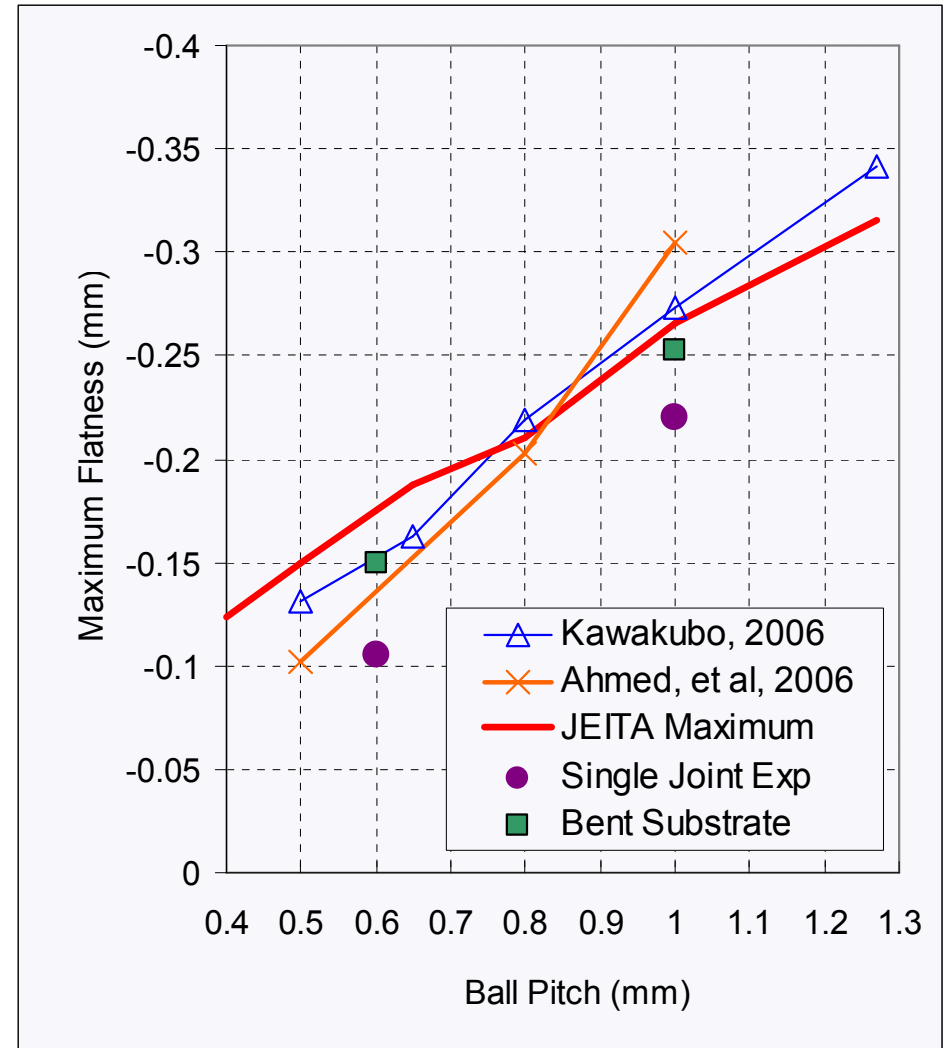
	Solder ball pitch	0.4	0.5	0.65	0.8		1.0	1.27	
1	Condition of solder ball height ^a	0.20	0.25	0.33	0.35	0.40	0.50	0.60	
2	Condition of solder paste thickness after reflow ^b	0.08	0.10	0.11	0.13		0.14	0.15	
3	Nominal solder joint height of the ideally flat package	0.18	0.23	0.29	0.31	0.36	0.43	0.5	
4	Highest solder joint height of BGA without open solder joint ^c	0.28	0.35	0.44	0.48	0.53	0.64	0.75	L1+L2
5	Lowest solder joint height of BGA without open solder joint ^d	0.16	0.20	0.25	0.27	0.31	0.37	0.44	0.87*L3
6	Highest solder joint height of BGA without solder bridge ^e	0.24	0.29	0.38	0.40	0.46	0.55	0.66	1.3*L3
7	Lowest solder joint height of BGA without solder bridge ^f	0.12	0.15	0.20	0.19	0.25	0.28	0.34	NOTE
8	Max relative displacement of BGA without open solder joint ^g	0.12	0.15	0.19	0.21	0.22	0.27	0.31	L4-L5
9	Max relative displacement of BGA without solder bridge ^h	0.12	0.14	0.18	0.21	0.21	0.28	0.32	L6-L7
	Max permissible package warpage (Absolute value) ⁱ	0.10	0.11	0.14	0.17	0.17	0.22	0.25	0.8 Max[L8,L9]
	Coplanarity at room temperature (For reference)	0.08	0.08	0.10	0.10	0.10	0.20	0.20	Tighter than JEDEC spec.

NOTE: Paste thickness + ball height whose ball diameter expands to 80% of ball pitch
Proposed

Ack: JEITA ⁸

Confirmation of the Formation Budget

- JC11 TG has completed experiments to confirm literature data
 - Forming single joint with a controlled separation
 - Bending a FCBGA substrate to range of coplanarity, do not change with temperature
- The data fits a consistent trend
- Propose using JEITA Maximum as a starting point





Numbers Check: The Current State

850 pin, 1mm pitch = 30mm Package

Contributions:

- Min Paste Thickness 125um
- Paste Expansion (SJ) 60um
- Ball Drop (Single Joint) 20um
- Ball Collapse (JEITA) 70um

Budget

Sum of Contributions: 275 um

JEITA Maximum: 280 um

Consumption:

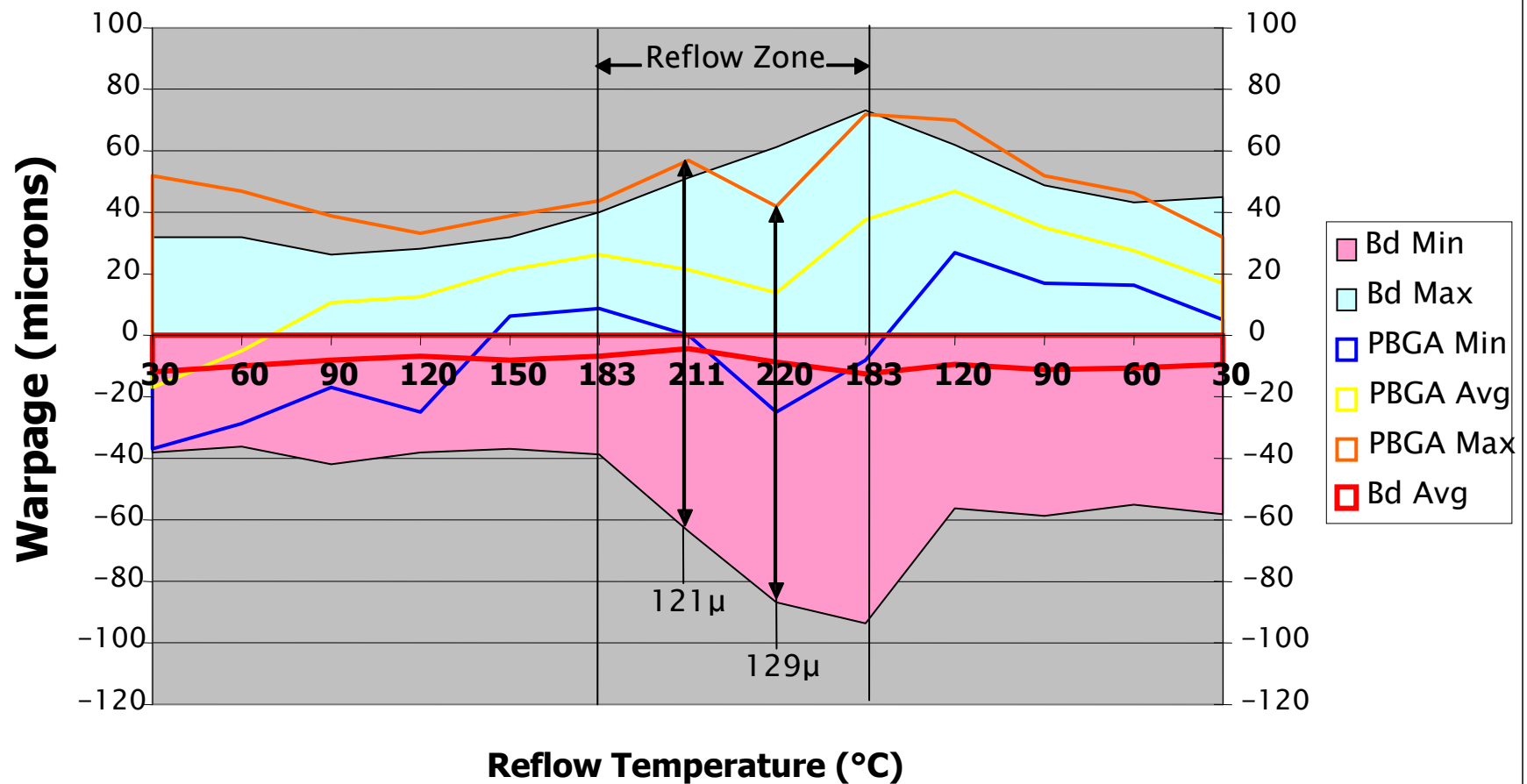
- Maximum Board Warpage
(7.5mil/in diagonal) 317um
- Maximum Package Coplanarity @
SMT
(JEITA) 220um

Total Consumption: 537um

- Its clear that numbers don't add up properly, yet packages surface mount anyway
- Most components and boards do not approach the maximum allowable
- However the case above is possible according to the specs, but not probable

Overlay of PBGA and Board Warpage

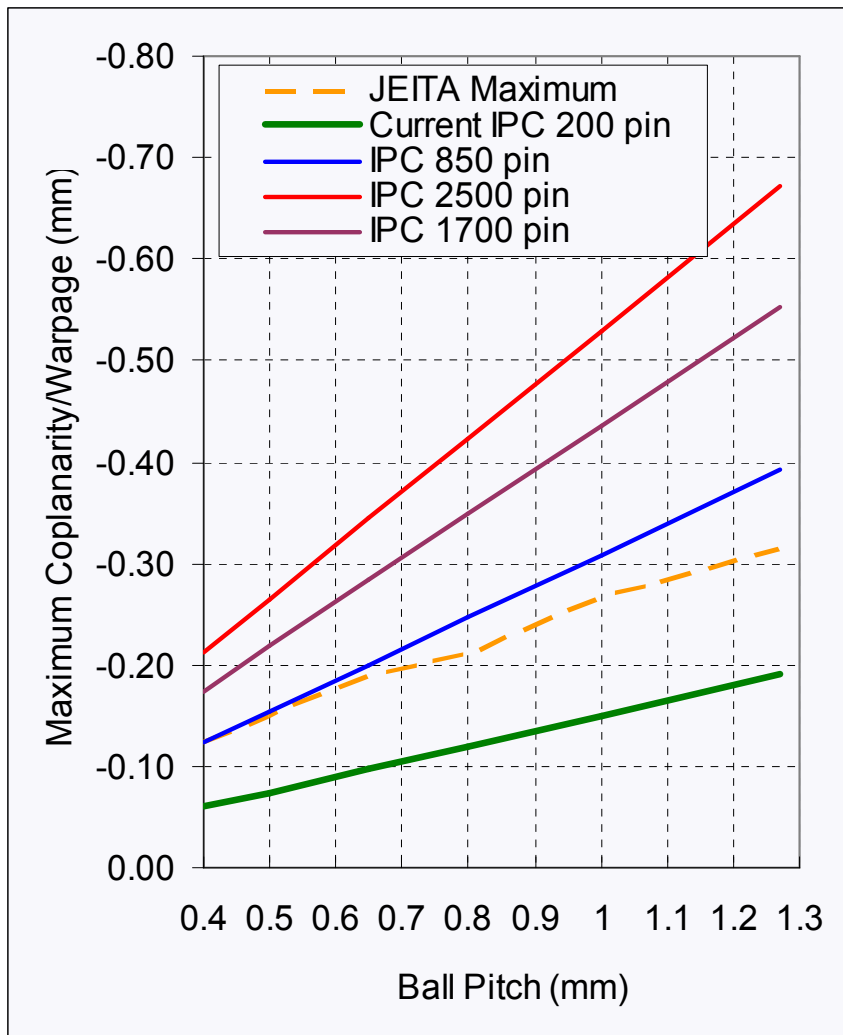
Warpage Analysis of 288 PBGA Std Material Set (Production Samples)
6 Layer Circuit Board (Production Samples)



Ack: Mike Varnau

A more realistic example
Proposed

Current IPC Standards



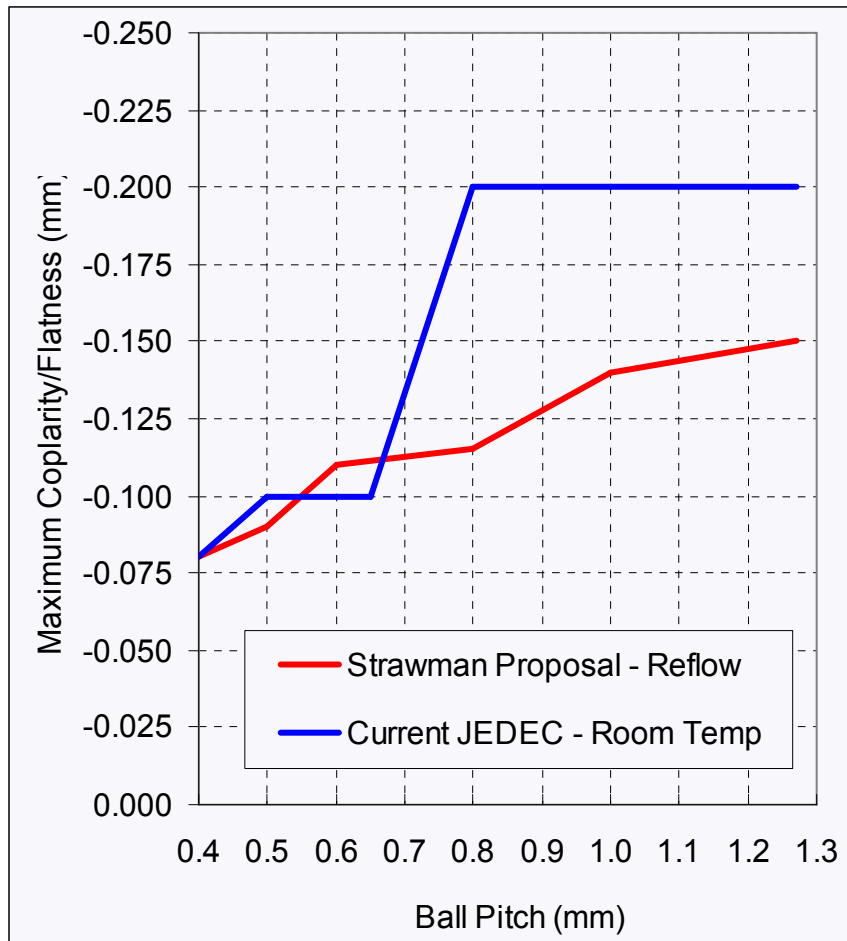
- Starting with the current assumes 0.75% warpage on the land area (diagonal)
- For pin counts (large packages) the board warpage consumes the entire budget
- Current board specifications do not scale with package size or pin count



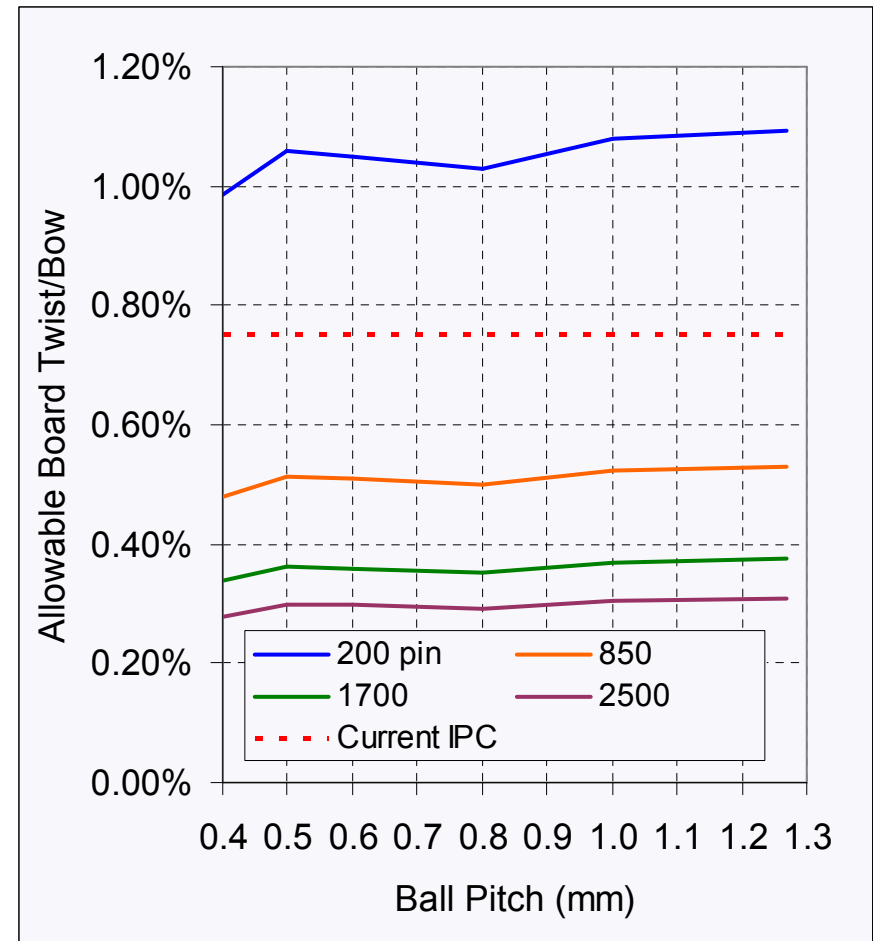
Where do we stand?

- Component methodologies nearly complete and a straw-man proposal is being circulated
- Board technologies not as mature, considerable development required
- Propose to move forward with JEDEC standard and use iNEMI group to initiate work to advance the board side
- Once board work is complete two standards coupled be reconciled

Straw-man Proposal



Package Total Warpage



Resulting Board Requirement



Goals

- Establish metrologies needed to measure board flatness in land area at both room and elevated temperature
- Develop strategy for setting requirements for differing board technologies and categories
- Set acceptance criteria for board flatness and conditions for sampling and measurement requirements



Next Steps

- Survey of member companies of internal and customer requirements and current capability
- Literature survey of applicable methods & survey commercially available systems
- Round-robin testing of systems to understand limitations
- Draft best practices document for high temperature methods for board design validation
- Develop best practices for factory monitoring if required