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iNEMI Statement of Work (SOW)
Board & Systems Manufacturing Test TIG
iNEMI Built-In Self-Test (BIST) Project
Phase 1 – Research Project Information (Survey)

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Basic Project Information

Scope of Work

This project's focus is on "Chip" Built-In Self-Test (BIST) study and promotion for board and system-level applications. The project is divided into 3 phases. Phase 1 is being presented as a "standalone project" and will be used as the baseline in defining the second and third phases.

Phase 1

The first phase is a survey of the industry on current BIST capabilities and future requirements. The major goals of this project phase are to get feedback from the industry on board level BIST that will assist in fine tuning the scope of Phase 2 of the project.

Phase 2

The current vision is that the second phase will be comprised of the following 3 parts:

1. Identification of Chip BIST technologies, which can be migrated to run at board/system-level test. Some examples of BIST techniques are list below:

BIST Technique	Fault Coverage	Study Directions
Internal MBIST	IC internal defects: stuck at fault, dynamic fault	Algorithms
External MBIST	External memory Defect: DDR, RLDRAM, FCRAM, TCAM, SSRAM stuck at fault, dynamic fault Interconnect defect: process defect PCOLA/SOQ and SSN	Algorithms, Diagnosis

BIST Technique	Fault Coverage	Study Directions
High speed IO BIST	Interconnect defect - SI /noise defect	Protocols, algorithms, interconnect between different vendors ICs, interconnect over backplanes
Logic BIST	IC internal defect	Applications, resolve NTFs issues
Frame BIST	IC internal defect, process defect, and system-level malfunctions	Instruments - - Protocols, Algorithms, diagnosis

2. Investigation of BIST tests that enable PCBA testing without or minimal use of fixture/ICT (In Circuit Test) system (currently the typical manufacturing test approach) to lower cost of test and enhance test coverage for high speed interconnects.
3. Promotion of the development of existing related standards for BIST design.

The deliverable will be a whitepaper on BIST ecosystem model (Revision 1), that will include guidelines for implementing BIST at the board level.

Phase 3

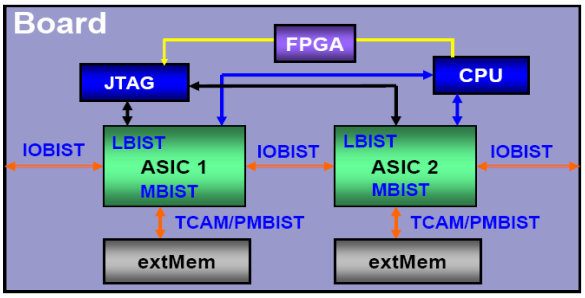
The third phase is the development of guidelines and recommendations for a new standard for PCBAs to run BIST tests, and the transfer of the implementation to the appropriate standards body (Phase 3 will take place if the outcome of Phase 2 recommends it).

The deliverable will be an updated whitepaper on BIST ecosystem model and guidelines and recommendations for a new standard, and transfer the implementation to the appropriate standards body.

Purpose of Project

Presently, there are no Standard Chip level interfaces or algorithms, for Built-In Self-Test (BIST), which limits the introduction of BIST at board level test. Most "chip" level BIST systems are designed to aid IC manufacturing; these algorithms are not suitable to the PCB board, or are not available to run at the board level.

The goal of this project effort is to launch an iNEMI project to develop and promote the adoption of chip BIST at the board/system level, encourage IC vendors to provide standard chip BIST interfaces and algorithms and in addition, encourage ATE/Instrument providers to develop products based existing related standards for BIST design, for example, an IEEE 1500/P1687a globalized Test Cost Model useful throughout the industry.



What the Project Is / Is Not

This Project IS:	This Project IS NOT:
Phase 1	
Survey the current adoption of component BIST in PCBA board testing.	Survey the detailed implementation of the chip BIST
Investigate needs/requirements of using BIST in Board testing.	
Highlight the top concerns and issues in the industry	
Collect technical expectations for the future	
Review any related research or development done within the industry	
Summarize, briefly, directly related academic research, if any	
Develop Phase 2 plans	

This Project IS:	This Project IS NOT:
Phase 2	
Identification of existing component BIST that can be run at the PCBA level.	TBD
Investigation of BIST to enable PCBA structural testing.	
Promotion of existing BIST standards	
Develop Phase 3 Plans	

This Project IS:	This Project IS NOT:
Phase 3	
Develop guidelines and recommendations for new standard for PCBAs to run BIST tests	Not a standards development
Transfer of the guideline and recommendations to the appropriate standards body for implementation	

Previous Related Work

Intent of the survey is to identify previously related work to ensure we are not duplicating what has been done or what is being worked on.

Some previous industry related work:

"Design for Board and System Level Structural Test and Diagnosis," Toai Vo et al, Cisco, ITC 2006

- Review any related research or development done within the industry
- Summarize, briefly, directly related academic research, if any

Prospective Participants

1. Current companies participating on the Project Formation Team are:
   - Hewlett Packard, Intel, Agilent, Huawei, Alcatel-Lucent, Cisco

2. Participant companies should also include:
   - Chip design companies (memory, microprocessor, ASIC, datacom)
     TI, Micron, Marvell, Broadcom, IBM, LSI, Maxim, Micrel, (ASIC vendors/manufacturers)
   - Board and system design companies (PC, networking, test)
     Dell, Delphi, Lenovo, Quanta. Sun Microsystems, etc.
   - EMS, CMs, ATE Suppliers, ICT Fixture suppliers,
     Celestica, Flextronics Foxconn, Plexus, Sanmina-SCI, Teradyne, Stats ChipPac, Verigy, ECT
   - Boundary scan suppliers
     Asset, JTAG, Intellitech
3. Participating companies need to be iNEMI members.

Project Plan

Schedule with Milestones:

		Months														
Task		**Nov**				**Dec**				**Jan**				**Feb**		
	Phase 1 Survey															
1.0	**Plan the survey**															
1.1	Define questionnaire (questions)															
1.2	Define survey hosting and data analysis method															
1.3	Prepare survey recipient list															
2.0	**Prepare logistics of survey (post/host survey, notify recipients)**															
3.0	**Conduct survey / Distribute Questionnaire**															
4.0	**Collect and analyze data**															
5.0	**Review/Share survey data with project members**															
6.0	**Identify the key areas for further discussion**															
6.1	Identify data to support scope for items in Phase 2															
7.0	**Prepare report of the survey result**															
7.1	Internal report for iNEMI Project team															
7.2	Summary report for iNEMI membership															
8.0	**Phase 2 preparation, project plan, SOW**															

Detailed *Information*

Phase 1 BIST Survey - Tasks

1.0 Plan the survey

1.1 Define the questionnaire (questions)

What are the questions that will be asked? They must be such that they enable the items in phase 2 to be clearly defined and scoped. Decide on the format of the questions to enable easy and clean data analysis.

1.2 Define survey hosting and data analysis method

Where will the survey be hosted from? For example, an iNEMI server, surveymonkey.com.

What tools will be needed to analyze the data? Task 1a defines what data should be collected.

1.3 Prepare survey recipient list

A list of recipients at relevant companies who design, use and run BIST needs to be compiled.

- Resources
  - Phase owner to lead gathering of questions for questionnaire
  - Prospective item owners to lead content of questionnaire per table below:

ITEM OWNER	Identify current state of chip BIST	Run or modify BIST at the board/system level	Investigate BIST as an alternative to ICT (low cost testing)	Promote development of related standards	Develop a new standard for BIST at the board level
Bill Eklow					
Yang Yang					
Jiang Zihua					
Li Hui					
Jun Balangue					
Zoe Conroy					

  - All team members need to contribute to the survey recipient list
  - One or more team member needs to propose how the survey will be hosted and the data analysis method

- Materials and processes
  - Software/server to Host survey (iNEMI server, survey monkey etc.)
  - Software to perform data analysis

2.0 Prepare logistics of survey (post/host survey, notify recipients)

- Resources
  - Team members to own posting the survey and send out to the recipient list

3.0 Conduct survey

- Resources
  - Team members (from Task 2) to send reminders to recipients, and close out the survey

4.0 Collect and analyze data

- Resources
  - Team members to collect all survey replies and compile data
  - Team produces a report based on the data

5.0 Share survey data with project members

- Resources
  - Team member to share data with team

6.0 Identify the key areas for further discussion. Identify data to support scopes for phase 2 tasks.

6.1 Identify data to support scope for items in Phase 2

- Resources
  - Project Team to clarify scope for phase 2, based on the survey data

7.0 Prepare report of the survey result

7.1 Internal report for iNEMI Project team

7.2 Summary report for iNEMI membership

- Resources
  - Team members to share summary of survey results; give Webinar / report to general iNEMI membership and present at a conference (e.g., International Test Conference)

8.0 Task 8. Phase 2 preparation, project plan and SOW

- Resources
  - Team member to develop Phase 2 plan and recommendation for implementation

Phase 2 Tasks (possibilities):

1.0 Run existing component BISTs, or modify BIST designs to run at the PCBA level.

1.1 Ask component suppliers to give details on their existing BIST, so their customers can run it at the board level (internal memory BIST, IO BIST/PRBS, etc.). (Survey question)

1.2 Ask suppliers to add the BIST instructions/details to their datasheets. (Survey question)

1.3 Understand the existing PCBA test coverage obtained from the existing BIST structures and whether any new types of BIST tests would add extra useful coverage.

1.4 Get suppliers to design BISTs on interfaces (not to any standard) (to add coverage per task 3), so that they can be run at the PCBA (EMBISTs, IOBISTs, PRBS loopback tests, etc.). (Survey question)

1.4.1 Resolve access issue on PCBA manufacturing test.

1.4.2 Get suppliers to make sure their high speed interface (with TX/Rx ports) can facilitate looping back an adjacent components IOBIST test.

1.5 Review the test access mechanism of JTAG, CPU and others, to determine a recommended mechanism in various application scenarios (development debug, manufacturing test, in field maintenance, etc.).

1.6 Evaluate the result of these BIST used in actual board/system-level test progress for, fault coverage, efficiency improving, and cost reduction.

2.0 Investigate/ask for BIST tests that enable PCBA testing without or minimal use of fixture/ICT (In Circuit Test).

2.1 Study and define the relation of BIST to other substitutions of ICT (such as Boundary Scan). (Can we get supports from other iNEMI projects related to BS and ICT?)

2.2 Survey the industry. Include ICT equipment suppliers (Agilent, Teradyne), OEMs/EMSs, ICT fixture suppliers. Questions include their current application, requirements, expectations of BIST as a substitutive technique to ICT.

2.3 Pilot some member companies to do some experiments in actual manufacturing process. To get valuable data about the test cost improvement (fixture cost, test time, test coverage, etc.).

2.4 Output a white paper, including all suggestions to introduce BIST into ICT.

2.4.1 List all types of BIST that are applicable to be introduced into ICT.

2.4.2 Summarize our experiment data about BIST in ICT.

2.4.3 Provide suggestions to new standards in the future from ICT test perspective.

2.4.4 Provide suggestions to ASIC vendors, test equipments suppliers and board manufacturers.

3.0 Promote the development of related standards for BIST design.

3.1 Scope of study will include the BISTs only used in PCBA test, and the BISTs formerly designed for ASIC package and test purpose, but can be reused in board level test. (overlap with (1) and (2) above).

3.2 Define the BISTs relationship to the other standards (i.e. 1149.x / P1687, etc.).

3.3 Define the methods to evaluate the chip BIST's design and application ability.

3.4 Provide BIST designers algorithms and test requirements specific for PCBA.

3.5 Define how to make the new standard backward compatible as much as possible to cover the existing BISTs. This compatibility will promote the acceptance of the new standard.

3.6 Investigate IC vendors, ATE suppliers, and manufacturers to collect requirements, suggestions, and current application data on chip BIST, determine barriers to chip BIST's adoption.

3.7 Encourage IC vendor to provide standard chip BIST interfaces and algorithms.

3.8 Encourage ATE/Instrument suppliers (board level manufacturing) adopt and develop products based on chip BIST.

Phase 3 New BIST Standards - Tasks

1.0 Develop guidelines for a new standard PCBAs to run BIST tests.

2.0 Implement the new standard thru the appropriate standards body for PCBAs to run BIST tests.

For example, BIST should be treated as instruments rather than simple protocols. Then, the new standard may be implemented through an layered (or stacked) architecture, including logic and physical layers, or software and hardware layers, etc. At the high level abstract layer, it may not be difficult to define a protocol or standard to cover fundamental BIST functionality and controls. Then, at the lower layer, the implementation could be done by whatever way, using existing or new BISTs. Actually, VISA is a good example.

Project Monitoring Plans

- Planned teleconference schedule: Weekly or Biweekly conference calls as needed on Monday afternoons at 5:00 p.m. (PDT/PST); 8:00 a.m./9:00 a.m. China/Taiwan.
- Meeting minutes provided through e-mail.
- Follow-up with individuals on an as needed basis.
- Workshops and face-to-face meetings as appropriate.
- Progress reports will be issued as tasks are completed.
- A mid-point progress update will be made to the iNEMI Technical Committee at the end of Task 3 – Conduct Survey / Distribute Questionnaire.
- Provide quarterly reports briefly indicating progress. This could be a short series of PowerPoint slides showing the work in progress.
- Review all project requirements with prospective participants before the project begins.

- A final report will be issued documenting the survey findings and recommendations at the end of Phase 1.
- Issue report on the planning for Phase 2 and make recommendation to continue or stop project at the end of Phase 1.

Outcome of the Project

Phase 1 success will be the collection and analysis of the Survey data and the development of Phase 2 project plan.

Completion of the phase 2 items will result in buy in from the industry on PCBA BIST testing, that it is a viable manufacturing solution and can help eliminate the need the extensive ICT (In Circuit Test). The project will promote the use of existing BIST standards to enable PCBA BIST.

The deliverable will be a whitepaper on BIST ecosystem model (Revision 1) including guidelines for implementing BIST at the board level. This will be sent to various International conference bodies for publication, e.g. ITC.

General and Administrative Guidelines

General and Administrative Guidelines for this project and all other iNEMI Projects are documented at http://thor.inemi.org/webdownload/join/gen_guidelines.pdf.