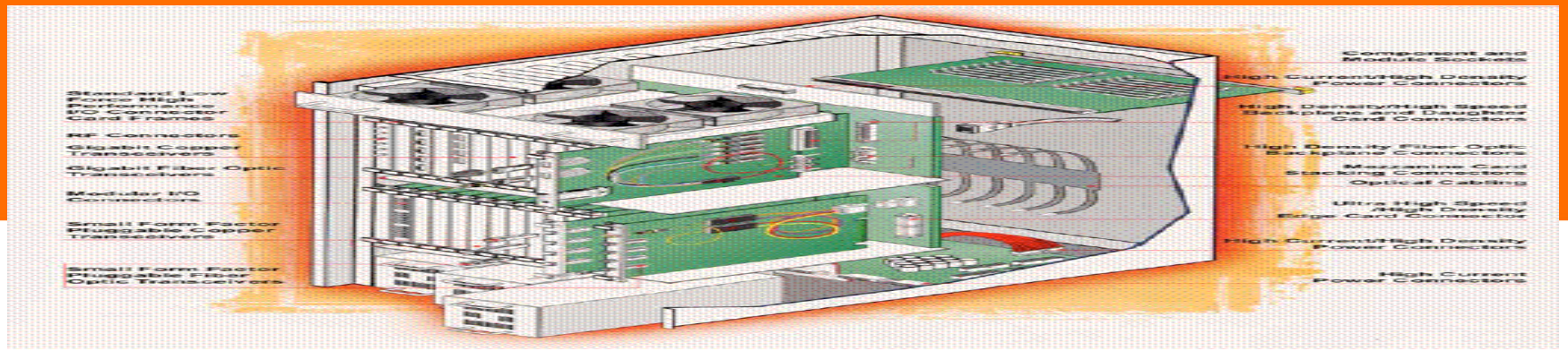

NEMI Cost Analysis: Optical Versus Copper Backplanes

Part I: Benchmarking Copper

NEMI project team
Adam Singer
APEX 2004

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Overview

- An apology – no optical comparison yet
  - *But, if you leave your card, we'll send you an update*
- NEMI team goal
- Background on copper and optical technology
- Cost modeling methodology background
- Copper backplane cost analysis
- "The Metric"
- Future work

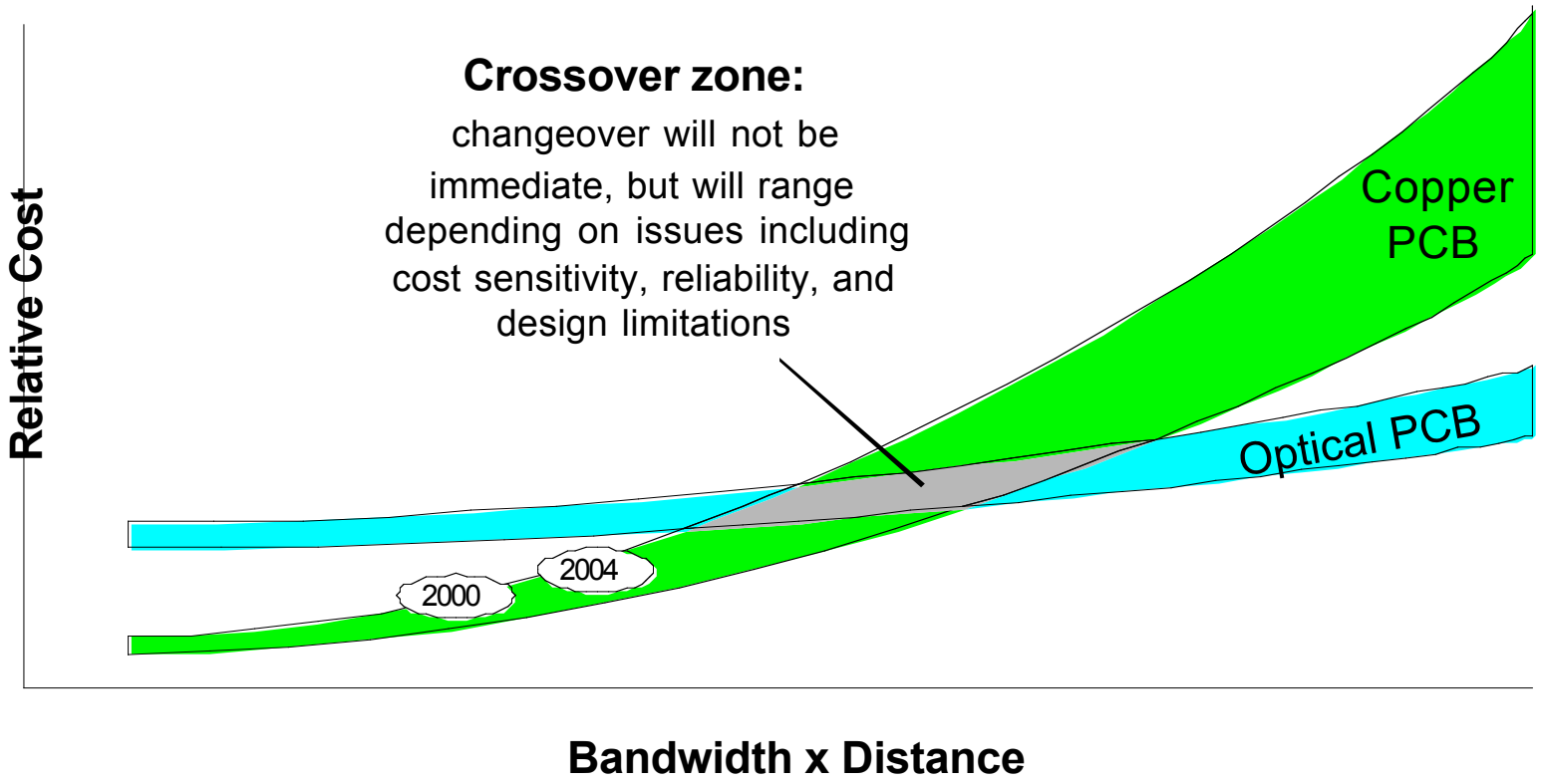
Optical PCBs – Needed Yet?

- Copper still finding ways to improve
- Market demand for next-gen telecom systems slowed dramatically in 2001-3
- Cost crossover point not yet understood

Reason for NEMI project

- *Develop cost models*
- *Compare Cu and optical costs*

NEMI's Goal



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Optoelectronics Concepts

Photons

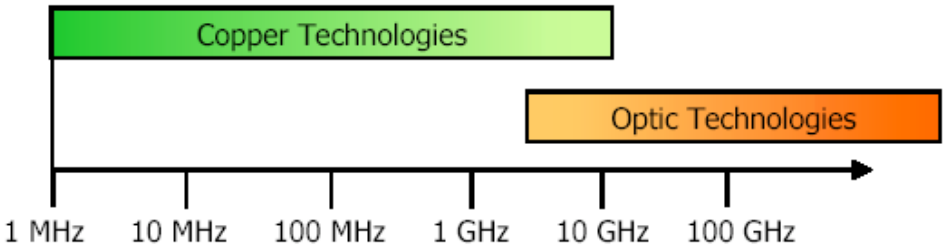
- **Zero Rest mass**
- **FxD > 10^{14} Hz x 100km**
- **Boson => Mult. Signals**
- **OE Conversion needed**

Best for long distance, high speed

Electrons

- **9.11 x 10^{-31}kg**
- **FxD > 10^{10} Hz x 0.001km**
- **Fermion: One Signal**
- **No OE Conversion**

Best for very short distance (<5 meters) at moderate to high speed



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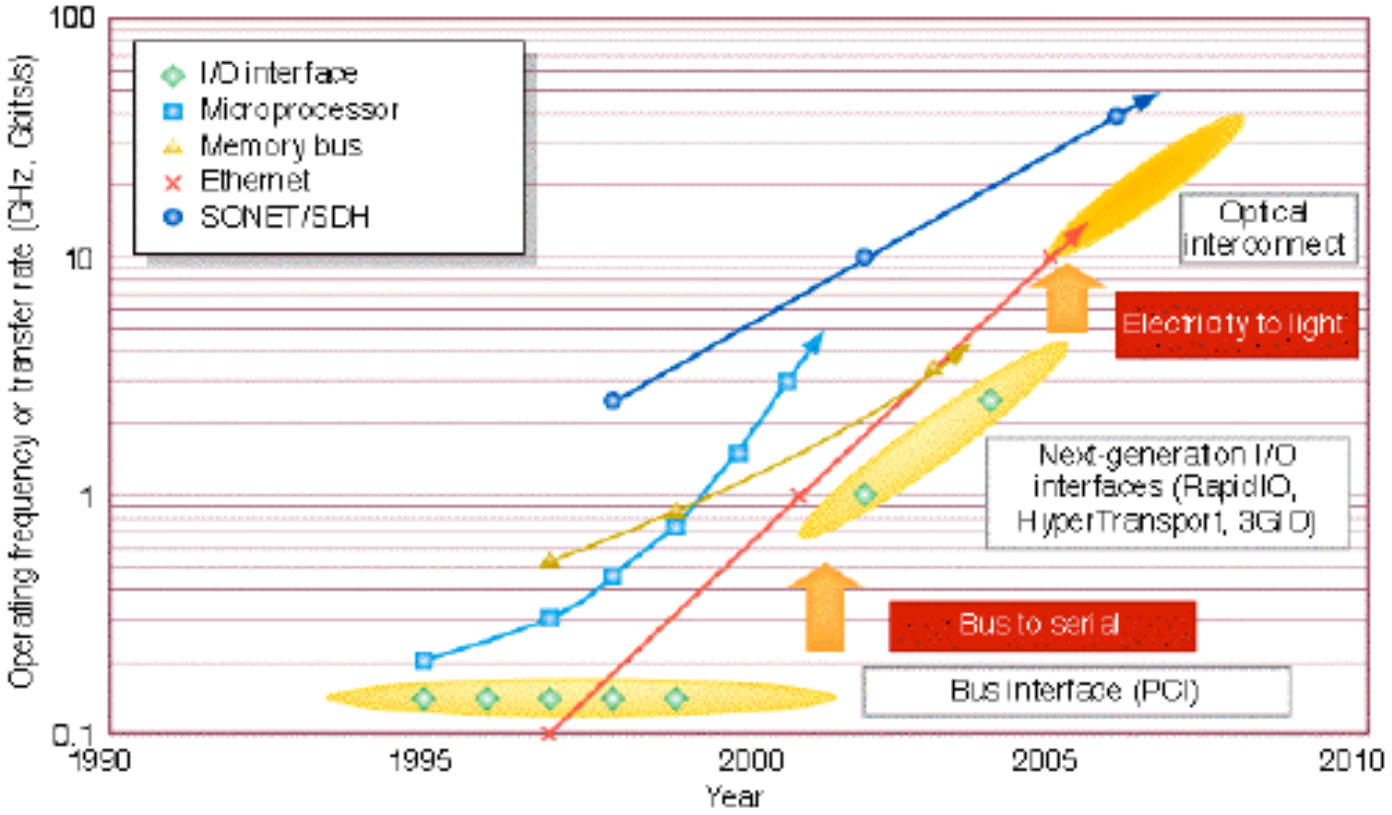
Value to Market



Nikkei BP

“Faster” Backplanes

- Making the copper thicker
- Making the dielectric layer thinner
- Using dielectrics with lower loss tangents
- Adding more signal layers
- Minimizing the signal length
- Maximizing distance between signals
- Making the board larger (wider and longer) to handle more signals per layer

Copper Roadmap

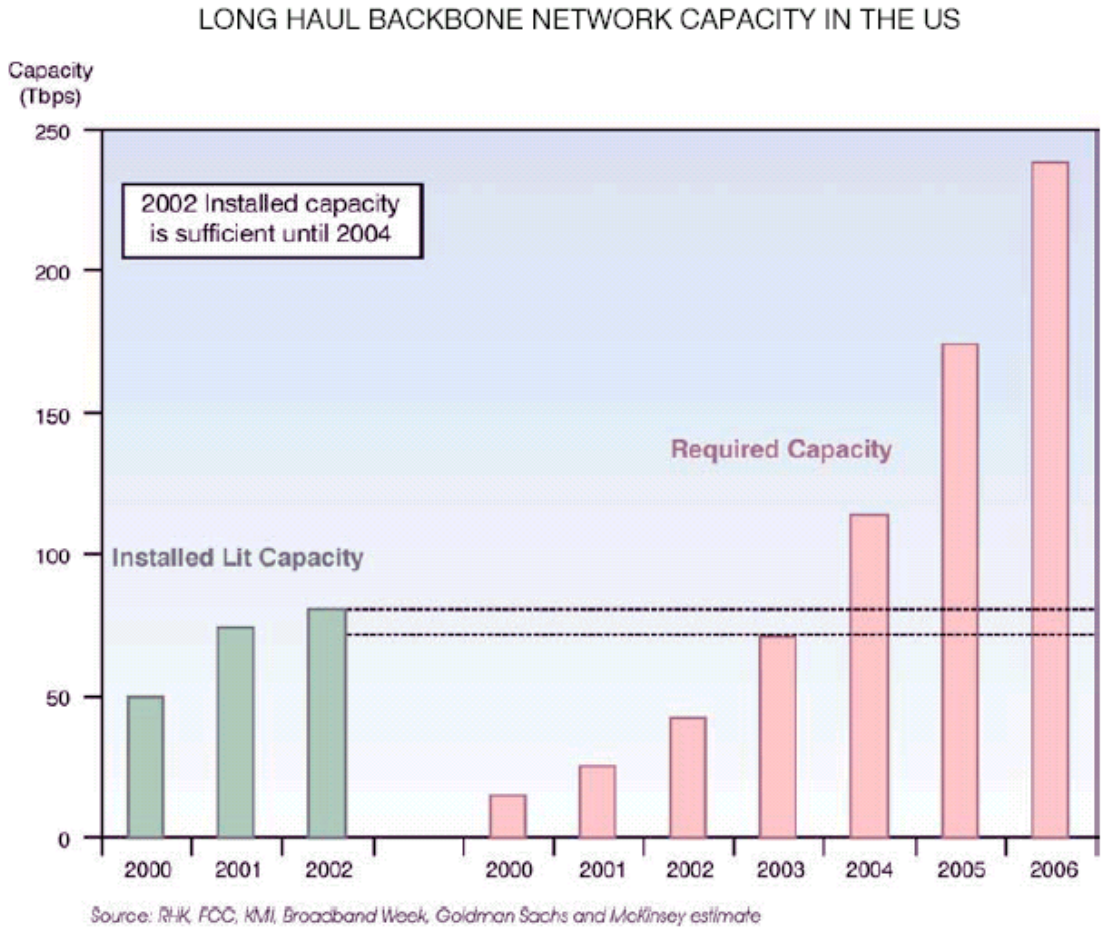
Generic Copper Backplane Bandwidth Technology Roadmap

PCB Technology	Materials	FR-4, Df = 0.020	PPO / CE, Df = 0.015-0.008	BT / APPE, Df = 0.010	PTFE, Df = 0.009 - 0.003	PTFE / Ceramic,	Df = 0.002 - 0.0009
	Processes						
	Transmission Line Design	Single transmission line, Length management		Differential pair, length, type (Surface microstrip, embedded microstrip, stripline, edge coupled, broadside coupled), location in stack			
	Via Design	Decrease PTH diameter, Remove non-functional pads, Increase anti-pad diameter (Clearance ring)					
	Connector Launch Design	Pad in via or PTH, micro vias, buried vias					
Connector Technology	Teradyne connectors	HDM	VHDM & VHDM L-series	VHDM-HSD	Gbk	GBx	
	ERNI connectors	ERmet	Ermet	Ermet ZD	ERmetZD	Ermet Zero XT	
	Tyco connectors	HM-ZD	Z-Pack HM-ZD MultiGig RT-1	Z-Pack HM-ZD	MultiGig RT-2	MultiGig RT-3	
	FCI	Metral 2000	AirMax VS Metral 4000	AirMax VS	AirMax VS	AirMax	
	Fujitsu		FCN-261Z00x		FCN260D		
	Winchester		Xcell			SIP-1000 I platform	
	Molex	Molex is a Teradyne licensee					
Receiver / Transmitter Signal Conditioning Chip Set	Taps required	None Required		One		Two	Mu
	Velio		GigaCore		GigaCore2		
Bus Architecture		Shared Bus ? Point to Point ? Multi point ? Sub type?					

Market Concepts

- Telecom capex dropped in ’03
  - Internet bubble effects still present
- Recovery in the ’04-’05 timeframe
  - Despite bubble, internet usage doubles every year

Market Status



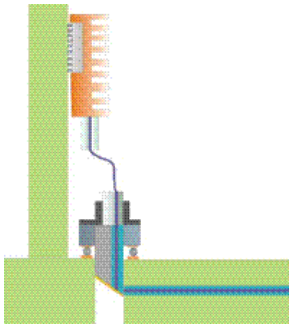
Courtesy of Prismark, September 2002

Optical Backplanes

- Today: optical fibers / fiber mat on surface
  - Point-to-point limitation
  - Splice or connector required for each fiber end
  - **Costly**
- Future: planar optical waveguides
  - Patternable layer on or within PCB
  - Bus architecture
  - Laser/detector arrays “self-aligned” in assembly

Current Challenges for Future Optical Backplanes

- Optical connector technology
  - Through-hole or SMT?
- Turning 90º with acceptable loss
- Reliability
- Manufacturability
- ***Cost of components and assembly***



The Cost Model

Microsoft Excel - PCB Model v4

File Edit View Insert Format Tools Data Window Help Acrobat

	A	B	C	D	E	F	G	H	I	J	K	L	M	N
1														
2	**DESIGN ISSUES**													
3	Product Name	Cu backplane			PROD									
4	Annual Production Volume	117	(000) board per year		VOL								Cost Preview	
5								Other assumptions:						
6	Panel Length	24	inch		PLEN			8	mil lines					
7	Panel Width	20	inch		PWID			8	mil spaces					
8								20	mil minimum drill diameter					
9	Finished Board Length	20	inch		BLEN			24	in max conveyor width					
10	Finished Board Width	18	inch		BWID			[the inputs above do not yet affect the model]						
11	Number of Drilled Through-Holes	5,000	per board		NHOLES									
12														
13	Minimum Panel Edge Margin	0.8	inch		PMARGIN									
14	Minimum Space Between Boards	0.1	inch		BMARGIN									
15	Boards Per Panel	1			BPPAN									
16														
17				Wgt Price			Lam	Price/sqft						
18	Number of Innerlayer Pairs - FR-4	15	100%	$2.17			FR-4	$2.17						
19	Number of Innerlayer Pairs - Type 1	0	0%	$0.00			Type 1	$6.00						
20	Number of Innerlayer Pairs - Type 2	0	0%	$0.00			Type 2	$0.00						
21	Number of Innerlayer Pairs - Type 3	0	0%	$0.00			Type 3	$0.00						
22	Number of Innerlayer Pairs - Type 4	0	0%	$0.00			Type 4	$0.00						
23	Number of Innerlayer Pairs - Type 5	0	0%	$0.00			Type 5	$0.00						
24	Number of Innerlayer Pairs - Type 6	0	0%	$0.00			Type 6	$0.00						
25	Number of Innerlayer Pairs - Type 7	0	0%	$0.00			Type 7	$0.00						
26	Number of Innerlayer Pairs - Type 8	0	0%	$0.00			Type 8	$0.00						
27	Number of Innerlayer Pairs / Avg Price	15	NIP	$2.17										
28														
29	Yield of Innerlayer Pairs	94.0%			INNERYIELD									
30														
31	Yield of Boards, Post-Lamination	99.2%	^ number of innerlayer pairs											
32	Yield of Boards, Post-Lamination	88.0%			TOTYIELD									
33														
34														
35	**PROCESSING ISSUES**													
36		***Sequence of Operations***												

Product Description | Facility Description | Operation Database | Cost Summary | Co

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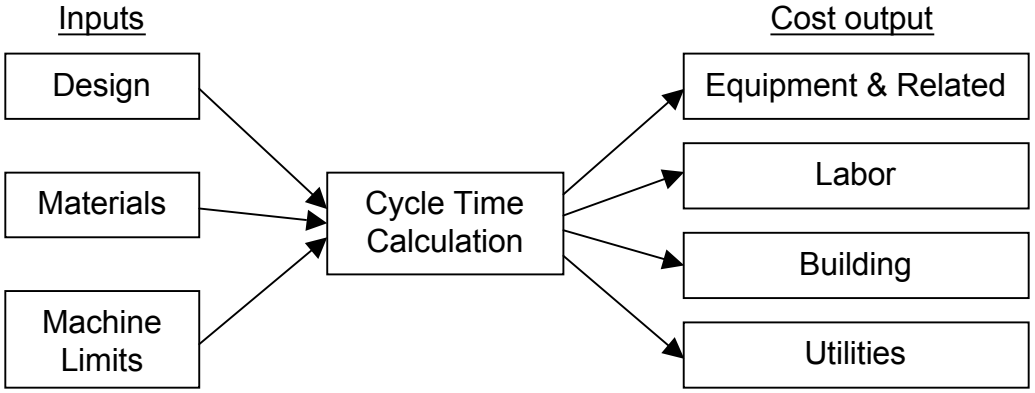
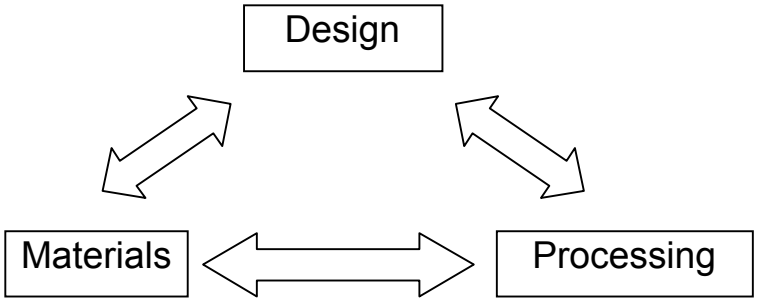
Models in Manufacturing

- Cost models
  - "Bottoms-up" like activities based costing
  - Engineering relationships
  - Purchasing inventory for BOM optimization
  - Scope: the mfg facility
  - Output: cost per part by operation and by factor (materials, equipment, and so on)
- Pricing models
  - Rules of thumb based on reference parts
  - Accounting data dependency
  - Profit included
  - Scope: include all business costs
  - Output: price per part
- Business models
  - "Bottoms up"
  - Scope: all of the business
  - Output: ROI, time to breakeven, NPV, and others

Cost Modeling Method

- Based on Technical Cost Modeling, as developed by IBIS Associates / MIT
- Activities Based Costing, plus engineering relationships
  - Cycle time = f(design, machine speed)





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Cost Model Context

- North American facility
- Equipment investment assumes max 24 inch width conveyors
- Yields reflective of 8 mil line / space
- Drilling reflects 20 mil minimum diameter
- Medium throughput (350Ksqft/yr topsurface)

Facilities Assumptions

Direct Labor Wage	$15.00	/hour
Indirect Labor Salary	$50,000	/year
Indirect Laborers:Direct Laborer Ratio	0.07	ilab/dlab
Indirect Labor Shifts per Day	1.2	shift/day
Benefits on Wage/Salary	35.0%	
Working Days per Year	360	d/yr
Working Hours per Day	24	h/d
Capital Recovery Rate	8%	/yr
Working Capital Period	1	mo(s)
Equipment Depreciation Life	5	yrs
Building Recovery Life	20	yrs
Total Space:Work Space Ratio	1.25	: 1
Price of Electricity	$0.110	/kWh
Dedicated Equipment?	0	[1=Y 0=N]
Equipment Investment Scaling Factor	100%	of baseline
Non-Recurring Engineering	$1,000	per design

Product Assumptions

- 32 metal layers
- No buried vias
- FR-4
- 24x20 inch panel
- 20x18 inch finished board
- 5,000 drilled holes per board
- ~1-3 Gbps performance

Process Flow

INNERLAYER	
Rec1	Receive Laminate
Cln1	Clean - Chemical
Pat1	Laminate Dry Film
Pat2	Expose Dry Film
Pat3	Photo Plotter
Pat4	Develop Dry Film
Pat5	Etch Cu - Strip Resist
Pat6	Film Punch
Pat7	Registration Punch
Ins1	AOI
Prp1	Oxide Coating System

OUTERLAYER	
Lam1	Receive Prepreg
Lam2	Receive Foil
Lam3	Kitting and Lay-up Area
Lam4	Laminate Multilayer (Press)
Lam5	Routing - Depin and Debook
Lam6	Deflash & ID
Drl1	Pin Stack - Before Drill
Drl2	Drill Through Holes
Drl4	Deburring
Drl5	Auto Hole Check
Drl6	Desmear & Etchback - PM
Plt1	Plate E'less Cu
Plt2	E'lytic Strike Cu
Cln2	Clean - Pumice Scrub
Pat1	Laminate Dry Film
Pat2	Expose Dry Film
Pat3	Photo Plotter
Pat4	Develop Dry Film
Plt3	Plate E'lytic Cu & Sn
Pat8	Strip Resist, Etch Cu, Strip Sn
Drl8	Manual Hole Size Check
Ins1	AOI
Rep1	Repair Opens & Shorts
Cln1	Clean - Chemical
Sma1	Flood Coat Solder Mask (DS Scree
Sma2	Tack Cure
Sma3	Expose Solder Mask
Sma4	Develop Solder Mask
Sma5	UV Cure
Sma6	Cure
Hsl1	HASL & Clean
Nmn1	Nomenclature Print
Fin1	Routing - Depaneling
Fin2	Clean
Ins2	Electrical Test
Ins3	Flying Probe
Fin3	Find, Analyze, Repair, Retest
Ins4	Final Inspection & Audit
Fin2	Clean
Fin4	Final packaging & labeling
Wst1	Waste Treatment
Nre1	Non-recurring Engineering

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Cost Summary

Cost Summary (per board)

Innerlayer Cost	$416	74%
Outerlayer Cost	$144	26%
Total Cost	*$560*	

Cost/Sqin (Top Surface, Board)	$1.55
Cost/Sqin (Top Surface, Panel)	$1.17
Cost/Sqin (Per Metal Layer)	$0.036

Total Equipment Investment	$44.0 MM
Total Building Space	23.0 K sqft
Total Building Investment	$2.1 MM

Cost Factor Breakdown (per board)

	Dir Labor	*Material*	*Utilities*	*Tooling*	*Equip*	*Bldg*	*Ind Labor*	*Maint*	*Capital*
Innerlayer Cost	$86	$258	$2	$10	$34	$0	$9	$7	$10
% of innerlayer	*21%*	*62%*	*0%*	*2%*	*8%*	*0%*	*2%*	*2%*	*2%*
Outerlayer Cost	$33	$49	$1	$18	$25	$0	$5	$5	$7
% of outerlayer	*23%*	*34%*	*1%*	*13%*	*18%*	*0%*	*4%*	*4%*	*5%*
Total Cost	**$119**	**$307**	**$3**	**$28**	**$59**	**$1**	**$14**	**$12**	**$17**
% of total	*21%*	*55%*	*1%*	*5%*	*11%*	*0%*	*2%*	*2%*	*3%*

Validated by two backplane fabricators:
+/- 10% of their costs

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Cost Analysis

	No. of Drilled Holes	No. of Metal Layers	Post Lam'n Yield	**Total Board Cost**	Cost per Board Metal Layer	Cost per Top Panel Surface Sqin	Cost per Top Panel Surface Sqin Metal Lyr	Total Equipment Invest (MM)	Total Building Space (Ksqft)
Baseline Case	5,000	32	88%	**$560**	$17.49	$1.17	$0.036	$44	23.0
Holes Lower	**2,500**	32	88%	**$545**	$17	$1.14	$0.036	$43	22.1
Holes Higher	**7,500**	32	88%	**$574**	$17.94	$1.20	$0.037	$45	24.2
Holes Highest	**10,000**	32	88%	**$588**	$18.39	$1.23	$0.038	$46	25.1
Layers Lower	5,000	**24**	91%	**$423**	$17.61	$0.88	$0.037	$38	20.0
Layers Higher	5,000	**36**	86%	**$634**	$17.61	$1.32	$0.037	$47	24.4
Holes & Layers Lowest	**2,500**	**24**	91%	**$411**	$17.14	$0.86	$0.036	$37	19.1
Holes & Layers Highest	**10,000**	**36**	86%	**$668**	$18.56	$1.39	$0.039	$49	26.5

“The Metric”

So far, cost has focused on board cost

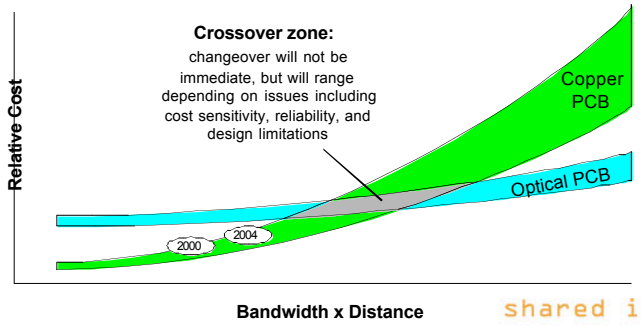
But is that fair comparison for optical PCBs?

- Performance will be at a different level
- Connectors will be different
- Assembly method probably different

So, what metric to use?

“The Metric”

- **Cost per Gbps per top surface square inch:** takes into account the number of metal layers (not including ground/power planes), maximum Gbps per channel, and maximum channels per inch (as determined by minimum line/space rules)
- **Cost per Gbps per channel per meter:** takes into account losses per unit length and maximum Gbps per channel
- **Cost per Gbps per board:** takes into account design-dependent maximum Gbps for all channels on the board at any one time
- **Cost per Gbps per board cross-section:** takes into account maximum Gbps per channel and the number of channels cut by a cross-section dividing the length of the board into equal parts
- Suggestions?



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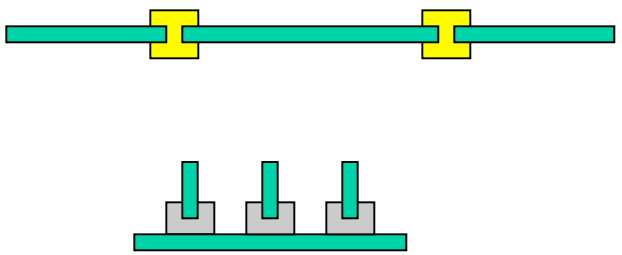
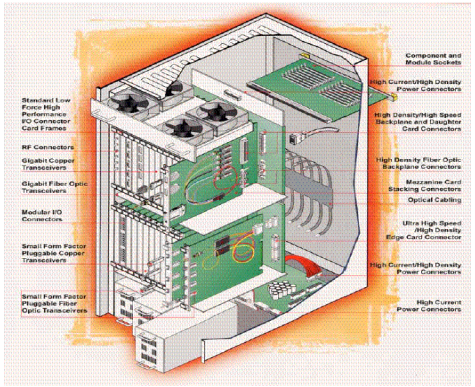
Future Work

- Next generation copper PCB for 10Gbps
- Assembly costs
- Optical PCB technology
  - Embedded, edge-coupled
  - Embedded, surface-coupled
    - Mirror/grating/in-via-coupling
    - Bent waveguide



Summary

- Copper backplane model in place & validated
- Your input on optical technology needed
- Your input on cost-performance metric needed



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