

# Electrical/Optical Cost Model Using A 10Gb/s Star Architecture

3280 Gb/S Backplane Bandwidth

1280 Gb/S User Bandwidth

2.5x Backplane Overspeed



# Cost Model Methodology

## System assumptions:

- ◆ **16 slot shelf; 14 I/O slots, 2 switch slots**
- ◆ **Sixteen 10Gb/s optical transceivers**
- ◆ **Redundancy**
  - **Connection to both switch modules from each I/O module**
- ◆ **Backplane Overspeed**
  - **1.2-2.5x**
- ◆ **Backplane frequency**
  - **10Gb/s**

## Determine components/costs to implement backplane with:

- ◆ **10G PAM4**
- ◆ **10G NRZ**
- ◆ **Optical BP (fiber based)**

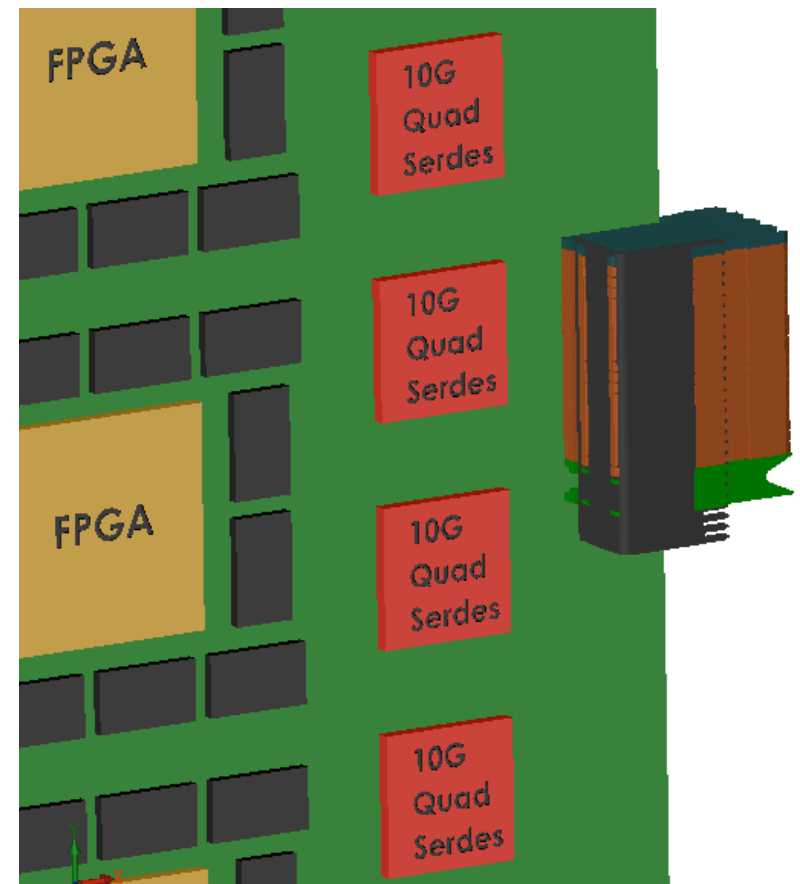
**Cost difference is calculated between different implementations; no assumptions yet on yield, testing, maintenance, design cost**

# Other Assumptions

- ◆ Optical transceivers are 12 channel, 10Gb/s (not currently available)
- ◆ The optics on the backplane are cable-based or a simple optical shuffle
- ◆ The costs of the optical connector are per mated fiber connection
- ◆ The difference between copper and optical interconnect are based on the components required to create the interconnect at the backplane. No architecture differences are assumed

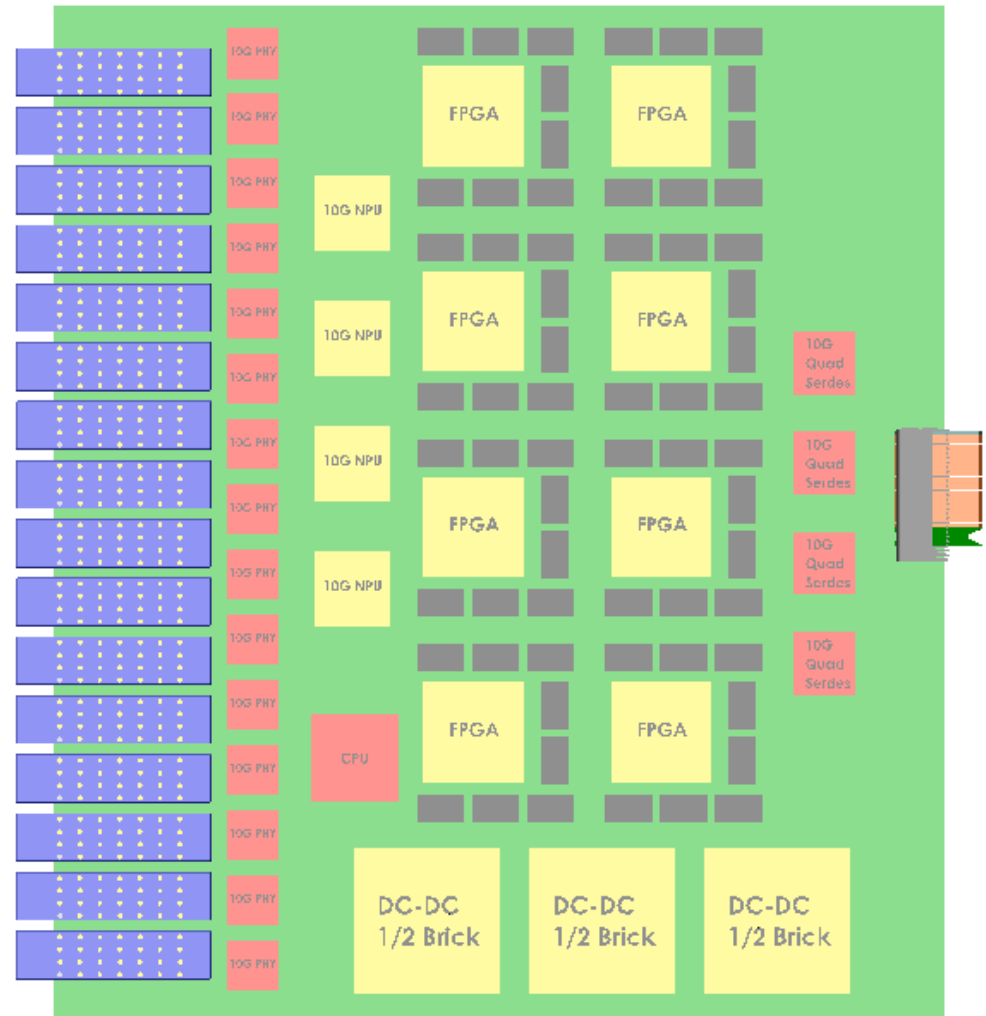
# I/O module layout - cont

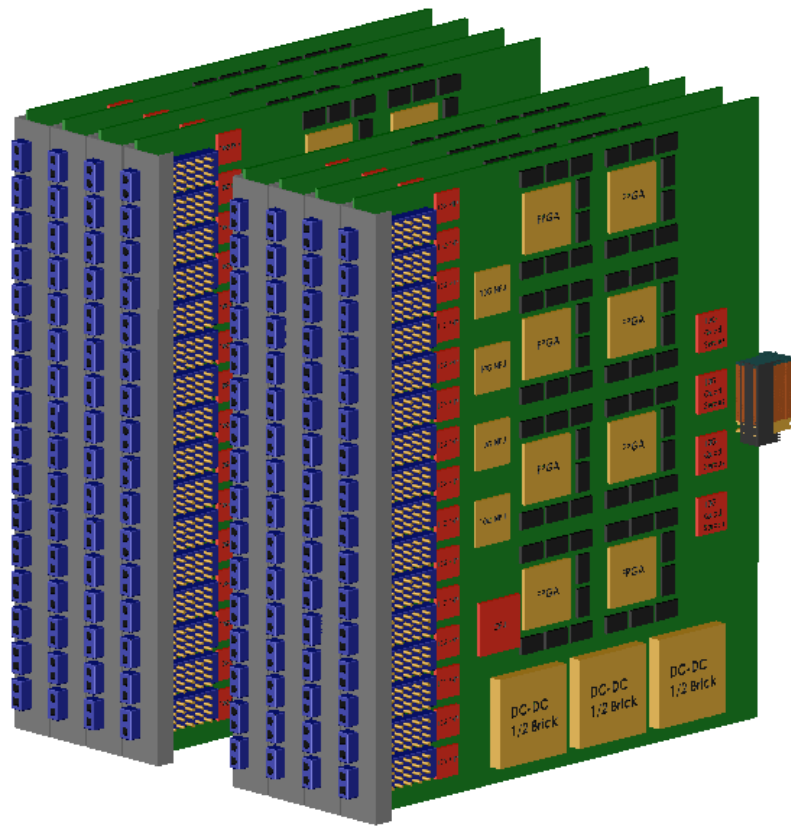
- ◆ The BP serdes are typically higher integration (Quad)
- ◆ The Connector is low in pin count but high in performance.
- ◆ “Wire Speed” =  $16 \times 10\text{Gb/s} = 160 \text{ Gb/S} \times 1.25 = 200\text{Gb/s}$  to Each Fabric.
- ◆ BP Overspeed needed for: Cell segmentation, headers, multicast traffic, and tags added by the NPU.
- ◆ 32 channels to each fabric. 64 total channels = 128 diff pairs.



# I/O module layout - cont

- ◆ I/O Module is done!
- ◆ Switch Fabric is next
  - Density challenges are at the fabric.





- ◆ 8 Line Cards on 1.2” Pitch
- ◆ Two Center Fabric Slots
- ◆ 8 x 400Gb/S = 3.2 Tb/S
- ◆ Connector Locations Drive  
Routing Layers and Cost on BP

