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iNEMI High-Reliability Task Force

Pb-Free[1] Manufacturing Requirements for High-Complexity, Thermally Challenging Electronic Assemblies

As the deadline for member state implementation of the European Union's Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (better known as the RoHS Directive) draws near, the electronics industry is working toward eliminating lead (Pb) used in processes, components and materials. However, this conversion to Pb-free alloy systems — typically SnAgCu (SAC) alloys —is causing concern among manufacturers that produce high-complexity thermally challenging products. Although many of the companies producing these products are planning to take advantage of the Pb exemptions to the RoHS Directive in the short term, these exemptions may not be available forever. The broad component mix, board thermal properties and resulting thermal gradients across these complex assemblies pose many thermal challenges and push the current capability limits of the soldering materials, maximum qualified component temperatures and primary attach and /or rework equipment. To meet these challenges, manufacturers are looking to the supply chain to provide materials, components and equipment capable of meeting these requirements.

The iNEMI High-Reliability (Hi-Rel) Task Force consists of electronic product manufacturers (OEMs and EMS providers) whose products are characterized by long service life and high-reliability requirements. (See Appendix A for a list of companies.) For these companies, maintaining product reliability is absolutely critical to survival. The Task Force has developed these recommendations to address the primary areas of concern for complex, thermally challenging electronic assemblies. In addition, this group intends to work with the appropriate standards bodies to help shape formal standards which will support evolving manufacturing needs.

Components

Component suppliers should address the requirements of J-STD-020C for all nonhermetic solid state surface mount devices to the maximum exposure temperatures specified in Table 4.2 of J-STD-020C for primary attach and rework.

For other non-IC, MCM, and SiP devices, it is recommended that the procedures outlined in J-STD-020C be used for establishing MSL ratings and peak temperature survivability. To be useful to moving forward, certain industry specifications, namely IPC-9503 and IPC-9504, should be updated to reflect Pb-free processing requirements.

Small surface mount devices (SMDs) that will be attached to the bottom side of a printed circuit board and then passed through a wave solder or solder dip machine (full body immersion) should meet the requirements of JESD22A111. Typical examples of components frequently wave soldered in this manner include (but are not limited to) small discrete components, SOT-23, and lower I/O leaded devices with pitch ≥ 1.27mm / 0.050 inch. JESD22A111 specifies a maximum exposure temperature for SnPb wave soldering of 260°C (+5/-0°C) for a maximum 10 (+/-1) seconds. Minimum hole-fill requirements for PTH devices (per IPC-A-610) also drives the need to increase solder pot temperature. Therefore, the maximum exposure temperature during testing should be increased to 265C minimum to accommodate the new alloys used for Pb-free wave soldering. To help offset this hotter temperature, the time required

[1] For purposes of this paper, "Pb-free" (or "lead-free") does **not** mean that no lead is present, but rather it means that the concentration level of lead in a homogeneous material is less than 1000 ppm.

at 265C can be reduced to 5 seconds minimum (laminar and chip wave combined).[2] Users should ensure that these are the maximum conditions the components experience during actual wave solder assembly. We recognize, however, that some thermally sensitive components will require special handling or fixtures if used on the bottom side.

All suppliers of BGAs or other area array packages should address the requirements of JEDEC Publication 95 co-planarity specification for the appropriate package outline specifications at room temperature. They should also address assembly capability when packages are subjected to the maximum reflow temperatures as specified in Table 4.2 of J-STD-020C.

Laminate and Other PWB Fabrication Materials

While laminate materials used for assembly with SnPb have been used successfully in lower complexity assemblies at Pb-free (i.e. SAC) processing temperatures, there are issues in using these materials for complex, thermally challenging products at these temperatures. Moving to higher temperatures increases materials sensitivities and the number of parameters (e.g. Td, Tg, CTE(x-y), CTE(z)) that must be re-examined. More testing and evaluation is required before each new laminate material can be stated to be compatible for assembly with Pb-free materials for its intended applications in high-complexity systems. After initial material selection, the manufacturer will need to validate acceptable performance of the materials in the use condition. Table 1 summarizes some of the potential test methods for validation of performance, including CAF and thermal/temperature cycling.

Equipment

Capability limits of the primary attach and rework equipment are strained by higher thermal mass PWBs and assemblies, and it is difficult to not exceed the minimum and maximum temperature limits imposed by J-STD-020C and JESD22A111.

We recommend that product and process designers work with equipment providers to integrate and resolve the issues of process speed, peak temperatures, flux chemistry, solder pot contamination and soldering gas atmosphere.

Reflow profiling studies using SnAgCu as the soldering material of various thermally challenging products have demonstrated that to stay below the upper component body temperature limits as defined by J-STD-020C while simultaneously staying above the minimum temperature to create a good solder joint requires that the oven be slowed down therefore extending the overall processing time by 20-30% and putting significant additional strains on the soldering materials. Key issues from a materials perspective include:

- ability of flux to handle higher temperatures at longer pre-heat times (135-200C for 3-4 minutes)
- total profile times of 8-9 minutes

Rework of large assemblies also presents challenges in the ability of the equipment to effectively heat the module being reworked while at the same time not overheating any adjacent components. Techniques to improve reworkability include:

- whole board preheat to reduce heatsinking effects of PWB power and ground planes
- improved adjacent component "shielding" from hot gas rework temperatures to prevent secondary reflow

The preheating of PWBs is also an issue when reworking PTH components. The higher tin content combined with the slower wetting/spreading of SnAgCu compared with SnPb results in the need for higher solder pot temperatures and longer contact time to achieve the same degree of hole fill. This manifests itself into higher Cu dissolution of the barrels and traces on the PCB requiring tighter controls of the rework processes and / or equipment.

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[2] 265°C for 5 seconds minimum is based on a wave solder pot temperature of 260°+/-5°C, a minimum wave solder conveyor speed of 3.25 feet/minute (0.65 inches/second), and a maximum wave contact distance (chip wave plus laminar wave) of 3.25 inches.

Table 1

Parameters for Pb-Free PWB Fabrication Materials		
Characteristic	**Test Method**	**Comments / Suggested Value [1]**
Decomposition temp, Td, (5% weight loss by TGA) [2,3]	IPC-TM-650.2.4.24.6	≥325°C
Glass transition temperature (T_g), ºC, by TMA [4]	IPC-TM-650.2.4.24.5	• Tg > 140°C for all products • >165°C for products with >10 layers, > 6:1 aspect ratio, or containing BGAs
In-plane coefficient of thermal expansion CTE(x-y), ppm/ºC,	IPC-TM-650.2.4.24C	Solder joint stress depends on peak processing temperature, component CTE
Out-of-plane coefficient of thermal expansion - CTE(z), ppm/ºC, α_1 (above Tg) and α_2 (below Tg)[5]	IPC-TM-650.2.4.41	Via/PTH barrel and land stress depends on peak processing temperature, PTH copper ductility
Secondary Parameters		
Time to delamination (T-260)	IPC-TM-650.2.4.24.1	≥ 30 minutes
Time to delamination (T-288)	IPC-TM-650.2.4.24.1 modified per paragraph 6.1 to 288°C	≥ 5 minutes
Test Method, Special		
Copper ductility – PTH barrel	IPC TM 650, 2.4.2	Depends on peak processing temperature, and PTH aspect ratio
Product Level Validation		
Solder float at 288°C (6X)	Similar to IPC Test Method TM650, 2.4.13 except loaded with SAC solder	First article cross-sections must pass
Conductive anodic filament (CAF) testing	Pre-conditioning + IPC 9691, IPC-TM-650, Method 2.6.25	Pass

NOTE 1: Suggested values are highly dependent upon the product being assembled. The values suggested are based on thermally complex high layer count boards that have high material resin content, require multiple Pb-free soldering processes at or near the limits of the J-STD-020C profile requirements, and have long life requirements. Specific values will vary with the requirements of the individual products.

NOTE 2: TGA – Thermo-gravimetric analysis.

NOTE 3: Td, a characteristic determined by a standard test method and evaluated at 5 minutes, is substantially higher than delamination temperatures evaluated at 30 and 5 minutes. Td should be used to compare similar materials, and not used as an absolute value in isolation.

NOTE 4: Thermo-Mechanical Analysis (TMA) is preferred over DSC and DMA in determining T_g because total expansion from room temperature to the maximum processing temperature is a critical product parameter and because TMA reports the expansion of the material as a function of temperature.

NOTE 5: The z-axis CTE's (Z Axis Expansion (%) per IPC TM 650, 2.4.41 (50 -260ºC)), both below and above Tg, are important to long-term reliability. Users and their product manufacturers should ensure that the materials specified and the associated plated-through-hole copper wall thickness and copper ductility will meet long-term reliability requirements of the products.

iNEMI Hi-Reliability Task Force

The following companies support the conclusions of this document:

Agilent Technologies, Inc.
Alcatel
Cisco Systems, Inc.
Celestica, Inc.
Delphi Electronics & Safety
Hewlett-Packard Company
IBM Corporation
Intel Corporation
Jabil Circuit, Inc.
Lucent Technologies
Plexus Corp.
Sanmina-SCI Corporation
Solectron Corporation
Sun Microsystems, Inc.