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International Electronics Manufacturing Initiative

Halogen Flame Retardant (HFR)-Free Leadership

January 20, 2009

Advancing manufacturing technology

Agenda

- **HFR-Free Transition Proposal – M. Rausch, Intel**
  - Market Analysis
  - Technology Envelope Proposal
  - Product Conversion Goals
  - Discussion of Proposal
- **Time Line and Initial Project – Steve Tisdale, Intel**
- **Next Steps – Bob Pfahl, iNEMI**

HFR-Free Proposal

Objective

1. Identify BFR-free PCB technology envelope which allows drop in replacement capability with standard FR4-based designs.
2. Identify technology readiness, supply capability and reliability characteristics for "BFR-free" alternatives to conventional printed wiring board materials and assemblies.
3. Provide Industry Standard Technology Envelope for BFR-free Materials across all market segments

HFR-Free Proposal

Market Analysis

MARKET AND GROWTH OF RIGID LAMINATE

	Area (Mm²)	2006	2007	2012	Value CAAGR ('07-'12)
FR 4	FR 4 Total	256.8	284.4	430.3	8.6%
	Notebook		18.0	39.1	16.7%
	Desktop		35.3	40.4	2.7%
	Mobile Phone		14.7	21.6	8.0%
	Other (Server, consumer)		216.4	329.2	8.8%
HFR-Free FR 4	Area (Mm²)	2006	2007	2012	Value CAAGR ('07-'12)
	HFR-Free FR 4 Total	11.4	20.9	60.9	23.9%
	Notebook		3.9	13.8	29.0%
	Desktop		1.8	5.2	23.6%
	Mobile Phone		7.5	21.4	23.4%
	Other (Server, consumer)		7.7	20.5	21.6%

CAAGR: Compound aggregate annual growth rate

If HFR-Free supplants standard FR4, CAAGR grows to almost 70%

(Potential for significant supply chain disruptions)

HFR-Free Proposal

Market Analysis

LAMINATE SCORECARD

Material	Dk	Df	Moisture Absorption	Tg	CTE	Flexure	Td	T260 /Cu	T288 /Cu	Peel Strength	IST	CAF	UL94V0	Shock	Vibe	Temp Cycle
A	Red	Green	Yellow	Yellow	Green	Red					Green	Green	Green	Red	Red	Yellow
B	Red	Green	Yellow	Yellow	Green	Red	Green	Green	Yellow	Green	Green	Green	Green			
C	Green	Green	Yellow	Yellow	Green	Red	Green	Green	Green	Green	Green	Green	Green	Red		
D	Green	Green	Yellow	Yellow	Green	Red	Green	Green	Green	Green	Green	Green	Green			
E	Green	Green	Yellow	Yellow	Green	Red	Green	Green	Yellow	Yellow	Green	Green	Green			
F	Red	Green	Yellow	Yellow	Green	Red	Green	Green	Yellow	Green	Green	Green	Green			
G	Yellow	Green	Yellow	Yellow	Green	Red	Green	Green	Yellow	Green	Green	Green	Green	Red	Red	Yellow
H	Yellow	Green	Yellow	Yellow	Green	Red	Green	Green	Yellow	Yellow	Green	Green	Green			
I	Yellow	Green	Yellow	Yellow	Green	Red	Green	Green	Green	Green	Green	Green	Green			
J	Yellow	Green	Yellow	Yellow	Green	Red	Green	Green	Yellow	Green	Green	Green	Green			
K	Green	Green	Yellow	Yellow	Green	Red	Green	Green	Green	Green	Green	Green	Green			

Color Code
- Green: Equal to or better than FR4 (No issue)
- Yellow: Marginal vs FR4 (Issue not clear)
- Red: Worse than FR4 (Clear Issue)
- White: No Data

Derived from iNEMI WG data

Material improvements will be required to meet “interchangeable with FR4” goal

(simplifies DIMM, PCIe add-in card transition)

HFR-Free Proposal

Technology Envelope Proposal

	New Value or Test Proposal			
	Property	Value		Unit
		Maximum	Minimum	
	Modified Value Range of STD Test			
1	Permittivity (Dk or Er), maximum			
	@ 1MHz			
	@ 1GHz			
	Scan range 1-20 GHz			
2	Loss Tangent (Df), maximum			
	@ 1MHz			
	@ 1GHz			
	Scan range 1-20 GHz			
3	Moisture Absorption, maximum		NA	
4	Flexural Strength, minimum	NA		
	Length direction			
	Cross direction			
5	Flammability			
6	Decomposition Temperature (Td)			
7	Z-Axis CTE			
	Alpha 1			
	Alpha 2			
	50-260C			
8	Young's Modulus			
9	Thermal Resistance			
	T260			
	T288			

DRAFT

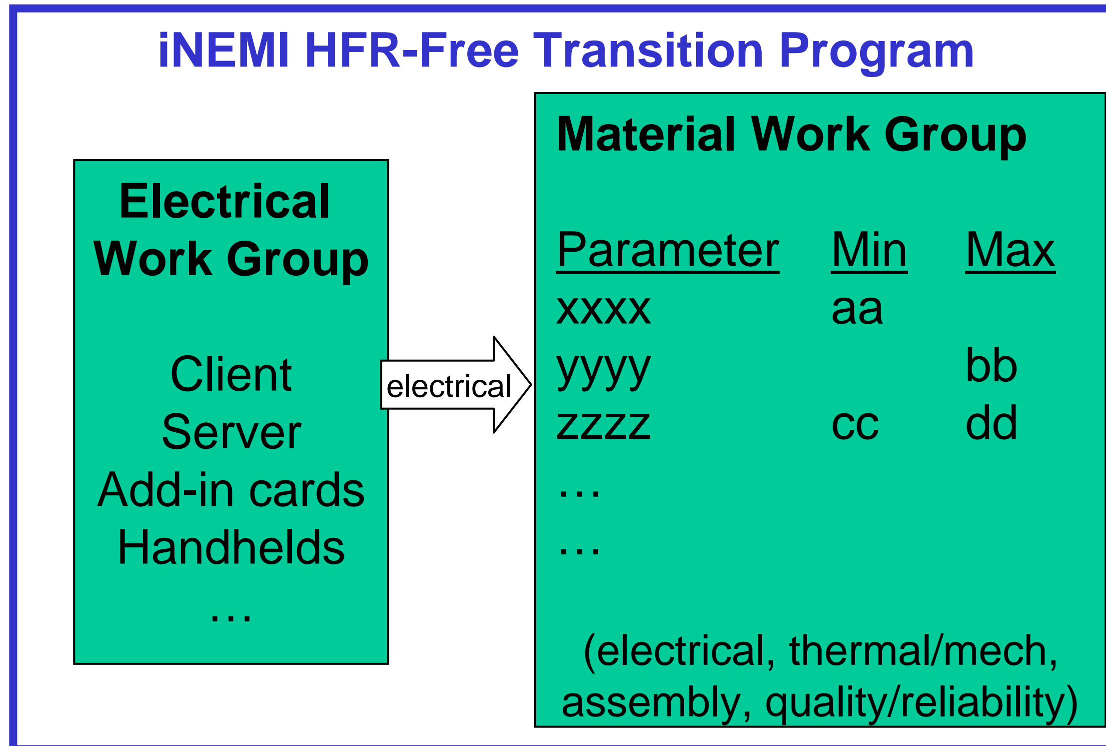
Proposal

- Identify key parameters
- Validate acceptable range of values
- Establish test methods

Objective

- Align entire supply chain behind common requirements

Technology Envelope Proposal



Program Lead:
Martin Rausch
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Electrical WG Lead:
Steve Hall, Intel

Materials WG Lead:
John Davignon, Intel

Keys to success

- **Gain participation from all members of supply chain**
  - OEM, ODM/EMS, PCB suppliers, Laminate suppliers, DIMM/add-in card suppliers
- **Member companies ensure technology envelope meets requirements**
  - Reliability, cost, availability, performance, etc…
- **Envelope gets used (de-facto standard)**
  - Specify product, drive new material development, etc…

Participation Requirements

All Participants Must:

1. **Agree on a transition date to HF PCB Materials**
    - Possibly by application / market segment
    - Full BOM enabling will be driven by OEM/ODM (This is due to the complexity of business models)
2. **Commit appropriate resources to meet project timeline**
    - Participate in Electrical and Material WG efforts to define technology envelope and test metrologies
    - Provide materials, components, test vehicles, and assist with modeling/design/assembly/test/failure analysis as needed
3. **Agree to use the HF PCB technology envelope parameters in future designs**
4. **Support industry standard recommendations to IPC/JEDEC (if applicable)**
    - HF PCB Technology Envelope

Is this acceptable?

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iNEMI HFR-Free PCB Technology Envelope Project

Stephen Tisdale, John Davignon, Stephen H. Hall
Intel Corporation
January 20, 2009

iNEMI HFR-Free PCB Technology Envelope Project

Project Objective

- Identify BFR-free PCB materials and technology envelope which allow drop in replacement capability of BFR-free Materials with standard FR-4 PCB Designs
- Identify technology readiness, supply capability and reliability characteristics for “BFR-free” alternatives to conventional printed wiring board materials and printed wiring board assemblies
- Provide Industry Standard Technology Envelope for BFR-free Materials across all market segments

3 - Phase Approach:

1. Design
2. Test
3. Results

iNEMI HFR-Free PCB Technology Envelope Project

IS / IS NOT

This Project IS:	This Project IS NOT:
Technical evaluation of key electrical and mechanical properties of HFR-free Materials	**An EHS assessment**
Focused on those design attributes which are of most value to the broader industry	**Biased towards specific laminate suppliers, geographies, or market segments**
Build on learning from prior investigations	**Repeat of prior work**
Focused on circuit board materials and solder joint reliability – Board / Component Interaction	**Focused only on materials characterization**
Focused on generating data / design guidelines for development of an industry standard	

iNEMI HFR-Free PCB Technology Envelope Project

Phase I: Design

Review prior work and make recommendations for testing needed. Investigation should take into account needs of electronic product sectors represented by iNEMI membership.

1. **Identify candidate materials**
   - Poll the supplier base, keying in on candidate materials that are commercially viable with consideration for market segment applications.
   - Identify candidate BFR-free laminate materials to allow drop-in replacement for standard FR-4

2. **Identify key performance characteristics and test criteria (Mobile / Desktop / Other?)**
   - Assess prior studies and identify critical knowledge gaps or technical issues. Make recommendations for performance tests needed. Review results of prior industry and member company investigations.
   - Output broadband frequency dependant dielectric constant and loss tangent of candidate halogen free laminate materials (10KHz - 20GHz)
   - Simulation results of high speed buses …. DDR3, PCI2,3 … others?

3. **Design test vehicle(s) and test methodologies, leverage standards where possible**
   - Specify test vehicle criteria required for performance testing. Agree on a minimal number of test vehicle designs and test requirements.

iNEMI HFR-Free PCB Technology Envelope Project

Phase II: Test

Develop, manage, and execute performance testing.

1. **Develop evaluation plan and schedule**
   - Outline key mechanical and electrical performance characteristics, and resource and time constraints. Focus on Electrical Characteristics, Delamination and Via & PTH reliability, Pad cratering and solder joint reliability.
     - » Build systems with dielectric materials that comply with the proposed BFR-free dielectric spec
     - » Provide data that shows comparison to identical FR4 systems
     - » Determine compatibility of candidate laminate materials with higher temperature assembly process reflow environments (mixed solder: 245 C / Pb-free, 260C).
2. **Procure parts and test vehicles**
   - Obtain needed evaluation materials. Consider lead times needed to synch with evaluation schedule. Solicit participation from supply partners.
3. **Assign teams to carry out completion of the testing in a standardized fashion**
   - Each test should be carried out in a manner that produces meaningful results. Industry standards should be followed where applicable. Testing should be coordinated to allow correlation of results and sharing of test materials.
4. **Perform mechanical and reliability testing on test vehicles.**
   - Leverage capabilities and expertise of participating members and supply partners. Follow test procedures carefully and record positive and negative results.

iNEMI HFR-Free PCB Technology Envelope Project

Phase III: Results

Compile results, assess significance, make recommendations, and publish report.

1. **Assess technology readiness / identify gaps**
   - Flag unexplored issues and identify technical risks that need to be resolved before materials can be widely adopted. Make recommendations for future work.
2. **Assess manufacturing capability and supply capacity**
   - Work with suppliers and EMS's to identify barriers to supply chain viability. Interpret implications of performance testing in terms of manufacturing capability.
3. **Publish results**
   - Compile and edit concise summary of methods, meaningful results, and recommendations. Goal is to roll the final report to members by Y/E 2010 with public release by IPC/APEX 2011

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iNEMI HFR-Free PCB Technology Envelope Project

Anticipated Outcome

- **Validate electrical and mechanical properties**
  - Loss tangent and Dk modeling over required range of signal speed
  - Signal Integrity Capability / Validation (DDR2, DDR3 etc)
  - Mechanical performance validation for lead free assembly and rework (delamination)
  - Critical Test Parameter Evaluation (CAF, IST, flex, etc.)
- **Validate Board Level Reliability Capability**
  - PCB Modulus / Thickness Impact on Mechanical Capability
  - HF Board Level Assembly / Rework Process Characterization
  - Mechanical Characteristics (Pad Crater / Ball Pull etc)
  - CTE Characteristics
  - SJR (Shock / TC etc)
  - HF Component / HF PCB Interaction
- **Provide Industry with an accepted Standard Technology Envelope for BFR-free PCB Materials**

Participant Expectations

1. **Agree on identifying a transition date / timeframe to move to HF PCB Materials**
   1. Possibly by application / market segment
   2. Full BOM enabling will be driven by OEM/ODM (This is due to the complexity of business models)

2. **Agree to commit appropriate resources to meet accelerated project timeline and targeted end dates**
   1. Weekly Calls, FTF Meetings When Appropriate
   2. Provide Key Electrical / Mechanical parameter requirements by market segment to generate appropriate Stack Up Definitions, Test Plans and Identify Appropriate Material Candidates
      1. Intel to provide the initial strawman
   3. Agree to provide materials, components, Test Vehicles, Design Capability, Modeling Capability, PCB Fabrication, PCB assembly, Test Capability, FA Capability as required by Test Plan

3. **Collaborate on input to final report**

4. **Agree to adopt the HF PCB technology envelope parameters in future designs**

5. **Provide Recommendations for Industry Standards to IPC / JEDEC to generate and publish a Spec (if applicable)**
   1. HF PCB Technology Envelope (Design Guidelines)

iNEMI HFR-Free PCB Technology Envelope Project

Phase 1 Requirements

Signal Integrity Strategy

Steve Hall - Intel

Signal Integrity with Halide Free Boards

Problem

- The permittivity range for available halogen free dielectrics is too wide for a single design (**HF → 3.6≤e_r≤5.2, requires ~2-3 separate designs)**
- High end of permittivity range increases crosstalk, risk & cost
  - **More layers needed to compensate for crosstalk when permittivity is too high → leads to more cost**
- Industry specs such as PCIe are based on standard FR4 behavior
  - **Changing the FR4 assumption requires the specs to be re-visited**

Plan

Define an "*electrical envelope*" for HF dielectrics to ensure drop in compatibility with 1080 FR4

- **Eliminates need for multiple design guides (HF & FR4)**
- **Ensures industry specs (e.g., PCIe) remain valid**

Strategy

- Characterize available HF dielectrics
  - **Assess critical electrical properties**
- Simulation
  - **Define the "dielectric electrical envelope" based on DDR3 & PCIe2,3**
- Validation Platforms
  - **Ensure envelope is valid**

Signal Integrity Input

1. Consensus/input on the variables and ranges in the electrical envelope
   - Dk (Er)
   - Df (TanD)
   - Delta TanD due to Moisture Uptake
   - Frequency (10 MHz – 20 GHz)

2. Consensus on dielectric property measurement methods going forward
   - Split Post Resonator
   - Short Pulse Propagation (TDR)
   - Transmission Line Extraction (VNA)

Signal Integrity Input

3. Comparative data to FR4 Baseline (1080 cloth) validating the HF electrical envelope corners
   - Tangible (non-simulated) data is needed to ensure nothing was missed
     - Identification / Development / Characterization of passive test boards (Loss, impedance, crosstalk … etc. on HF vs FR4)
     - Apples / Apples comparison of DDR & PCIe margins on active systems (HF vs. FR4)
   - Description of test methodology for each current data set is critical

Signal Integrity Output

- **Identification of the key electrical parameters of the HF dielectric needed to ensure electrical performance on par with 1080 FR4**
  - Ensures drop in compatibility with FR4 Designs
    - Eliminates need for two sets of design guides (HF & FR4)
    - Ensures industry specs (e.g., PCIe) remain valid
    - Removes the signal integrity risk of HF PCBs

Note: HF electrical properties do not need to overlap 100% with FR4 … needs to be close enough

PCB Material Development Strategy

John Davignon - Intel

PCB Materials HF WG Strategy

- **Problem Statement:**
  - The majority of HF PCB Laminate Materials have Electrical and Thermo-Mechanical properties that make a smooth transition difficult.

PCB Materials Development Input

- **PCB Materials WG Goals:**
  - **Define a technology envelop to provide a set of FR-4 electrically equivalent HF PCB materials, and test methods/conditions which meets the quality and reliability requirements for all relevant market segments .**
  - **Ensure the Industry Laminate Suppliers have the capability and capacity to support the industry HF laminate requirements**

PCB Materials Development Input

Expectations of Consortia Membership:

- Joint evaluation and analysis of Laminate Properties and definition of Technology Envelope. Including:
  - Setting Max-Min Values
  - Test Methodology/Characterization
  - Reliability and Product Performance Validation
- Laminate Supplier will support/build according to the Technology Envelope/Guidelines
- OEM/ODM will build with the Laminates that meet this Guidelines/Technology Envelope

PCB Materials Development Input

1. **Define Initial Technology Envelope**
   - List material properties that need a modified range of values
   - List new material properties that do not appear on Suppliers datasheets

2. **Correlate known defects/performance degradation to Laminate Material Properties**
   - Provide defect examples that we want to improve
   - Provide Hypothesis for correlation of Defect to Material Properties
   - Build a test suite to validate correlation
   - Deliver the "Defect to Material Property" correlation

PCB Materials Development Input

3. **Define Metrologies & Methods to assess these Material Properties at Laminate Supplier**
   - Review existing test methods from all Industries
   - Develop new test methods if needed
   - Deliver Test Methods to Consortia and Industry

4. **Build TV and Products to verify PCB Reliability, SJR and Assembly Yields of Laminates within Tech Envelope**
   - Identify and build vehicles to quantify the reliability of the laminates within this test envelope
   - Deliver the Technology Envelope to Industry

5. **Work with Supply Chain to verify Capacity of Laminate**

PCB Materials Development Input

Proposed Technology Envelope Properties

Material Property or Performance Metric	Impact of Property	Value/Range
Permittivity (Dk or Er)	Impacts impedance modeling and cross talk. Variation impacts electrical performance. Nominal property affects design rules and material selection.	Targeting a tighter range within the present FR-4 Spec (3.6 -4.0)
Moisture Absorption	Impacts Dk and Df stability, delamination, isolation resistance. Diffusivity rate impacts moisture test results and final value recorded.	Lower is better
Flexural Strength	Modify test method for applicable data. Used for mechanical modeling simulation.	Higher flex Modulus/Stiffer laminates have shown less warpage and better assembly capabilities, but are more brittle and prone to Thermo Mechanical failures
Flammability	UL certification testing. Need to evaluate UL rating requirements.	Lower rating could allow more flexibility in formulations and other material properties
Young's Modulus	Determine temperature dependent flexibility of the material modeling input	No spec, some laminators are giving this data but not all. Need to determine if Flex Modulus or Stiffness would be better or sufficient.
Thermal Resistance (T260, T288)	Impacts laminate integrity, especially delamination	No spec or target value Higher is better
Fracture Toughness	Understand material property for pad crater mechanical modeling	No spec, not recorded on most laminator data sheets. No correlation to defects at this time. Should relate to Themo Mechanical performance.

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PCB Materials Development Input

Proposed Technology Envelope Properties, continued

OK for now, No degradation	Impact of Property	Value/Range
Loss Tangent (Df)	Impacts HSIO margin. Maximum property affects system design rules (such as bus lengths) and material selection. Variation impacts performance.	Lower is better
CTE (Alpha 1, Alpha 2, %)	Impacts Via reliability and laminate integrity	Lower is better, but present values OK. HF materials appear to have lower CTE (X,Y & Z)
Decomposition Temperature (Td)	Used to understand material weight loss at temperature levels. Unsure of correlation to defects at this time	No spec

Other Areas of Interest	Impact of Property	Value/Range
Filler % and Particle size	Affects many properties (CTE, toughness, flexural, etc.)	No spec
Thermal Conductivity	Could effect SJR or reliability	

Test Methods	Impact of Test	Testing Level
Cold Ball Pull	Pad Crater/Cracking performance indicator/comparison	System or Bare Board Level
Shock	Product performance test for comparison	System Level
Vibe	Product performance test for comparison	System Level
Temp Cycle	Product performance test for comparison. MEB examines only the bare board performance	Bare PCB Level
IST/HATS	Understand via reliability and material integrity performance test	Bare PCB Level
Isolation and Moisture Resistance	Understand material integrity and board level reliability	Bare PCB Level

iNEMI BFR-Free High Reliability PCB Project
Proposed Project Schedule

Project Execution SI

• Phase 1 (Identification of Electrical Envelope)	Jun'09
• Phase 2 (Characterization)	Dec'09
• Phase 3 (Validation)	Jun'10
• Release Results	Jul'10

Project Execution PCB

• Phase 1 (Define Initial Envelope)	Jun'09
• Phase 2 (Correlate Defects)	Oct'09
• Phase 3 (Define Metrologies / Methods)	Oct'09
• Phase 4 (Build TVs / Verify Reliability)	May'10
• Phase 5 (Verify Supply Capability)	Jul'10

iNEMI HFR-Free PCB Technology Envelope Project

Team Structure

Project Chair – S. Tisdale (Intel) Project Co-Chair - TBD					
Signal Integrity WG – S. Hall (Intel)			PCB Material Development WG – J. Davignon (Intel)		
Name	Email	Phone	Name	Email	Phone

iNEMI

Email contacts:

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Bob Pfahl

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BACKUP

Ensuring Halide Free PCB's Do Not Cause Signal Integrity Problems

Jan 12, 2009

Electrical Problem with HF designs

- The available permittivity range for halogen free dielectrics is too wide for a single design
  - **Standard 1080 FR4 → $3.6 \le \varepsilon_r \le 3.9$**
  - **HF FR4 → $3.6 \le \varepsilon_r \le 5.2$ (requires ~2-3 separate designs)**
- High permittivity increases crosstalk, risk & cost
  - **DDR3 & PCIe3 are already high risk & crosstalk limited**

    → <u>more crosstalk = more risk</u>
  - **High permittivity leads to more cost**
    - **more layers, pool, better via technology … etc. to reduce crosstalk**

    → <u>more layers & better vias = more cost</u>
  - **Initial data indicates "*area-neutral*" layout "tweaks" are ineffective for crosstalk reduction** (Not fully explored yet)
- If the dielectric properties of the boards change significantly, then industry specs such as PCIe would need to be revisited

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Plan

Define an "*electrical envelope*" for HF dielectrics to ensure ...

1. **signal integrity does not roadblock the PCB halogen free transition in 2011**
2. **drop in compatibility with 1080 FR4**
   - **Eliminates need for two sets of design guides (HF & FR4)**
   - **Ensures industry specs (e.g., PCIe) remain valid**

   Note: HF electrical properties do not need to overlap 100% with FR4 ... needs to be close enough
3. **the industry has the ingredients needed to design halide free systems in 2011 timeframe**

SI Strategy

- Identify, bound & validate the key electrical parameters of the HF dielectric needed to ensure electrical performance on par with 1080 FR4

Target plan: **Assume that FR4 & HF guidelines are identical and define HF envelope appropriately**

Fallback 1: **Examine layout "tweaks" to guarantee HF and FR4 design compatibility**

Fallback 2: **Separate HF and FR4 designs**

1. Dielectric electrical characterization
   - **Test the available dielectric materials to determine critical electrical properties (e.g., ε_r, tanδ, frequency dependence, moisture absorption)**
   - **Determine common characterization methods**
2. Simulation
   - **Define & test the "dielectric electrical envelope" required for a drop in FR4 replacement (based on DDR3 and PCIe2,3 links)**
3. Validation Platforms
   1. **Re-spin previously validated stable systems with HF materials at the corners of the "dielectric electrical envelope"**
   2. **Validate the trends observed in simulation**

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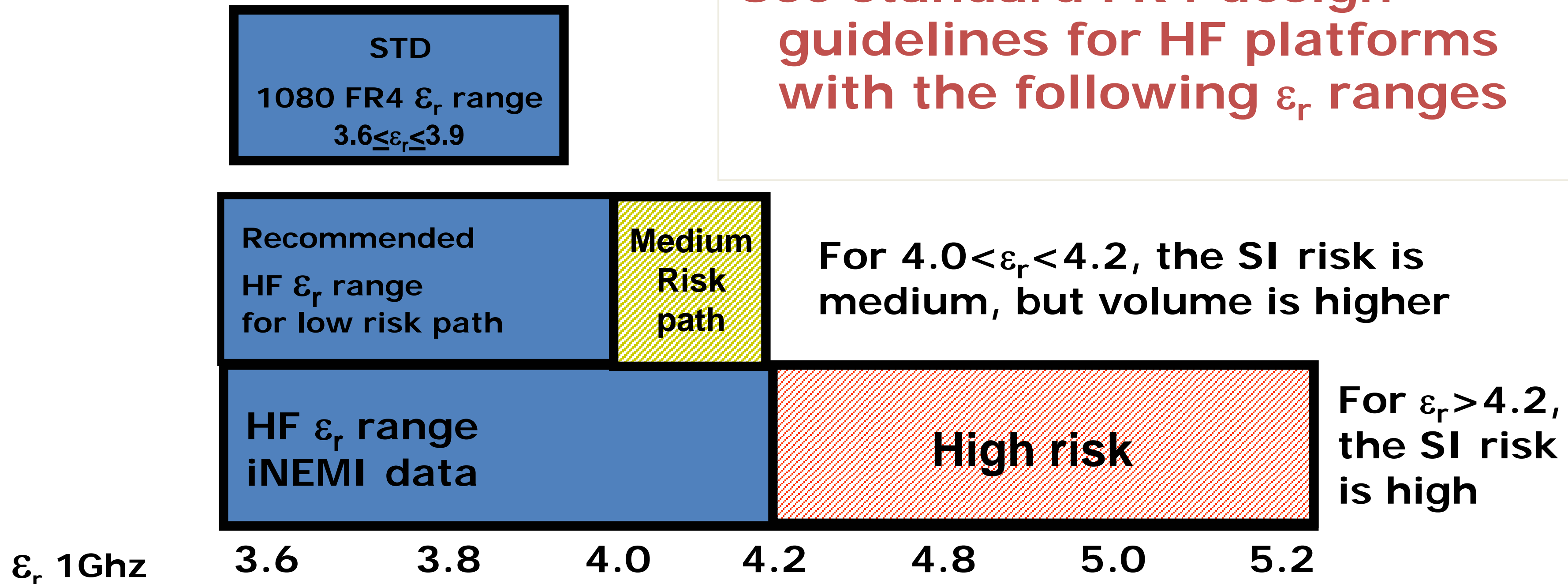
Preliminary recommendation for HF Permittivity Ranges



Target HF materials with a permittivity of **$3.6 \leq \varepsilon_r \leq 4.0$**

Allows a single design for HF & FR4 AND mitigates crosstalk

If volume requires additional material sets, **$3.6 \leq \varepsilon_r \leq 4.2$** can be considered

Materials also need to pass Thermo/Mechanical criteria and pass rel. tests

Notes:
1. The variation around the nominal values is assumed to be ~ +/-0.15
2. All values are considered to be nominal
3. Assume loss tangent similar or better than FR4

Help Needed

- Comparative data validating the HF electrical envelope corners
  - Tangible (non-simulated) data is needed to ensure nothing was missed
  - Apples / Apples comparison of DDR & PCIe margins (HF vs. FR4)
- Consensus/input on the variables and ranges in the electrical envelope
- Consensus on dielectric property measurement methods

Summary

- Initial recommendation is to target HF materials with a permittivity of $3.6 \leq \varepsilon_r \leq 4.0$
  - If volume requires additional material sets, $3.6 \leq \varepsilon_r \leq 4.2$ can be considered
- Intel's final "*electrical dielectric envelope*" for HF board materials will be completed WW36 of 2009
  - Drop in for FR4
  - Compatible for high speed buses (validated on DDR & PCIe)

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PCB Materials HF WG Strategy

WG Mission Statement

- PCB Technology Envelope WG
  - **Define a technology envelop for a set of FR-4 electrically equivalent HF PCB materials, technology parameters and test conditions which meets the quality and reliability requirements for all relevant market segments .**
  - **Ensure the Industry Laminate Suppliers have the capability and capacity to support industry requirements**

HF PCB Fabrication Status

- Most higher end PCB suppliers offer halogen free material and have optimized their processes to produce quality boards.
- HF material processes different than FR4 at the PCB fabricator. Experience with the material is needed to assure quality results.
  - Press parameters adjusted for optimum cure and resin flow.
  - Drilling impacted by the addition of fillers which increases wear on drill bits and reduces maximum hit count and resharps.
  - Desmear increased at plating to insure quality interconnects.

- Lower Technology suppliers are trailing industry in Halogen free fabrication capability.
  - Many have not built with Halogen free material
  - Some that have tested halogen free material do not yet have UL certification

PCB Supplier Readiness will be the responsibility of the OEM/ODM

MARKET AND GROWTH OF RIGID LAMINATE

Area (Mm²)	2006	2007	2012	Value CAAGR ('07-'12)
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Mobile Phone		7.5	21.4	23.4%
Other (Server, consumer)		7.7	20.5	21.6%

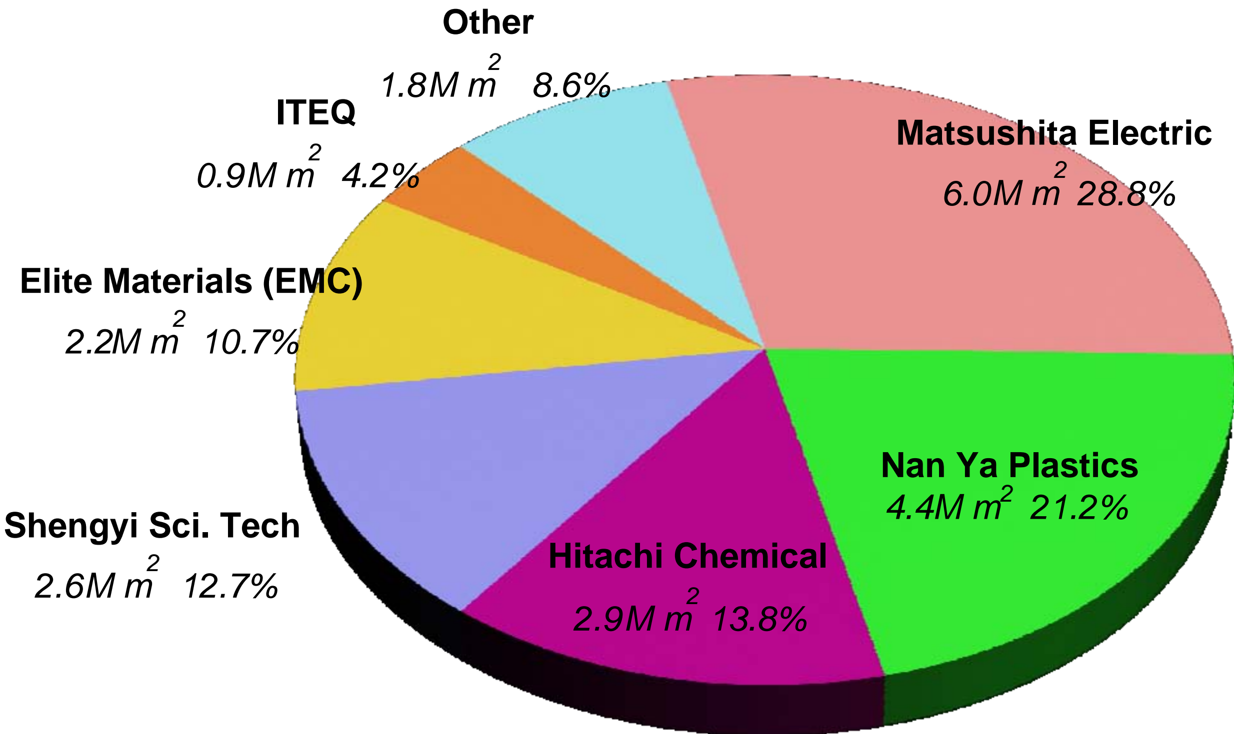
If HF supplants standard FR4, CAAGR grows to almost 70%

(assuming HF FR4 reaches FR4 volumes for '12)

FR-4 HALOGEN-FREE MARKET

AREA

2007



ls38.032kk-halogen free

TOTAL LAMINATE: 20.9M m^2

Ack: Nanya Laminate Division

HF materials sets

Supplier	Material ID	Tg	Dk	Df	Vendor Status	UL Testing		Laminate Availability
		Literature Value	Literature	Literature Value		Sample	Approval	
Doosan	DS-7402	150	4.4	0.015	?			
	DS-7402H	170	4.5	0.014	Available		Rev July 2007	
	DS-7402D	160	3.9	0.01	R&D	est Q1'09	Est Q1'10	Not available to PCB fab
EMC	EM-285	152℃ (TMA)	4.5	0.011	Industry Leader			
	EM-370 (5)	152℃ (DSC)	4.5	0.013	Available			
	EM-370	175℃ (DSC)	4.5	0.012	Available			
Hitachi	LLZ-71G	175oC (TMA)	3.6	0.0055-0.007	Available	Dec-05	Rev Nov 2007	Very low volume-RF 2yrs
	BE67G H	140-150 (TMA)	4.8-5.0 (@1MHz)	0.007	Industry Leader			
	BE67G R	155	4.5-4.7	0.009-0.011	Available			
	HE-679G	185oC (TMA)	3.9	0.0085-0.0095	Development	Apr-08	est Feb 2009	Qual samples only
ITEQ	IT175-GD	170	3.8	0.008	R&D	TBD	TBD	Not available
	IT140G	155	4.5 (@1MHz)	0.015	Industry Leader			
	IT170-GR	175	4.5 (@1MHz)	0.009	Available		Rev Oct 2007	Available
	IT155-G	160	4.6 (@1MHz)	0.009	Available		Rev Feb 2008	Available
Nan Ya	NPGN150	143 (TMA)	3.8~4.0	0.012~0.013	Available		Rev July 2008	Available
	NPGN170	162 (TMA)	3.9~4.1	0.012~0.013	Available		Rev July 2008	Available
	NPG-150	150	3.8~4.0	0.012~0.014	Industry Leader			
	NPG-170	170	4.1	0.012~0.014	Available			
	NPG180	176 (TMA)	4.2~4.5	0.013~0.015	Development	TBD	TBD	Not available
Panasonic	R1566	148	4.8	0.01	Industry Leader			
Park-Nelco	N4000-7EF	150 (DSC)	3.9-4.1	0.013-0.016	Available	Aug-05	Rev Jan 2008	Available
Shengyi	S1155	135	4.7 (@1MHz)	0.01	Industry Leader			
	S1165	165	5.4 (@1MHz)	0.035	Available			
TUC	XX872 HF	185 (TMA)	3.8	0.008	R&D	est Q1'09	TBD	Internal TUC pilot run only
	TU-752	140 (TMA)	4.3	0.013	Available			
	TU-862	170	4.1	0.010-0.011	Development		Rev Oct 2008	Available

Color Code	Dk<4.0@1GHz
Industry Leader: Makes ups 80% of Industry HF Laminate	

HF Laminate Scorecard

Material	Scorecard															
	Dk	Df	Moisture Absorption	Tg	CTE	Flexure	Td	T260 /Cu	T288 /Cu	Peel Strength	IST	CAF	UL94V0	Shock	Vibe	Temp Cycle
L	Red	Green	Yellow	Yellow	Green	Red					Green	Green		Red	Red	Yellow
B	Red	Green	Yellow	Yellow	Green	Red	Green	Green	Yellow	Green	Green	Green	Green			
C	Yellow	Green	Yellow	Yellow	Green	Red	Green	Green	Green	Green	Green	Green	Green	Red		
D	Yellow	Green	Yellow	Yellow	Green	Red	Green	Green	Green	Green	Green	Green	Green			
E	Yellow	Green	Yellow	Yellow	Green	Red	Green	Green	Yellow	Yellow	Green	Green	Green			
F	Red	Green	Yellow	Yellow	Green	Red	Green	Green	Yellow	Green	Green	Green	Green			
G	Red	Green	Yellow	Yellow	Green	Red	Green	Green	Yellow	Green	Green	Green	Green	Red	Red	Yellow
H	Red	Green	Yellow	Yellow	Green	Red	Green	Green	Yellow	Yellow	Green	Green	Green			
I	Red	Green	Yellow	Yellow	Green	Red	Green	Green	Green	Green	Green	Green	Green			
J	Red	Green	Yellow	Yellow	Green	Red	Green	Green	Yellow	Green	Green	Green	Green			
K	Yellow	Green	Yellow	Yellow	Green	Red	Green	Green	Green	Green	Green	Green	Green			

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Color Code
- Green: Equal to or better than FR4 (No issue)
- Yellow: Marginal vs FR4 (Issue not clear)
- Red: Worse than FR4 (Clear Issue)
- Black: No Data

Key Message: Laminate Properties will not meet requirements without significant intervention

Technology Envelop (new values)

	New Value or Test Proposal			
	Property	Value		Unit
		Maximum	Minimum	
	Modified Value Range of STD Test			
1	Permittivity (Dk or Er), maximum			
	@ 1MHz			
	@ 1GHz			
	Scan range 1-20 GHz			
2	Loss Tangent (Df), maximum			
	@ 1MHz			
	@ 1GHz			
	Scan range 1-20 GHz			
3	Moisture Absorption, maximum		NA	
4	Flexural Strength, minimum	NA		
	Length direction			
	Cross direction			
5	Flammability			
6	Decomposition Temperature (Td)			
7	Z-Axis CTE			
	Alpha 1			
	Alpha 2			
	50-260C			
8	Young's Modulus			
9	Thermal Resistance			
	T260			
	T288			

Data Collection and Analysis

– Validate electrical and mechanical properties (MEB/Product)
  - **Loss tangent and Dk modeling over required range of signal speed**
  - **Signal Integrity Capability / Validation (DDR2, DDR3 etc)**
  - **Mechanical performance validation for lead free assembly and rework**
  - **Critical Test Parameter Evaluation (CAF, IST, flex modulus, etc.)**

– Validate Board Level Reliability Capability (ETB/STB/MTB)
  - **PCB Modulus / Thickness Impact on Mechanical Capability**
  - **HF Board Level Assembly / Rework Process Characterization**
  - **Mechanical Characteristics (Pad Crater / Ball Pull etc)**
  - **CTE Characteristics**
  - **SJR (Shock / TC etc)**
  - **HF Component / HF PCB Interaction**

– Provide Industry with a Recommended Design Guideline for BFR-free PCB Materials

Help Needed – PCB Materials Dev

- Joint evaluation and analysis of Laminate Properties and definition of Technology Envelope. Including:
  - Setting Max-Min Values
  - Test Methodology/Characterization
- Laminator Support to build Laminate to the Technology Envelope/Guidelines
- OEMs to Build with the Laminate that meets these Guidelines/Technology Envelope

iNEMI BFR-Free High Reliability PCB Project

Test Vehicle	Test Category	Test	Test Method	Pre-Stress Reflow Temperatures
MEB II (16.5" x 22.5") 1 electrical quadrant 2 mechanical quadrants 1 mechanical / assembly quadrant	**Mechanical / Reliability**	**IST**	**IPC TM650 2.6.26 @ 150C**	
		CAF	**IPC TM650 2.6.25**	
		Flexural Modulus	**ASTM D790**	
		Cu Peel Strength	**IPC TM650 2.4.8C**	
		Tg / z-Axis CTE	**IPC TM650 2.4.24C**	
		Solder Mask Adhesion	**TM650 2.4.28B**	
		Insulation resistance	**TM650 2.5.7**	
		Solder Float / Cross Section	TM650 2.6.8E	
		Microhardness	Future Tech Microhardness	
	Electrical	**Permittivity (Dk) and Loss Tangent (Df) up to 30GHz**	**VNA**	
		Moisture Diffusivity Impacts on Insertion Loss	**VNA**	
		Capacitance	TM650 2.5.2A	
		CAT Trace and Space	Portable CAT Tester	
		Drill Registration	Intel Hand Probe	
	Assembly	Temp Cycle (HATS)	HATS	
		Transient Bend	Instron	
		Rework		
		Board Side Ball Pull	Dage 4000	

Note : Materials Must be LF Process Capable

iNEMI BFR-free High Reliability PCB Project Tasks

Phase 1 Tasks	Team Leader	Company Support	Key Contact
Identify Candidate Materials			
Material Suppliers			
Identify Key Performance Characteristics			
Test Vehicle Identification			
• Provide Component Test Vehicle			
• Provide PCB Test Vehicle			
• Provide TV / PCB Design Service			
Provide PCB Assembly Capability			

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iNEMI BFR-free High Reliability PCB Project Tasks

Phase 2 Tasks	Team Leader	Company Support	Key Contact
Develop Test Plan / Schedule			
Procure Components & PCBs			
TEST Plan / Schedule			
IST			
CAF			
Flexural Modulus			
Cu Peel Strength			
Tg / z-Axis CTE			
Solder Mask Adhesion			
Insulation resistance			
Solder Float / Cross Section			
Microhardness			
Permittivity (Dk) and Loss Tangent (Df) up to 30GHz			
Moisture Diffusivity Impacts on Insertion Loss			
Capacitance			
CAT Trace and Space			
Drill Registration			
Temp Cycle (HATS)			
Transient Bend			
Rework			
Board Side Ball Pull			
TCT			
Mechanical shock			
Monotonic bending			
FA			

iNEMI BFR-free High Reliability PCB Project Tasks

Phase 3 Tasks	Team Leader	Company Support	Key Contact
Write Project Team Report			
Executive Summary			
Introduction			
Purpose of the Project			
Materials & Methods			
Results			
Conclusions			
Analysis of Success			
Write Generic iNEMI Report			
Write External Paper			

iNEMI®

International Electronics Manufacturing Initiative

Next Steps

Bob Pfahl, iNEMI
January 20, 2009

Advancing manufacturing technology

Outline of Next Steps

- **Brief Introduction of what iNEMI brings to the table**
- **Identify key players in the Supply Chain**
- **Identify how to engage them**
- **Proposal for face to face kick off meeting on February 18**
- **Discussion of Next Steps**

Profile of Successful Projects

The “sweet spot” of iNEMI projects:

- **Addresses knowledge gap of industry**
  - Common problem
  - Best solved by working together
  - Often a pre-cursor to standards development
- **Brings together a segment of supply chain to provide industry-wide response**
  - OEMs
  - ODM/EMS providers
  - Materials, equipment, software, and/or component suppliers
- **Direct alignment with member companies’ commercial interests.**

iNEMI's HFR-Free Activities

- Projects
  - BFR-Free PCB Project
  - BFR-Free High Reliability PCB Project
- Initiatives
  - iNEMI PVC Alternative Initiative
- Proposed Initiatives
  - HFR-Free Connectors

iNEMI Project Facilitation

- **Staff Members to guide development of Statements of Work (SOW) Project Statement (PS), and to monitor Project performance.**
- **Board of Directors and Technical Committee to aid projects in obtaining support from firms.**
- **Projects executed under the provisions of the National Cooperative Research and Production Act of 1993.**
- **Projects conducted under the iNEMI Intellectual Property Policy.**
- **Guidance provided on anti-trust policy and export compliance protocols.**

iNEMI Membership Information

- iNEMI is a 501 (c) (6) not for profit corporation made up of electronic equipment manufacturers, their suppliers, other consortia/associations, government agencies, and universities.
- Detailed Membership Information is available on our web site: http://www.inemi.org/cms/join/
- Jim McElroy (CEO) is available to discuss membership: jmcelroy@inemi.org

Key Players: OEMs by Sector

- Mobile Phones (Significant Conversion):
  - Nokia, LG, Samsung, Motorola
- PCs (Leaders Converting Now):
  - Acer, Asus, Apple, Dell, HP, Intel, Lenovo, Sony, Toshiba, Hitachi, Inspur, Sharp
- Add-in Cards (Will need to convert as PC's convert)

- Servers and Beyond (Many are evaluating):
  - Dell, HP, IBM, Intel, Sun, Supermicro, Cray, Bull, Unisys
- Netcom (Watching Developments):
  - Cisco, Alcatel Lucent, Nokia-Siemens, Huawei
- Military (Could care less)
  - Lockheed Martin, Boeing

Key Players: ODM/EMS

- **Foxconn, Inventec, Pegatron, Quanta, Wistron, Compal, ECS, Gigabyte, Kontron, MSI, Mitac, Radisys, Celestica, Flextronics, Jabil, Sanmina-SCI**

Key Players: PCB Manufacturers

- Foxconn/Pan Pacific, Ibiden, NanYa, Catac, E&E, Ellington, Gold Circuits, Hannstar, Tripod, WUS, APCB, Asus/ Boardtech, AT&S, Broadtech, Compec, EIT, Sanmina-SCI, Global Brand Manufacturing, Meadville, Multek, Shining Bridge/Golden Elite, Unimicron, Via System, Yufo

Key Players: Laminators

- **Doosan, EMC, Hitachi Chemical, ITEQ, ShengYi, Grace, ISOLA, Kingboard, NanYa Plastics, Panasonic/Matsushita, Park Nelco, TUC, Ventec, Elite**

How to Engage Key Players

- Top Down
- By Sector
- By Market Share
- Individual Contact

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International Electronics Manufacturing Initiative

Next Steps: Discussion

Advancing manufacturing technology

Next Meeting

- **Face to Face**
- **February 18, 2009**
- **Location: Cupertino, CA**
- **Time: 8:30 AM-Noon**

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