

Ensuring Halide Free PCB's do not Cause Signal Integrity Problems

iNEMI HF Signal Integrity WG Kickoff

02-18-2009



Agenda

- Proposed directive
- Problem
- Plan of attack
- The electrical envelope
- WG requirements

Proposed Directive

HF Consortium:

- Begin delivering halogen free product lines
 - Gain industry consensus on a transition strategy
 - Gain agreement from the big players of a HF “standard” to ensure adequate performance for high speed designs
 - Use the “standard” to communicate requirements to material vendors to help increase volume and reduce cost

SI Work Group

- Goal: Keep signal integrity out of the critical path for the halogen free transition
- Strategic Challenge: Define and gain industry consensus on the electrical requirements of HF dielectrics ensuring suitability for high-speed digital designs

Electrical Problem with HF designs

- The available permittivity range for halogen free dielectrics is too wide for a single design
 - Standard 1080 FR4 $\rightarrow 3.6 \leq \epsilon_r \leq 3.9$
 - HF FR4 $\rightarrow 3.6 \leq \epsilon_r \leq 5.2$ (requires ~2-3 separate designs)
- High permittivity increases crosstalk, risk & cost
 - DDR3 & PCIe3 are the focus
 - \rightarrow more crosstalk = more risk
 - High permittivity leads to more cost
 - more layers, pool, better via technology ... etc. to reduce crosstalk
 - \rightarrow more layers & better vias = more cost
 - Initial data indicates "area-neutral" layout "tweaks" are ineffective for crosstalk reduction (Not fully explored yet)
- If the dielectric properties of the boards change significantly, then industry specs such as PCIe may need to be revisited

Plan of Attack

- Identify, bound & validate the key electrical parameters of the HF dielectric needed to ensure equal or better performance with 1080 FR4

Target plan: Assume that FR4 & HF guidelines are identical and define HF envelope appropriately

Fallback 1: Examine layout “tweaks” to guarantee HF and FR4 design compatibility

Fallback 2: Separate HF and FR4 designs

3-tier approach

1. Simulation

- Define, test and publish an “dielectric electrical envelope” required for a drop in FR4 replacement (based on DDR3 and PCIe2,3 links)
 - $\tan\delta$, ϵ_r , freq. dependence, moisture absorption ... others?

2. Dielectric electrical characterization

- Test available dielectric materials to identify an existing set that falls within the envelope
- Determine common characterization methods

3. Validation Platforms

1. Re-spin previously validated stable systems with HF materials at the corners of the “dielectric electrical envelope”
2. Validate the trends observed in simulation

Requirements

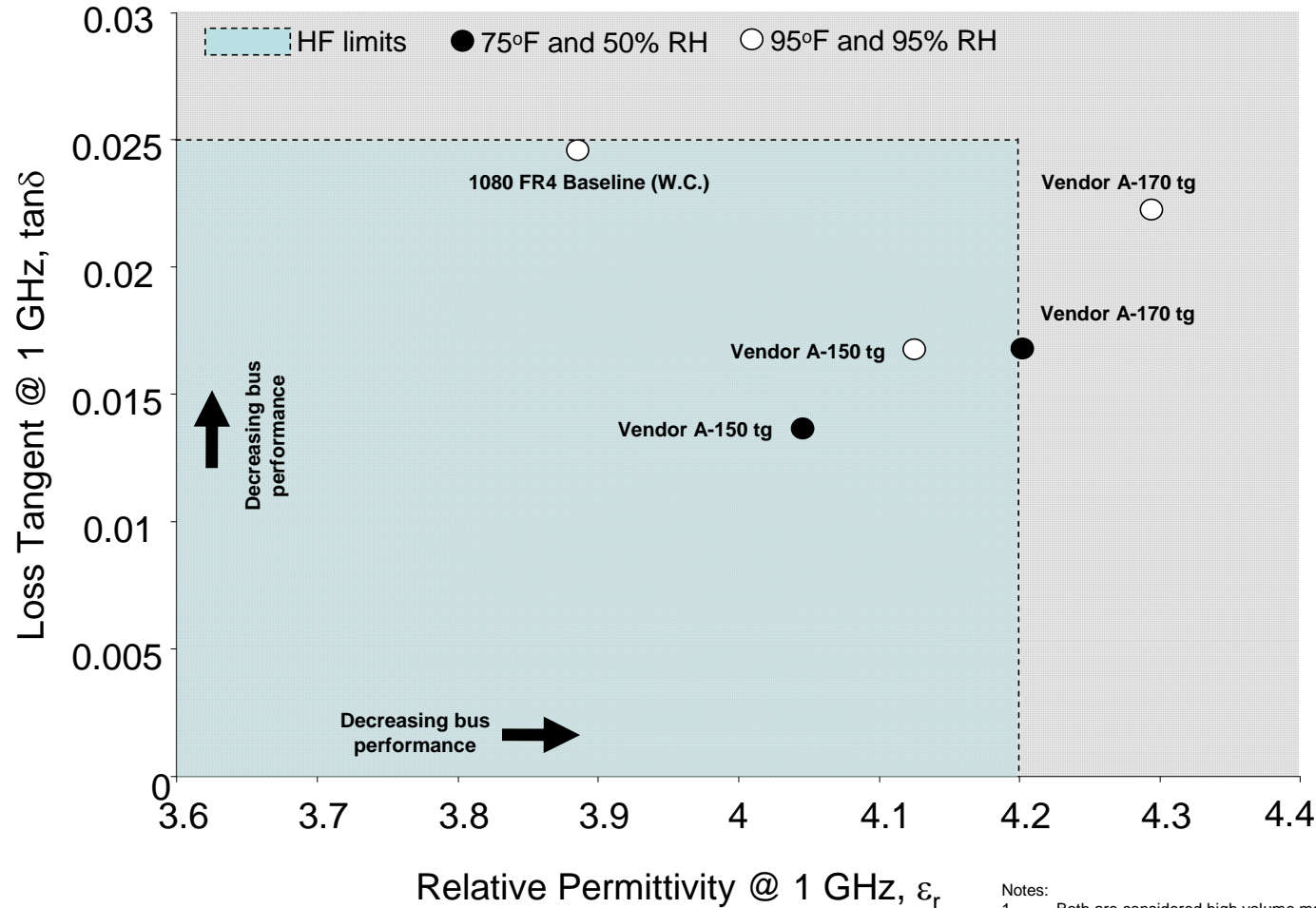
The "*electrical envelope*" for HF dielectrics must ensure ...

1. Signal integrity does not roadblock the PCB halogen free transition
 - The dielectric performance must equal to or be better than FR4
 - The electrical properties must be adequate for all buses
2. Drop in compatibility with 1080 FR4 (and possibly 2116)
 - Eliminates need for two sets of design guides (HF & FR4)
 - Ensures industry specs (e.g., PCIe) remain valid

Note: HF electrical properties do not need to overlap 100% with FR4 ... needs to be close enough
3. The material suppliers have the industry requirements needed to design high volume halide free systems

Current status of the envelope

Rev. 0.0 Halogen Free dielectric electrical envelope with 1-2 plies of 1080 glass
(comparison of materials tested to the rev. 0.0 envelope)



Notes:
1. Both are considered high volume materials
2. Nominal permittivity assumed

- Need to comprehend frequency variations
- Must come to consensus on envelope
- Populate current materials as characterized
- May need to track 2116 construction

Envelope includes $\tan\delta$, ϵ_r & moisture absorption

What's needed from WG members - Discussion

- Simulation analysis of envelope to provide data driven consensus on the absolute limits – What is the difference compared to standard FR4?
 - The rev. 0.0 envelope is a good starting point ... can we widen it? Does it need to be further restricted?
 - Suggest DDR3,4 and PCIe2,3 be the test cases
- Agreement on common stackups for FR4 and HF boards to ensure we are comparing apples to apples
- Tangible non-simulated data from real platforms showing the difference in bus margin as a function of material properties, with FR4 as the baseline
- Electrical characterization of the dielectrics your company is planning to use to design HF platforms
 - Must 1st agree on common characterization methods and metrics

Next steps - Discussion

- **Step 1: Timeline (End Date ~ Q3'10)**
 - Envelope needs to be finalized, agreed upon & communicated to material suppliers to ensure adequate lead time for new products
 - Subteam to propose timeline by WW11
- **Step 2: Material Characterization (~Q4'09)**
 - Need commitments to characterize materials
 - Must agree on common measurement technique
 - Subteam to commit to characterize current / new HF materials
- **Step 3: Simulations to identify/refine envelope (~Q1'10)**
 - Need volunteers & commitment dates
 - Specifically, bus margins of HF materials compared to FR4 baseline
 - Need to refine current envelope
 - Subteam to commit to provide PCIe2, 3 & DDR3 simulation data points
- **Step 4: Real system validation data (~Q2'10)**
 - Need commitments to deliver tangible data from real systems showing HF margin deltas against FR4 baseline for DDR and PCIe buses
 - Subteam to commit to deliver data points for various materials

Need commitments and dates so timeline can be constructed