

**iNEMI Statement of Work (SOW)
Environmentally Conscious Electronics TIG
iNEMI HFR-Free Technology Leadership Program**

Version 5.0

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Purpose:

Identify key electrical and mechanical HFR-free PCB material characteristics to material suppliers and identify a proposed set of technology guidelines. Identify supply chain readiness, supply capability and material parameter characteristics for “HFR-free” alternatives to conventional printed wiring board materials and printed wiring board assemblies.

Background and Motivation:

The European Union’s Restriction on the use of certain Hazardous Substances (RoHS) Directive prohibits the use of polybrominated biphenyls (PBBs) and polybrominated diphenyl ethers (PBDEs) in nonexempt electronic equipment. These compounds, used as flame-retardants, have been shown to present unacceptable risks to human health and the environment. Although PBBs and PBDEs are typically not used in circuit board materials, stakeholders are beginning to urge the electronics industry to take a precautionary stance on the use of other non-regulated halogenated organic substances, such as brominated epoxies for circuit board applications.

For this reason, many companies have set their own specific transition dates to move to HFR-free technology. This has, however, created some confusion in the supply chain since these dates vary by company. To alleviate this, the goal of this project is to identify the feasibility of the supply chain to support OEM / ODM / EMS / Supplier to smoothly transition to these new materials.

Goals of the Program:

1. Define the electrical signaling and PCB material property requirements as well as the associated test conditions that deliver the data required to make design and supply chain readiness decisions.
2. Define the material set parameters and test conditions for all relevant market segments.
3. Leveraging prior investigations, carry out the necessary testing of available materials from participating companies.
4. Analyze results.
5. Publish a set of material guidelines for use by industry that meets all market segment requirements – signaling, mechanical, quality / reliability, SMT yield, and environmental. This may require design tradeoffs and/or material property changes to resolve marginal parameters.
6. Drive test conditions and material properties into supplier data sheets. This may entail engaging IPC to revise existing industry standards.

Is / Is Not:

This Program <u>IS</u>:	This Program <u>IS NOT</u>:
A technical evaluation of key electrical and mechanical properties of HFR-free materials	An EHS assessment
Focused on those design attributes which are of most value to the broader industry	Biased towards specific laminate suppliers, geographies, or market segments
Building on learning from prior investigations	A repeat of prior work
Focused on circuit board materials characteristics and test methodology, along with Board / Component Interaction	Focused only on materials characterization
Focused on generating data and design guidelines for development of an industry standard	

Scope of Work:

Phase I: Design

Review prior work and make recommendations for testing needed. Investigation should take into account needs of electronic product sectors represented by iNEMI membership.

1. Identify candidate materials for evaluation

Poll the supplier base, keying in on candidate materials for market segment applications.

- Identify candidate HFR-free laminate materials to allow interchangeability for standard halogenated materials

2. Identify key performance characteristics and test criteria

Assess prior studies and identify critical knowledge gaps or technical issues. Make recommendations for performance tests needed. Review results of prior industry and member company investigations.

- Electrical
 - i. Output broadband frequency dependent dielectric constant (Dk) and loss tangent (Df) of candidate halogen-free laminate materials (10KHz - 20GHz)
 - ii. Moisture absorption impact on Dk, Df
 - iii. Breakdown Voltage Analysis
 - iv. Simulate results of high speed buses DDR3, PCI2,3
- Thermo-Mechanical
 - i. Critical Margin Degradation Review
 - ii. Define and correlate test metrology to critical defects

3. Design minimal number of test vehicle(s) and test methodologies, leverage standards where possible

Specify test vehicle criteria required for performance testing. Agree on a minimal number of test vehicle designs and test requirements.

- Electrical

- Define Test Methodology & Metrology
- Define Test Vehicles
- Identify Third Party for Electrical Parameter Testing
- Gauge R&R
- Thermo-Mechanical
 - Define Test Metrologies
 - Perform Sensitivity Study on Metrology (Gauge R&R)
 - Define Test Coupons
 - Define Test Vehicle Construction

Phase II: Test / Validation

Develop, manage, and execute performance testing.

1. Develop evaluation plan and schedule

Outline key mechanical and electrical performance characteristics and resource and time constraints. Build systems with dielectric materials from participating suppliers that meet IPC/JEDEC proposed spec.

2. Procure parts and test vehicles

Obtain needed evaluation materials. Consider lead times needed to synch with evaluation schedule. Solicit participation from supply partners.

3. Assign teams to carry out completion of the testing in a standardized fashion

Each test should be carried out in a manner that produces meaningful results. Industry standards should be followed where applicable. Testing should be coordinated to allow correlation of results and sharing of test materials. Intention is to use supplier data with a sampling of test boards sent to a third party test house for verification.

4. Perform mechanical and reliability testing on test vehicles

Leverage capabilities and expertise of participating members and supply partners. Follow test procedures carefully and record positive and negative results.

5. Validation of results

OEM / ODM validation of predictability of materials tested.

6. Comprehend results and determine if modification to specific test methods may be required

Phase III: Results

Compile results, assess significance, make recommendations, and publish report.

1. Assess technology readiness / identify gaps

Flag unexplored issues and identify technical risks that need to be resolved before materials can be widely adopted. Make recommendations for future work.

- Electrical Parameters Rolled into Final Recommendation from Thermo-Mechanical Team

2. Assess manufacturing capability and supply capacity

Work with suppliers and EMS's to identify barriers to supply chain viability. Interpret implications of performance testing in terms of manufacturing capability.

3. Publish results

Compile and edit concise summary of methods, meaningful results, and recommendations. Goal is to issue the final report to members by Y/E 2010 with public release by IPC/APEX 2011

- Test Suite Methodologies Identified and Documented
- Recommended Ranges for Critical Margin Parameters (Market Segment Guidelines)
- Publish Generic Transition Timing / Volume by Market Segment
- Incorporate Test Suite Methodology into Laminate Data Sheets

Anticipated Outcome:

- **Validate electrical and mechanical properties**
 - Loss tangent and Dk modeling over required range of signal speed, bus designs
 - Signal Integrity Capability / Validation (DDR2, DDR3, etc.)
 - Mechanical performance validation for lead free assembly and rework (delamination)
 - Critical Material Property and Test Parameter Evaluation (CAF, IST, flex, etc.)
- **Validate Board Level Reliability Capability**
 - HF Board Level Assembly / Rework Process Characterization
 - Mechanical Characteristics (Pad Crater / Ball Pull, etc.)
 - SJR (Shock / TC, etc.)
 - Material Property Validation
- **Initiate development of HF PCB Material Test Suites for critical parameter data generation which will be incorporated into Laminate Supplier Data Sheets**

Participant Profile:

iNEMI's member companies will encourage the participation of individuals from different disciplines and divisions within their organizations to contribute on the range of tasks outlined in the project plan. The group should include representatives of:

- OEMs
- ODMs
- Component and Board manufacturers
- Assembly EMS providers
- Dielectric material suppliers

Resources Required from Participants:

The HFR-Free Technology Leadership Program asks each participating company to commit to the following:

- 1) Provide at least one man-month or equivalent in-kind support (e.g. materials, test samples, equipment, etc.) annually.

- a) Agree to commit appropriate resources (possibly more than 1 man month) to meet accelerated project timeline and targeted end dates.
- 2) In the event project expenses are incurred, the costs will be shared among participants.
- 3) Agree that this consortium will provide technical support within its membership in sharing knowledge regarding PCB Defects / Margin Degradation / Test Metrologies / PCB Design / Design Rules and Fabrication for the duration of the program.
- 4) Provide Key Electrical / Mechanical parameter requirements by market segment to generate appropriate Stack Up Definitions and Test Plans.
- 5) Agree to provide materials, components, Test Vehicles, Design Capability, Modeling Capability, PCB Fabrication, PCB assembly, Test Capability, FA Capability as required by Test Plan.
- 6) Design and /or assemble test samples for evaluation, and/or carry out tests and evaluations as negotiated and agreed to, with other members of the projects, to fulfill the Statement of Work.
- 7) Collaborate on input to final report. Document results and publish findings to iNEMI members.
- 8) Provide Recommendations for Industry Standards to IPC / JEDEC to generate and publish an acceptable Industry Specification for HF Design Rules as necessary.
 - a) Commit to promote the adoption of any recommended standards, tools, or processes that are developed by this project internally within the participating company and its supply chain partners.

Program Formation Participants:

iNEMI HFR-Free Technology Leadership Program

First Name	Last Name	Company
Jones	Huang	Acer
Richard	Lai	Acer
Clifford	Bast	Acer
Michael	Cochran	Acer
Susan	Landry	Albemarle
T.J.	St. Romain	Albemarle
Amir	Salehi	Apple
Bill	Cornelius	Apple
Dennis	Pyper	Apple
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Ding	Chen	Celestica
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Ji	Xue	Cisco
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Todd	Myers	Cisco
Scott	Hinaga	Cisco
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Greg	Hsiao	Compal Electronics
May	Hsieh	Compal Electronics
Glide	Wu	Compal Electronics
Vincent	Kao	Compal Electronics
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Jason	Lin	Compeq Mfg.
Li-Cheng	Luo	Compeq Mfg.
Raj	Kumar	DDI
Darcy	Chu	Dell
Eric	Wang	Dell
Lit	Wu	Dell
Richard	Lin	Dell
Scott	O'Connell	Dell
David	Baranauskas	Dell
Larry	Legler	Dell
Nathan	Ramamurthy	Dell
Steven	Ethridge	Dell
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Ed	Tinsley	Dell
Maureen	Martinez	Dell
Wallace	Ables	Dell
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Simon	Lee	Dow Chemical Company
Robert	Hearn	Dow Chemical Company
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Ka Wai	Chan	Elec & Eltek
Li	Chou	Elite Material Co.
Li	Chou	EMC
Yih-Rern	Peng	EMC
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Kirk	Chen	Flextronics
Eva	Chen	Flextronics
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Bruce	Lee	Foxconn
Danny	Chen	Foxconn
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Scott	Lin	Foxconn
Sony	Teng	Foxconn
Thu	Nguyen	Foxconn
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Kenny	Su	Gemtek Technology
Yang	Chih-Ming	Gemtek Technology
Anderson	Cheng	Gold Circuit Electronics
David	Chen	Gold Circuit Electronics
MR	Lin	Gold Circuit Electronics
Michael	Griffin	Gold Circuit Electronics
Michael	Lin	Grace T.H.W.
Davis	Lai	HannStar Board
Frank	Yeh	HannStar Board
Lance	Tao	HannStar Board
Frank	Wang	HannStar Board
Helen	Holder	Hewlett-Packard
Rich	Barnett	Hewlett-Packard
Terry	Fischer	Hitachi Chemical
Sang	Liu	Huawei
Shun	Zhang	Huawei
Wen	Huang	Huawei
Dongdong	Wang	Ibiden
Bhyrav	Mutnury	IBM
Curtis	Grosskopf	IBM
Matt	Kelly	IBM
Timothy	Mann	IBM
Jeffrey	Cheng	ICL
Aubrey	Sparkman	Independent
Martin	Rausch	Intel
Connos	Tai	Intel
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Gary	Long	Intel
Jamie	Gillespie	Intel
John	Davignon	Intel
Kawa	Chang	Intel
Peter	Fenton	Intel
Satish	Parupalli	Intel
Stephen	Hall	Intel
Stephen	Tisdale	Intel
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Jimmy	Liou	Isola Group
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Chuang	Chia Hao	IST
Ck	Yu	IST
Graver	Chang	IST
Hsieh	Han-Kun	IST
Tina	Shao	IST
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Ray	Reu	ITRI
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Anthony	Corkell	Lenovo
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Glenn	Lorant	MIC Specialty Chemicals
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Ranny	Lo	Micro-Star International
Wang	Toy	MiTAC International
Kenichi	Mori	Mitsubishi Gas Chemical
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Eric	Hsu	NanYa PCB
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Li	Ya-Chun	Pegatron
Chun Yao	Chen	Pegatron
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York	Wang	Quanta Computer
Grace	Huang	Quanta Computer
Mila	Li	Quanta Computer
Chris	Yuan	Quanta Computer
Ian	Huang	Quanta Computer
Antony	Yao	Quanta Computer
Joyce	Kuo	Quanta Computer
Mike	Chang	Quanta Computer
Brian	Nelson	Sanmina-SCI
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Jian Wei	Cai	Shengyi Sci. Tech Co.
Jin Rong	Ye	Shengyi Sci. Tech Co.
Harry	Yang	Shengyi Sci. Tech Co.
Scarlet	Wang	Shengyi Sci. Tech Co.
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Jun	Ma	Sun
Karl	Sauter	Sun
George	Hsin	Taiwan Union Technology Corp (TUC)
Marvin	Cheng	Taiwan Union Technology Corp (TUC)
Raymond	Foo	Taiwan Union Technology Corp (TUC)
Vincent	Choi	Taiwan Union Technology Corp (TUC)
Wendy	Chi	Taiwan Union Technology Corp (TUC)
Yu-Ju	Liu	Taiwan Union Technology Corp (TUC)
Lee	Starr	Tech Circuits
Pearl	Chou	Techmax Technical
Jim	Lee	TI
Casanova	Hsieh	Tripod Technology
Jerry	Huang	Tripod Technology
Terry	Yang	Tripod Technology
Wilson	Yang	Tripod Technology
H	Shi	Tripod Technology
Sue	Li	TSRC Corp
Jason	Chen	TSRC Corp
Crystal	Vanderpan	UL
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De Cheng	Wang	Universal Scientific Industrial
Mosa	Lin	Universal Scientific Industrial

First Name	Last Name	Company
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Ander	Hsieh	Wistron
Feng Yuan	Chen	Wistron
Jimmy	Yang	Wistron
Jay	Huang	Wistron
Eddie	Mok	WUS Printed Circuit
Andrew	Bell	WUS Printed Circuit

Project Participant Commitment Matrix (combined tasks of Materials & SI Projects):

Phase I Tasks	Team Leader	Company Support	Key Contact
Identify Candidate Materials			
• Material Supplier			
Identify Key Performance Characteristics			
Test Vehicle Identification			
• Provide Component Test Vehicle			
• Provide PCB Test Vehicle			
• Provide TV / PCB Design Service			
• Provide PCB Assembly Capability			

Phase II Tasks	Team Leader	Company Support	Key Contact
Develop Test Plan / Schedule			
Procure Components & PCBs			
Test Plan / Schedule			
Priority Tier 1			
BMP	Dk & Df		
TMP	Delamination characteristics under mechanical or thermal stress conditions		
TMP	CAF resistance		
TMP	Long term life prediction, such as IST or thermal shock test		
AP	Lead Free Reflow Test		
BMP	Moisture absorption		
BMP	Coefficient of thermal expansion (z-axis and x-, y-axes)		
OC	UL Fire ratings (V0-V1)		

Phase II Tasks		Team Leader	Company Support	Key Contact
Priority Tier 2				
AP	Rework (Pad Peeling)			
TMP	Pad Cratering (brittle fracture)			
BMP	Decomposition temperature (Td)			
TMP	Copper Pad Adhesion (CBP/Hot Pin Pull/ Shear or Tensile)			
PM	PCB fabrication process, drill wear, lamination & desmear cycle			
TMP	Shock & Vibe and Drop test data			
Priority Tier 3				
BMP	Fracture Toughness of Resin / Resin Cohesive Strength			
BMP	Glass transition temperature (Tg)			
OC	MOT Maximum Operating Temperature			
TMP	Transient Bend			
TMP	Co-Planarity Warpage characteristics as a function of stack-up, layer thickness, and temperature			
OC	Affect of Fillers			
Priority Tier 4				
BMP	Flexural strength			
OC	Resin system dependency/hardening/curing agents			
TMP	Plastic and elastic deformation characteristics as function of stack-up, layer thickness, and temperature			
BMP	Micro and macro hardness			
BMP	Stiffness			
PM	Punchability / Scoring / Break-off Performance			
OC	Electrical Properties (UL CTI rating)			

- BMP Basic Materials Properties
 TMP Thermo Mechanical Performance
 PM Process / Manufacturing
 AP Assembly Process
 OC Other Concerns¹

Phase III Tasks		Team Leader	Company Support	Key Contact
Write Project Team Report				
	• Executive Summary			
• Introduction				
• Purpose of the Project				
• Materials & Methods				
• Results				
• Conclusions				
• Analysis of Success				
• Write Generic iNEMI Report				
• Write External Paper				

¹ Further prioritization of Tasks will be done during Phase I.

Task Schedule:

- Phase I (Design)
- Phase II (Test)
- Phase III (Results)

<u>Phase I</u>	Dec-2008	Jan-2009	Feb-2009	Mar-2009	Apr-2009	May-2009	June-2009	July-2009	Aug-2009	Sept-2009
Review prior work and make recommendations for testing needed	X	X	X	X	X	X	X	X		
Identify Key Performance Characteristics		X	X	X	X	X	X	X		
Test Vehicle Identification										
• Provide Component Test Vehicle						X	X	X		
• Provide PCB Test Vehicle						X	X	X		
• Provide TV / PCB Design Service						X	X	X		
• Provide PCB Assembly Capability						X	X	X		
Test Method Identification										
• Identify Test Methods							X	X		
• Separate Testing into Priority Tiers							X			
Prepare Detailed Phase II Plans										
• Timeline for Test Vehicle (TV) Design							X	X		
• Timeline for Test Vehicle (TV) Acquisition							X			
• Timeline for Development of Test Methods							X			
• Cost of Test Vehicles (if needed)							X			
- Components							X			
- PCB Materials TV							X			
- Signal Integrity TV							X			
- Design Services							X			
- PCB Assembly Services							X			
• Cost of Test Services (if needed)							X			
Formal Review of Phase II Plans										
								X		

Phase II	Jan-2009	Feb-2009	Mar-2009	Apr-2009	May-2009	Jun-2009	Jul-2009	Aug-2009	Sep-2009	Oct-2009
Develop, manage, and execute performance testing						X	X	X	X	X
Physical Design of Test Vehicles						X	X	X		
Acquire Test Vehicles and associated components						X	X	X		
Test Plan / Schedule										
Priority Tier 1										
Dk & Df										
Delamination characteristics under mechanical or thermal stress conditions										
CAF resistance										
Long term life prediction, such as IST or thermal shock test										
Lead Free Reflow Test										
Moisture absorption										
Coefficient of thermal expansion (z-axis and x-, y-axes)										
UL Fire ratings (V0-V1)										
Priority Tier 2										
Rework (Pad Peeling)										
Pad Cratering (brittle fracture)										
Decomposition temperature (Td)										
Copper Pad Adhesion (CBP/Hot Pin Pull/Shear or Tensile)										
PCB fabrication process, drill wear, lamination & desmear cycle										
Shock & Vibe and Drop test data										
Priority Tier 3										
Fracture Toughness of Resin / Resin Cohesive Strength										
Glass transition temperature (Tg)										
MOT Maximum Operating Temperature										
Transient Bend										
Co-Planarity Warpage characteristics as a function of stack-up, layer thickness, and temperature										
Affect of Fillers										
Priority Tier 4										
Flexural strength										
Resin system dependency/hardening/curing agents										
Plastic and elastic deformation characteristics as function of stack-up, layer thickness, and temperature										
Micro and macro hardness										
Stiffness										
Punchability / Scoring / Break-off Performance										
Electrical Properties (UL CTI rating)										

Phase III	Oct-2009	Nov-2009	Dec-2009	Jan-2010	Feb-2010	Mar-2010	Apr-2010			
Compile results, assess significance, make recommendations, and publish report										
• Assess performance relative to market segment requirements										
• Assess technology readiness / identify gaps										
• Assess manufacturing capability and supply capacity										
• Report results in white paper										
• Present Results to iNEMI Membership – Webinar										
• Present Results to industry – (Example APEX) – Paper – Presentation										

PCB Materials & Signal Integrity Project Monitoring Plans:

- How will you ensure open lines of communication among participants?
 - Bi-weekly conference calls
 - Meeting minutes provided through email
 - Follow-up with individuals on an as-needed basis
 - Workshops and face-to-face meetings as appropriate
- Planned teleconference schedule
 - Bi-weekly conference calls
- Request progress reports as tasks are completed
- Dates of technical reviews (2 per year) and progress reports and what they will contain
- Practice risk analysis by anticipating problems and having alternate solutions ready
 - What happens if??
- Use opportunity analysis to identify new areas or topics that might be addressed in additional projects. This will prevent the scope of the current project from expanding and keep the project focused on the original goals.
- Review project requirements with suppliers before the project begins.

Outcome of the Program:

- Successful completion of this program will include the publication and presentation of the knowledge gap analysis in the public domain.

- Deliverables of this program include the following:
 - Workshop and associated slides for project members summarizing preliminary assessment of the state of knowledge.
 - Final slides and publication of our knowledge assessment.
 - Program results will be shared with the industry in order to drive alignment throughout the supply chain.
 - Knowledge assessment results will be shared through presentations and industry meetings and publication in an archival journal subject to group participant approval process.
 - Updated standards will be shared through publication of the new standards

General and Administrative Guidelines:

General and Administrative Guidelines for this project and all other iNEMI Projects are documented at http://thor.inemi.org/webdownload/join/gen_guidelines.pdf.