iNEMI®

International Electronics Manufacturing Initiative

Halogen Flame Retardant (HFR)-Free Technology Envelope Project

February 18, 2009

Advancing manufacturing technology

Agenda

11:00	Introductions
11:15	Overview of Project
11:30	Approve Participant Expectations
12:30	Review Timeline & Sub-team Requirements
1:00	Lunch
2:00	Company Participation (Critical Mass)
2:30	Identify Sub-team Participants
3:00	Break Out Sessions (SI & PCB)

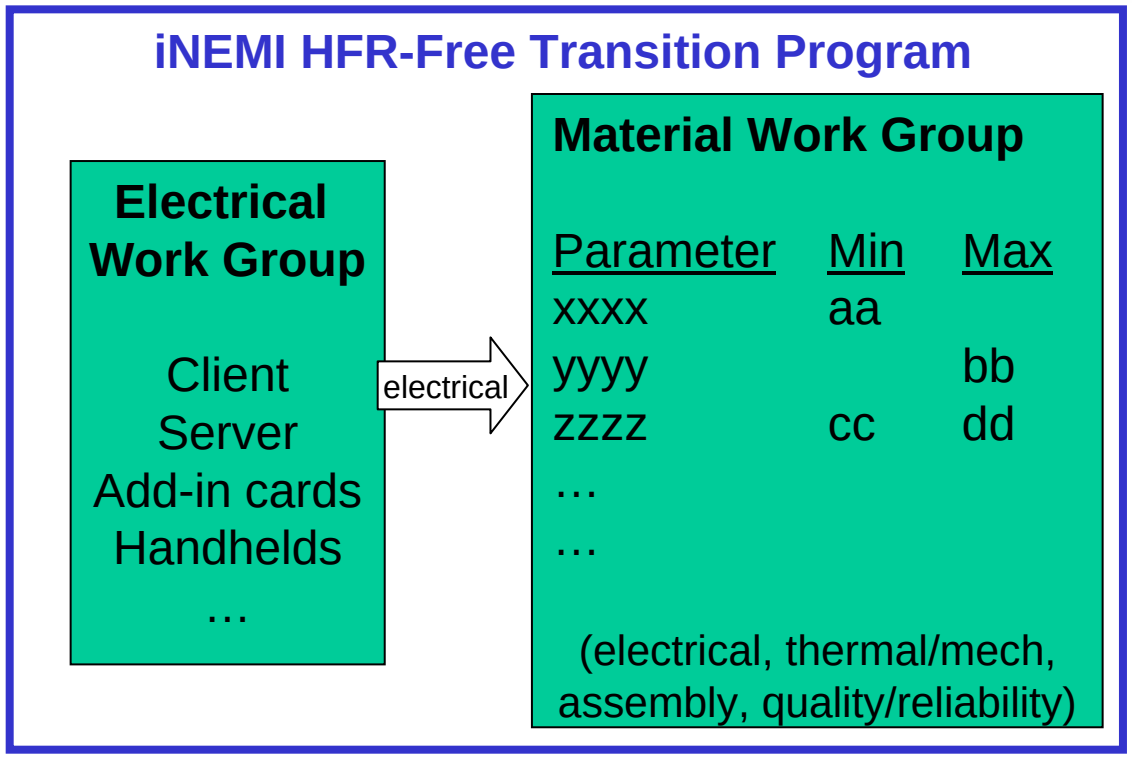
- Define strategy to craft technology timeline
- Identify major barriers to completing the work on time
- Recommend support needed to overcome barriers

5:30	Break (Steve Hall, John Davignon will draft reports during break)
6:00	Sub-team Reports (SI & PCB)
6:30	Wrap Up – Next Meetings Scheduled
7:00	Adjourn

Objective

1. Identify HFR-free PCB technology envelope which allows drop in replacement capability with standard FR4-based designs.
2. Identify technology readiness, supply capability and reliability characteristics for “HFR-free” alternatives to conventional printed wiring board materials and assemblies.
3. Provide Industry Standard Technology Envelope for HFR-free Materials across all market segments

Organizational Structure



Program Lead:
Martin Rausch
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Electrical WG Lead:
Steve Hall, Intel

Materials WG Lead:
John Davignon, Intel

Keys to success

- **Gain participation from all members of supply chain**
  - OEM, ODM/EMS, PCB suppliers, Laminate suppliers, DIMM/add-in card suppliers
- **Member companies ensure technology envelope meets requirements**
  - Reliability, availability, performance, etc…
- **Envelope gets used (de-facto standard)**
  - Specify product, drive new material development, etc…

HFR-Free Proposal
Deliverables

	New Value or Test Proposal			
	Property	Value		Unit
		Maximum	Minimum	
	Modified Value Range of STD Test			
1	Permittivity (Dk or Er), maximum @ 1MHz @ 1GHz Scan range 1-20 GHz			
2	Loss Tangent (Df), maximum @ 1MHz @ 1GHz Scan range 1-20 GHz			
3	Moisture Absorption, maximum		NA	
4	Flexural Strength, minimum Length direction Cross direction	NA		
5	Flammability			
6	Decomposition Temperature (Td)			
7	Z-Axis CTE Alpha 1 Alpha 2 50-260C			
8	Young's Modulus			
9	Thermal Resistance T260 T288			

Options

- **Define envelope using material parameters**
  - Must correlate stress test results to material parameters
- **Define suite of tests acceptable materials must meet**
  - Must establish common set of test methods

Approve Project / Participant Expectations

iNEMI HFR-Free PCB Technology Envelope Project

IS / IS NOT

This Project IS:	This Project IS NOT:
Technical evaluation of key electrical and mechanical properties of HFR-free Materials	**An EHS assessment**
Focused on those design attributes which are of most value to the broader industry	**Biased towards specific laminate suppliers, geographies, or market segments**
Build on learning from prior investigations	**Repeat of prior work**
Focused on circuit board materials and solder joint reliability – Board / Component Interaction	**Focused only on materials characterization**
Focused on generating data / design guidelines for development of an industry standard	

iNEMI HFR-Free PCB Technology Envelope Project

Phase I: Design

Review prior work and make recommendations for testing needed. Investigation should take into account needs of electronic product sectors represented by iNEMI membership.

1. Identify candidate materials

- Poll the supplier base, keying in on candidate materials that are commercially viable with consideration for market segment applications.
- Identify candidate HFR-free laminate materials to allow drop-in replacement for standard FR-4

2. Identify key performance characteristics and test criteria (Mobile / Desktop / Other?)

- Assess prior studies and identify critical knowledge gaps or technical issues. Make recommendations for performance tests needed. Review results of prior industry and member company investigations.
- Output broadband frequency dependant dielectric constant and loss tangent of candidate halogen free laminate materials (10KHz - 20GHz)
- Simulation results of high speed buses …. DDR3, PCI2,3 … others?

3. Design test vehicle(s) and test methodologies, leverage standards where possible

- Specify test vehicle criteria required for performance testing. Agree on a minimal number of test vehicle designs and test requirements.

iNEMI HFR-Free PCB Technology Envelope Project

Phase II: Test

Develop, manage, and execute performance testing.

1. Develop evaluation plan and schedule

- Outline key mechanical and electrical performance characteristics, and resource and time constraints. Focus on Electrical Characteristics, Delamination and Via & PTH reliability, Pad cratering and solder joint reliability.
  - Build systems with dielectric materials that comply with the proposed BFR-free dielectric spec
  - Provide data that shows comparison to identical FR4 systems
  - Determine compatibility of candidate laminate materials with higher temperature assembly process reflow environments (mixed solder: 245 C / Pb-free, 260C).

2. Procure parts and test vehicles

- Obtain needed evaluation materials. Consider lead times needed to synch with evaluation schedule. Solicit participation from supply partners.

3. Assign teams to carry out completion of the testing in a standardized fashion

- Each test should be carried out in a manner that produces meaningful results. Industry standards should be followed where applicable. Testing should be coordinated to allow correlation of results and sharing of test materials.

4. Perform mechanical and reliability testing on test vehicles.

- Leverage capabilities and expertise of participating members and supply partners. Follow test procedures carefully and record positive and negative results.

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Phase III: Results

Compile results, assess significance, make recommendations, and publish report.

1. Assess technology readiness / identify gaps

- Flag unexplored issues and identify technical risks that need to be resolved before materials can be widely adopted. Make recommendations for future work.

2. Assess manufacturing capability and supply capacity

- Work with suppliers and EMS's to identify barriers to supply chain viability. Interpret implications of performance testing in terms of manufacturing capability.

3. Publish results

- Compile and edit concise summary of methods, meaningful results, and recommendations. Goal is to roll the final report to members by Y/E 2010 with public release by IPC/APEX 2011

iNEMI HFR-Free PCB Technology Envelope Project
Anticipated Outcome

- **Material Property Path Vs. Test Suite Path**

– **Validate electrical and mechanical properties**
  - Loss tangent and Dk modeling over required range of signal speed
  - Signal Integrity Capability / Validation (DDR2, DDR3 etc)
  - Mechanical performance validation for lead free assembly and rework (delamination)
  - Critical Test Parameter Evaluation (CAF, IST, flex, etc.)

– **Validate Board Level Reliability Capability**
  - PCB Modulus / Thickness Impact on Mechanical Capability
  - HF Board Level Assembly / Rework Process Characterization
  - Mechanical Characteristics (Pad Crater / Ball Pull etc)
  - CTE Characteristics
  - SJR (Shock / TC etc)
  - HF Component / HF PCB Interaction

– **Provide Industry with an accepted Standard Technology Envelope for HFR-free PCB Materials**

Participant Expectations (Input?)

1. **Agree on identifying a transition date / timeframe to move to HF PCB Materials**
   1. Possibly by application / market segment
   2. Full BOM enabling will be driven by OEM/ODM (This is due to the complexity of business models)

2. **Agree to commit appropriate resources to meet accelerated project timeline and targeted end dates**
   - Weekly Calls, FTF Meetings When Appropriate
   - Provide Key Electrical / Mechanical parameter requirements by market segment to generate appropriate Stack Up Definitions, Test Plans and Identify Appropriate Material Candidates
     - Intel to provide the initial strawman
   - Agree to provide materials, components, Test Vehicles, Design Capability, Modeling Capability, PCB Fabrication, PCB assembly, Test Capability, FA Capability as required by Test Plan

3. **Collaborate on input to final report**

4. **Agree to adopt the HF PCB technology envelope parameters in future designs**

5. **Provide Recommendations for Industry Standards to IPC / JEDEC to generate and publish a Spec (if applicable)**
   1. HF PCB Technology Envelope (Design Guidelines)

Timeline / Sub-team Requirements

Signal Integrity Strategy

Steve Hall - Intel

Signal Integrity with Halide Free Boards

Problem

- The permittivity range for available halogen free dielectrics is too wide for a single design (**HF → 3.6≤e_r≤5.2, requires ~2-3 separate designs)**
- High end of permittivity range increases crosstalk, risk & cost
  - **More layers needed to compensate for crosstalk when permittivity is too high → leads to more cost**
- Industry specs such as PCIe are based on standard FR4 behavior
  - **Changing the FR4 assumption requires the specs to be re-visited**

Plan

Define an "*electrical envelope*" for HF dielectrics to ensure drop in compatibility with 1080 FR4

- **Eliminates need for multiple design guides (HF & FR4)**
- **Ensures industry specs (e.g., PCIe) remain valid**

Strategy

- Characterize available HF dielectrics
  - **Assess critical electrical properties**
- Simulation
  - **Define the "dielectric electrical envelope" based on DDR3 & PCIe2,3**
- Validation Platforms
  - **Ensure envelope is valid**

Signal Integrity Input

1. **Consensus/input on the variables and ranges in the electrical envelope**
   - **Dk (Er)**
   - **Df (TanD)**
   - **Delta TanD due to Moisture Uptake**
   - **Frequency (10 MHz – 20 GHz)**

2. **Consensus on dielectric property measurement methods going forward**
   - **Split Post Resonator**
   - **Short Pulse Propagation (TDR)**
   - **Transmission Line Extraction (VNA)**

Signal Integrity Input

3. **Comparative data to FR4 Baseline (1080 cloth) validating the HF electrical envelope corners**
   - **Tangible (non-simulated) data is needed to ensure nothing was missed**
     - **Identification / Development / Characterization of passive test boards (Loss, impedance, crosstalk … etc. on HF vs FR4)**
     - **Apples / Apples comparison of DDR & PCIe margins on active systems (HF vs. FR4)**
   - **Description of test methodology for each current data set is critical**

Signal Integrity Output

- **Identification of the key electrical parameters of the HF dielectric needed to ensure electrical performance on par with 1080 FR4**
  - Ensures drop in compatibility with FR4 Designs
    - Eliminates need for two sets of design guides (HF & FR4)
    - Ensures industry specs (e.g., PCIe) remain valid
    - Removes the signal integrity risk of HF PCBs

Note: HF electrical properties do not need to overlap 100% with FR4 … need to be close enough

PCB Material Development Strategy

John Davignon - Intel

Baseline Assumption / Materials WG Goals

Problem Statement:

- **The majority of HF PCB Laminate Materials have Electrical and Thermo-Mechanical properties that make a smooth transition difficult.**

Goals

- **Define a Reliable HFR Laminate for DT/NB/Server Markets**
- **Develop a Laminate Technology Envelope and/or Test Methodology to define the required laminate properties or performance response**
- **Deliver a Timeline for HFR Laminate Suppliers to manufacture laminates in volume with these properties/performance criteria**

Material WG Strategy Options

(A) Material Property Path

Vs.

(B) Test Suite Path

The consortia needs to decide on one strategy based on timelines and resources available.

(A) Matr'l Property Strategy (Laminate based)

1. Correlate known defects/performance degradation to Laminate Material Properties
2. Define Metrologies & Methods to assess these Material Properties at Laminate Supplier Level
3. Consortia test and review Laminate Material properties and performance values
4. OEM/ODM Build TV and Products to verify PCB Reliability, SJR and Assembly Yields of these Laminates within Tech Envelope
5. Set Technology Envelope values for Laminates with corresponding Metrologies
6. Work with Supply Chain to verify Capacity of Laminate within Tech Envelope
7. Incorporate new Tech Envelope criteria into laminate data sheet

(B) Test Suite Strategy (System based)

1. **Define all known defects / performance degradation**
2. **Define System Based Test Suite**
   - Define test methods to assess defect levels
   - Develop Common Test Vehicles for assessment
3. **Set up third party test house**
4. **Consortia builds, test and review Material performance**
5. **OEM / ODM builds Products to verify PCB Reliability, SJR and Assembly Yields of Laminates in Test suite**
6. **Set Technology Envelope values for Laminates**
7. **Work with Supply Chain to verify Capacity of Laminate within Tech Envelope**
8. **Incorporate new Tech Envelope criteria into laminate data sheet**

PCB Materials Development Input

Expectations of Consortia Membership:

- Joint evaluation and analysis of Laminate Properties and definition of Technology Envelope. Including:
  - Setting Max-Min Values
  - Test Methodology/Characterization
  - Reliability and Product Performance Validation
- Laminate Supplier will support/build according to the Technology Envelope/Guidelines
- OEM/ODM will build with the Laminates that meet this Guidelines/Technology Envelope

iNEMI BFR-Free High Reliability PCB Project
Proposed Project Schedule

Project Execution - SI	*Completion TGT*
• Phase 1 (Identification of Electrical Envelope)	Jun'09
• Phase 2 (Characterization)	Dec'09
• Phase 3 (Validation)	Jun'10
• Release Results	Jul'10

Project Execution - PCB	
• Phase 1 (Define Initial Envelope)	Jun'09
• Phase 2 (Correlate Defects)	Oct'09
• Phase 3 (Define Metrologies / Methods)	Oct'09
• Phase 4 (Build TVs / Verify Reliability)	May'10
• Phase 5 (Verify Supply Capability)	Jul'10

Follow-Up Project / Sub-Team Meetings

- **Sub-Team Conference Calls (Times TBD)**
  - **Week of March 02 PCB WG**
  - **Week of March 09 SI WG**
  - **Week of March 16 PCB WG**
  - **Week of March 23 SI WG**
- **Full Project FTF Meetings**
  - **IPC / APEX (Las Vegas, NV)**
    - **April 1, 2009**
    - **1:00pm – 5:00pm**
    - **Room TBD**
- **Future FTF Meeting Venues - TBD**
  - **IPC Midwest (Schaumburg, IL) Sept 20 – 24**
  - **SMTAi (San Diego, CA) Oct 4 - 8**

Company Participation Critical Mass

Companies Required For Project Success

Companies Present Today / Need Commitment to Continue to Participate in Project	Additional Companies Needed
Acer Inc.	
Apple	
Ciba Corp.	
Cisco Systems, Inc.	
Dell	
Dow Chemical Company	
Guangdong Shengyi Sci. Tech Co., Ltd.	
Hewlett-Packard Company	
Hitachi Chemical Co. America, Ltd.	
Huawei Technologies Co., Ltd. (USA)	
iNEMI	
Intel Corporation	
Inventec	
ITEQ Corporation	
Lenovo	
Nan Ya Plastics	
On Demand Circuit Services, Inc.	
Panasonic Electric Works	
Pegatron	
Tech Circuits, Inc.	
SBC GLobal	

Sub-team Participants

iNEMI HFR-Free PCB Technology Envelope Project

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Signal Integrity WG – S. Hall (Intel) Co-Chair : TBD			
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PCB Material Development WG – Chair : J. Davignon (Intel) Co-Chair : TBD			
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Larry Legler (Dell), Connos Tai (Intel), Chen Chun Yao (Pegatron) have not signed up for either subgroup

iNEMI HFR-Free PCB Technology Envelope Project

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PCB Material Development WG – Chair : J. Davignon (Intel) Co-Chair : TBD			
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Breakout Sessions

3:00 – 5:30

Signal Integrity – P/C 90466254

PCB Materials – P/C 41138840

Wrap Up – Next Meeting Schedules

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