Ultra Low Loss Laminate/PCB for High Reliability & Performance

Call for Participation Webinar
May 13-14, 2014

Project Leaders:
Stephen Tisdale, Intel
Gary Long, Intel
Mason Hu, Cisco

iNEMI Staffs:
Haley Fu
Masahiro Tsuriya

iNEMI
International Electronics Manufacturing Initiative
Advancing manufacturing technology
Agenda

• Introduction of Project Chairs
• iNEMI Project Development Process
• Project Briefing
  – Companies Involved in Planning
  – Project IS/ISNot
  – Background & Objectives
  – Preliminary Experimental Plan
  – Timeline
• How to Join
• Q&A

Note: All phones will be on mute until the end of the presentation
Introduction of Project Chairs

• Gary Long… *Intel, PCB Technology Development Technologist*

• Stephen Tisdale… *Intel, Industry Standards Manager*

• Mason Hu… *Cisco Systems, Supply Chain Operation Director*
iNEMI Project Development Process - 5 Steps

0. INPUT
1. SELECTION
2. DEFINITION
3. PLANNING
4. EXECUTION / REVIEW
5. CLOSURE

“Initiative”
Open for Industry input

iNEMI Technical Committee (TC) Approval Required for Execution

“Project”
Limited to committed Members

Limited to committed Members
Project Briefing

Companies Involved in Planning

• Held several meetings in March and April, developing the project SOW (statement of work) and PS (project statement)

• People from 30+ companies joined the meetings. Appreciate their participation and inputs.
  
  – 3M, Agilent, Alcatel-Lucent, Avago, CALCE, Cisco Systems, Davignon Consultancy, Dow, Georgia Institute of Technology, Hewlett Packard, Hitachi Chemical, IBIDEN, IBM, Intel, Interconnect Technology Analysis, iST, ITEQ, Jabil, KETI, MacDermid, MGC, MSI, Namics, Nan Ya CCL, Oak-Mitsui Technologies, Peregrine Semiconductor, Rogers, Shengyi, SMCI, and Tapco Circuit Supply
## IS / IS NOT Analysis

<table>
<thead>
<tr>
<th>This Project IS:</th>
<th>This Project IS NOT:</th>
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<tbody>
<tr>
<td><strong>Provide initial analysis of what the Project IS and IS NOT</strong></td>
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<tr>
<td>Characterization of the Cu roughness</td>
<td>Comprehensive Cu roughness study</td>
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<tr>
<td>Evaluation of Electrical properties (Dk/Df) and performance loss based on glass types</td>
<td>Comprehensive study of glass types</td>
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<tr>
<td>Evaluation of Specific Mechanical Reliability characteristics (Delamination, fill etc)</td>
<td>Comprehensive manufacturability study</td>
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<tr>
<td>Documentation of manufacturability / manufacturing performance (manufacturer feedback on drill wear; hole wall roughness, hybrid stack-up compatibility etc)</td>
<td>Hybrid Stack-up Evaluation</td>
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<td>Characterize temperature and humidity effect on the electrical performance</td>
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<td>Characterize electrical performance vs frequency to a minimum of 40GHz</td>
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Project Background & Objectives

• **Problem Statement**
  – Currently there are very limited options for low cost high performance PCB materials capable of high volume manufacturing (HVM) process. High Layer Count / Multi -layer Constructions are becoming more and more complex with fewer material options.

• **Opportunity**
  – Drive competitive cost / high performance laminate capability by providing more material choices capable of HVM processing.

• **Purpose**
  – Provide detailed performance data to aid in material selection by evaluating new materials based on electrical and thermo-mechanical capabilities for high layer count / multi-layer applications.
  – Deliver material comparisons in a standardized format representative of typical product attributes.
  – Use industry standard testing protocols to evaluate the laminate material performance in a comprehensive manner.

• **Scope of Work**
  – The project will consist of designing, building, and evaluating a test vehicle or vehicles to examine the performance and reliability of selected laminate materials that fit the defined envelope set by the work group.
  – Evaluation of new materials based on electrical and thermo-mechanical capabilities for high layer count / multi-layer applications.
Preliminary Experimental Plan

Material Selection

Proposed Material Envelope

– Electrical Targets:
  • Dk – 3-4.2 @ 1GHz
  • Df – <= 0.005 @ 1GHz

– Thermo Mechanical Targets:
  • Tg – >160C
  • Z-CTE – <3.0% from 50 to 260C
  • Flexural or Young’s Modulus target?

– Construction:
  • Capable of multiple dielectric thicknesses from 3 mil to 10 mil
  • VLP or HVLP copper for cores

– UL V-0 rating

– Low halogen vs. brominated optional
Preliminary Experimental Plan

Test Board Construction

- 22 layers
- 4 – 2oz layers in the center of the stack-up
- 150 mils thick
- Single lamination
- Backdrilled electrical structures
- OSP surface finish (question compatibility with microprobing)
- Spread glass plys (i.e. 1086, 1067, etc.)
- Center prepreg higher resin content
Preliminary Experimental Plan

Material Testing

– Electrical Testing (target frequencies – 1 to 40+ GHz):
  • Resonator testing – Split post or cavity on low mid and high resin laminate samples
  • Transmission line structures (microstrip, stripline, and offset stripline)
    – VNA with microprobe
    – S3 with SMA connectors
    – SPP
    – SET2DIL
  • Test both dry and saturated

– Thermo Mechanical Testing:
  • TMA for z-CTE
  • Copper peel strength
  • Cold Ball Pull
Material Testing

- Reliability Testing (Board Level):
  - Thermal Cycling - 10/20/28 mil via/pad stack at 1mm pitch & 0.8mm pitch
    - IST
    - HATS
    - CITS, or other method
  - Precondition 6 or 10 X at 260C reflow
  - Split preconditioning between reflow and selective wave
  - Test conditions, and length of test TBD depending on method chosen
  - CAF - 12/22/30 mil via/pad stack at 0.8 mm, and 0.65 mm pitch all inline
    - Precondition 6 or 10 X at 260C reflow
    - Split preconditioning between reflow and selective wave
    - Test conditions, and length of test TBD depending on method chosen
  - Thermal Stress - Via/pad stacks and pitch from above tests
  - Solder float X times at 288C per IPC TM-650 2.6.8
Preliminary Experimental Plan

Test Board Characterization:

– X-section:
  • Hole wall quality:
    – Roughness, etch back, plating thickness and distribution
  • Copper roughness:
    – Measure core side and prepreg side of electrical structures
  • Physical measurements:
    – Measure dielectric thickness, trace widths and height of electrical structures

– Fabrication Feedback:
  • Oxide treatment used
  • Drill profile (feeds and speeds, stack-up, etc.)
  • Press profile
Material selection, Experiment matrix, Test vehicle(s) design, Resource allocation and Schedule will be firmed up during the Definition phase, which will be reviewed by the Technical Committee before Execution.

Member’s engagement and commitment to schedule are required.
How to Join

• Project has been approved by the iNEMI Technical Committee
• Open Enrollment for Project Sign-up will continue until May 31, 2014
• Project SOW and PS (Project Statement) can be found at the [Ultra Low Loss Laminate/PCB For High Reliability and Performance Project Page](http://www.inemi.org/node/2660)

• Steps for Joining the Project
  – Please note: iNEMI membership is required to participate in the iNEMI Project for Metals Recycling. The period for becoming a founding member of this project will close on May 31, 2014. Steps for joining the project are outlined below.
    • For iNEMI members:
      – Complete and sign the project statement
      – Fax the completed statement to +1 (703) 834-2735 or scan + email to infohelp@inemi.org
    • For non-members:
      – Discuss annual membership fees with Bill Bader in North America (bill.bader@inemi.org), Haley Fu in Asia (haley.fu@inemi.org), or Grace O'Malley in Europe (gomalley@inemi.org).
      – Complete the iNEMI membership application. ([www.inemi.org](http://www.inemi.org))
      – Fax the completed documents to +1 (703) 834-2735 or scan + email: infohelp@inemi.org.
      – Complete and sign the Project Statement
      – Fax the completed statement to +1 (703) 834-2735 or scan + email: infohelp@inemi.org.
Project Statement Agreement

- Have any intellectual property or background technology to disclose in conjunction with this project?
  - Does □ Does not □ (check one)

- The initial cost projection for this project is a maximum cost exposure for a single company set at US$5,000.

- Check the items in the Appendix for in-kind support

- Participant & management signature

### Appendix: Resource In-kind Contribution

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<thead>
<tr>
<th>Material</th>
<th>Design</th>
<th>Test Vehicle</th>
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<tr>
<td>Laminates</td>
<td>Text board fabrication</td>
<td>Electrical Testing (target frequencies – 1 to 40+ GHz)</td>
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<td>Copper foil</td>
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<td>- Resonator testing – Split post or cavity on low and high resin laminate samples</td>
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Input others not in the list but you recommend
www.inemi.org

Email contacts:

Masahiro Tsuriya
m.tsuriya@inemi.org

Haley Fu
haley.fu@inemi.org