International Electronics Manufacturing Initiative

Advancing manufacturing technology

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iNEMI Statement of Work (SOW)
Board Assembly TIG
iNEMI Solder Paste Deposition Project

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Co-Project Leader:
TC Coach:

Basic Project Information

Background

As the density of board design increasing fast, the distances between the adjacent components become much smaller. When the miniature chip components (such as the 0201 / 01005 components) and the fine pitch components (such as 0.4 mm pitch QFPs/CSPs) which require smaller volumes of solder paste are close to the castle-like components, connectors with poor pin co-planarity and CCGAs which require more solder paste, only one single thickness stencil could not satisfy all of the components at the same printing process. For example, the miniature and fine pitch components can obtain good printing and assembly effect by 0.1mm or 0.12mm stencil,, while the solder joints of large components might open for lacking of solder paste, on the other hand, the big components can solder well by 0.15mm even 0.18mm stencil,, whereas some defects such as the tombstone, bridge or solder ball might happen to the miniature and fine pitch components.

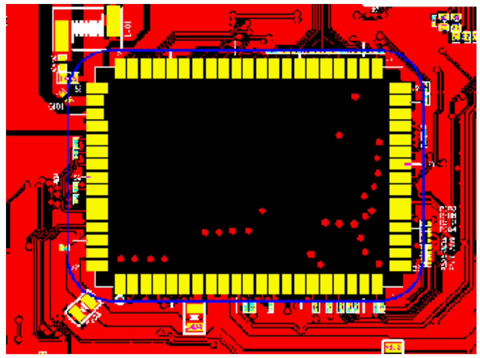

Fig.1 Miniature components close to the castle-like components

In this case, a step stencil may be the preference. This type of stencil is simple, flexible and low-cost, and useful to print miniature or fine pitch components by a thinner stencil foil but print other components by a thicker stencil foil, therefore it is widely used.

The problem of the step stencil is what the proper distance between the different components is, because the step of stencil may affect the thickness of solder paste deposition especially for the miniature and fine pitch components around the step. The keep-out distances K1 and K2 are shown in Figure 2. If the layout of PCB satisfies the keep-out distances, all of the components can get the proper solder paste volume. Neither K1 nor K2 would be the same in different cases, such as different step thickness or different components position. However, in the IPC-7525, step-down stencil and step-up stencil use the same design rule of the keep-out distances. So far we have not investigated more details about that.

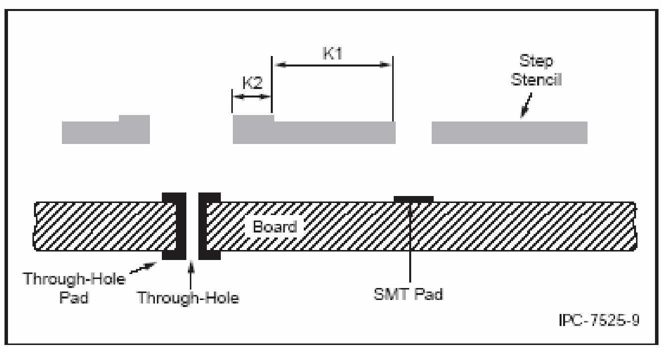

Fig.2 The keep-out distance between the components and the step of the step stencil

At present, the step stencil is the cheapest and most popular solution, but the layout density could not increase more because of the keep-out distances. And if there is a metal shield inside which has many miniature and fine pitch components, the step stencil could not solve this conflict. Because the step which encircles the inside components to supply the sufficient solder paste for the shield would result in the excessive solder paste to the inside components. For these reasons we suggest finding a new stencil technology, a new printing technology, a new dispensing technology, or a new paradigm for paste deposition to solve this problem. For example, developing a new printer to integrate the dispensing function with the printing technology—printing one thickness for normal components, and dispensing for other large components which require more solder paste.

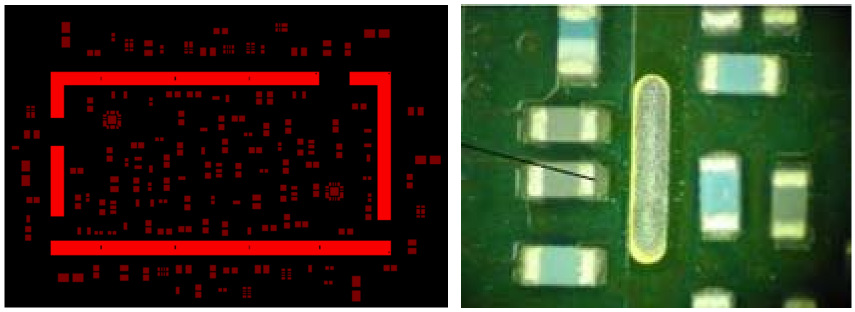

Fig.3 Miniature components inside the metal shield

Scope of Work

1. Research on the keep-out distances (K1 and K2) of step stencils in different conditions are as followed: 3D-SPI is used to measure the volumes of solder paste and then a requirement of PCB layout is proposed.
   - Project Object
     - ✓ One goal of this research is to reduce the keep-out distance (K1 + K2) to 1.0mm for step down/up stencil;

       (IPC-7525: K1≥36h, K2≥0.65mm, if h=0.06mm, K1+K2=2.81mm; if h=0.03mm, K1+K2=1.73.)
     - ✓ Another goal is to find the tendency of the deposition thickness near the steps, and then deduce formulas just like IPC-7525 Stencil Design Guidelines above.

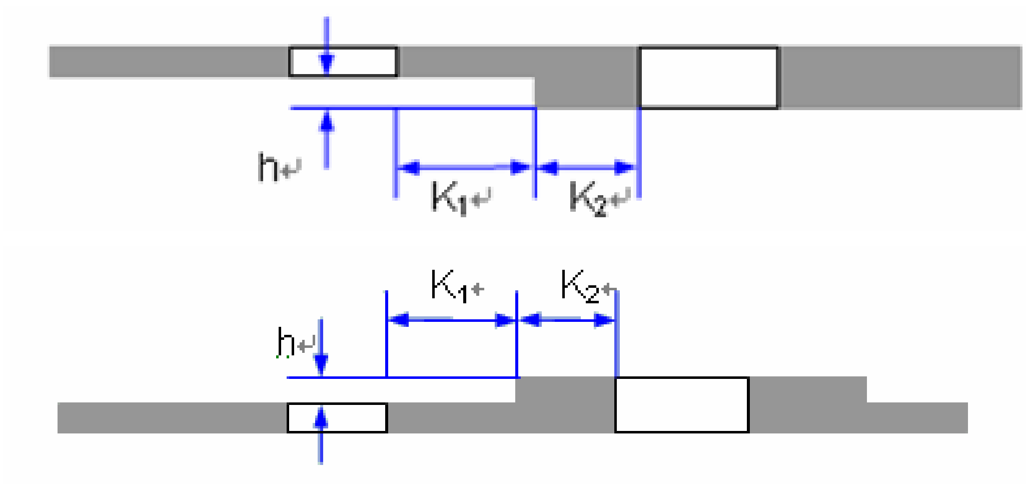

Fig.4 step-down stencil and step-up stencil

   - Experimental strategy
     - ✓ Selecting types of components based on the requirements of members;
     - ✓ Acceptance criterion of keep-out distance depends on the final assembly results. We try to attain the relationships between printing quality and assembly results;
     - ✓ The experimental results will be inspected by visual-mechanical inspection according to IPC-A-610D Acceptability of Electronic Assemblies, so the dummy and the daisy-chain design are not needed;
     - ✓ Confirming the acceptance of DPMO and the calculations of defects for it decides the samples in later experiments;
     - ✓ Phase 2 depends on the results of phase 1, and if the research in phase 1 obtains good solutions, phase 2 pauses, otherwise, phase 2 continues.

Notes：

- ✓ *The thickness of HASL varies much which may affect the solder paste inspection, and we have no data collection about that. Therefore, this surface finish will be remained and the measurement in thickness for HASL will be added;*
- ✓ *The perfect performance of solder paste type 5 is well-known in printing for 01005, so it will not be used in this project;*
- ✓ *The keep-out distances on PCB will be designed in multiple levels；*
- ✓ *Online 3D-SPI is applied to inspect the volume of solder paste printed on the PCB, and the data will be collected and analyzed.*

◆ PCB

The information of experimental boards used in this research are shown in table 2, and the designs of them are two steps:

Table 2. Possible PCB options

Experimental PCB	PCB length (mm)	PCB width (mm)	PCB thickness (mm)	Copper thickness of top layer	Surface finish
1	321~366.7	220~280	1.6/2.0/2.5	1OZ	HASL/OSP
2	≤100	≤50	0.8/1.0	HOZ	OSP

◆ Components

Components in different positions such as position1 and position2 are shown in figure 5, and components required in this research are shown in table 1, and the through-hole reflow components are not involved;

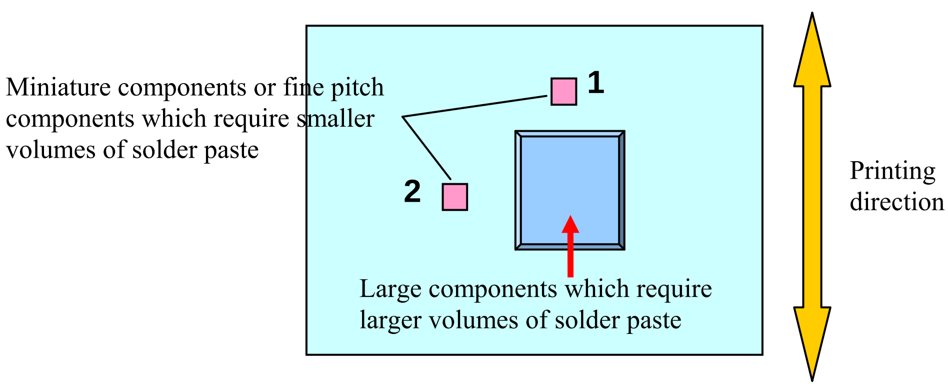

Fig.5 Relative positions of the different components

Table 1. Components suggested for research

	Component type	Manufacturer Suggested	I/O count	Pitch (mm)	Array	Body size (mm*mm)	PCB code in Table 2
Miniature and fine pitch components	01005					0.25*0.13	Only 2
	0201					0.6*0.3	1 and 2
	0402					1.0*0.5	1 and 2
	CSP		41	0.5	8*7	4.0*3.2	1 and 2
	CSP		192	0.4	16*16	7.0*7.0	1 and 2
	QFP		100	0.5		16*16	1 and 2
	QFP		128	0.4		16*16	1 and 2
Large components	Castle-like		12+2	2.0		20.3*14.8	1 and 2
	Shielding box					45*32	1 and 2
	BTB Connector		120	0.8		21.8*6.6	Only 1
	CCGA		1088	1.27	33*33	33*33	Only 1

- Groups for experiment conditions

The possible conditions including factors and levels for PCB1 are shown in table 3. Table 4 presents 16 groups in 64 (the 2^6 factorial groups) for PCB1, and it is possible two more factors with two levels could be added now if the project needs.

Table 3. Factors and Levels for PCB1

Factors		Levels	
		1	2
1	Surface finish	OSP	HASL
2	Solder paste	Lead-Free	SnPb
3	Solder particle	Type 3	Type 4
4	Stencil type	Laser-cut steel stencil	Electroform nickel stencil
5	Step type	Step-down	Step-up
6	Step thickness	0.03mm	0.06mm

Table4. Conditional groups and Budgets for PCB1

Number	Surface finish	Solder paste	Solder particle	Stencil type	Step type	Step thickness	Budget/US dollar	Owner suggested
1	OSP	Lead-Free	Type 4	Laser-cut	Step-up	0.06	600	
2	OSP	Lead-Free	Type 4	Electroform	Step-down	0.03	1,500	
3	OSP	Lead-Free	Type 3	Electroform	Step-up	0.06	1,500	
4	OSP	Lead-Free	Type 3	Laser-cut	Step-down	0.03	600	
5	OSP	SnPb	Type 3	Electroform	Step-down	0.06	1,500	
6	OSP	SnPb	Type 4	Laser-cut	Step-down	0.06	600	
7	OSP	SnPb	Type 4	Electroform	Step-up	0.03	1,500	
8	OSP	SnPb	Type 3	Laser-cut	Step-up	0.03	600	
9	Lead-Free HASL	Lead-Free	Type 3	Electroform	Step-up	0.03	1,500	
10	Lead-Free HASL	Lead-Free	Type 4	Electroform	Step-down	0.06	1,500	
11	Lead-Free HASL	Lead-Free	Type 3	Laser-cut	Step-	0.06	600	

					down			
12	Lead-Free HASL	Lead-Free	Type 4	Laser-cut	Step-up	0.03	600	
13	SnPb HASL	SnPb	Type 3	Electroform	Step-down	0.03	1,500	
14	SnPb HASL	SnPb	Type 3	Laser-cut	Step-up	0.06	600	
15	SnPb HASL	SnPb	Type 4	Electroform	Step-up	0.06	1,500	
16	SnPb HASL	SnPb	Type 4	Laser-cut	Step-down	0.03	600	

The conditions including factors and levels of PCB2 are shown in table 5. Table 6 presents the 2^3 full factorial DOE matrix of PCB2.

Table 5. Factors and Levels for PCB2

Factors		Levels	
		1	2
1	Surface finish	OSP	/
2	Solder paste	Lead-Free	/
3	Solder particle	Type 3	Type 4
4	Stencil type	Laser-cut steel stencil	Electroform nickel stencil
5	Step type	Step-down	Step-up
6	Step thickness	0.03mm	/

Table 6. Conditional groups and Budget for PCB2

Number	Solder particle	Stencil type	Step type	Budget/ US dollar	Owner suggested
1	Type 3	Electroform	Step-down	1,300	
2	Type 3	Electroform	Step-up	1,300	
3	Type 4	Electroform	Step-down	1,300	
4	Type 4	Electroform	Step-up	1,300	
5	Type 3	Laser-cut	Step-down	400	
6	Type 3	Laser-cut	Step-up	400	
7	Type 4	Laser-cut	Step-down	400	
8	Type 4	Laser-cut	Step-up	400	

- Total Budget

Materials	**Budget/US dollar**
PCBs	7,200
Step stencils	5,400
Components	14,000
Solder paste	600
Total	27,200

2. New technologies of paste deposition will be investigated and compared to solve the problem mentioned above which could not be solved by the step stencil. Suggesting the printing equipment supplier to be the leader to promote the research of new solder paste deposited technologies, such as developing new function equipments combining the

inkjet technologies with printing technologies.

3. Project schedule: 2008.02 ~ 2009.03

- Phase1— Researching on the keep-out distance design rule of the step stencil（2008.02 ~ 2009.03）
- Phase2— Investigating and developing new solder paste deposited technologies（2009.03 ~ 2009.12）

Purpose of Project

- Researching systemically on the keep-out distances of step stencils.
- Looking for the new solutions to components with different requirements of solder paste volumes on the same board in high-density layout.

Previous Related Work

- Chapter 3.5 in IPC-7525 Stencil Design Guidelines describes the design about the step stencils, and deduces a formula: $K1 \geq 36h$, $K2 \geq 0.65mm$.

Participants

Participant needed	Resource needed	Manufacturer Suggested
Printer suppliers (select one or two suppliers if needed)	**Printer Inkjet printer**	**DEK**
		Speedline（MPM）
		Panasonic
Inspector suppliers (select one supplier)	**3D-SPI**	**Kohyoung**
		Cyber
		Parmi
Stencil manufacturers (select one manufacturer)	**Step stencils**	
PCB manufacturers (select one or two manufacturers if needed)	**Drafting the experimental PCBs Manufacturing the experimental PCBs**	
Components suppliers	**Miniature & large components used in this research**	**Tyco**
		IBM
		Amkor
		Panasonic
Solder paste suppliers (select one supplier)	**Solder paste: type 3&type4; Sn/Pb & lead-free**	**Indium**
		Loctite
		Alpha
		Kester
		Tamura
		Senju
OEMs and EMS`	**SMT assembly line; Engineers**	**Huawei**
		Alcatel-Lucent
		Celestica
		RohmHaas

Project Plan

Schedule with Milestones

Phase 1 – Detailed Information

Phase1- Researching on the design rule of the step stencil																
Quarter		08Q1			08Q2			08Q3			08Q4			09Q1		
Month		1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
Task Description	**Deadline**															
Task1 - Define the project and call for the participants																
✓ Drafting out the project SOW	2008-2-20															
✓ Discuss and optimize SOW	2008-4-30															
Task2 - Project preparation																
✓ Sign the SOW and project agreement	2008-5-30															
✓ Confirm project members and resources	2008-5-30															
Task3 - Fulfill general experimental scheme																
✓ Consulting IPC about the origin of the design rule for step stencils in IPC-7525	2008-5-30															
✓ Draft out and evaluate the experimental scheme	2008-6-30															
✓ Draft the layout of PCBs	2008-7-15															
✓ Design the step stencils	2008-7-30															
Task4 - Design experimental board																
✓ Draw the experimental PCBs	2008-8-10															
✓ Evaluate the PCB design	2008-8-25															
Task5 - Materials Preparation																
✓ PCBs ✓ Components ✓ Solder paste ✓ Step stencils	2008-9-20															
Task6 - SMT assembly experiment																
✓ Print and solder paste online inspection, mount and reflow	2008-10-30															
✓ Solder joint visual-mechanical inspection	2008-10-30															
✓ Analyze experimental data	2008-11-20															
✓ Design and improve experiment	2009-1-30															
Task7 - Project summary																
✓ Evaluate conclusions and putting out a final report	2009-2-20															

✓ Decide whether to continue phase 2 or not	2009-3-30														
Phase2- Investigating and developing new solder paste deposition technologies															

Phase 2 – Detailed Information

- Investigating new printing technologies and equipments;
- Evaluating solutions and possibility;
- Experiments with these technologies and equipments.

Project monitoring plans

- How will you ensure open lines of communication among participants?
- Planned teleconference schedule
- Request progress reports as tasks are completed
- Dates of technical reviews (2 per year) and progress reports and what they will contain
- Practice risk analysis by anticipating problems and having alternate solutions ready
- Use opportunity analysis to identify new areas or topics that might be addressed in additional projects. This will prevent the scope of the current project from expanding and keep the project focused on original goals
- Review project requirements with suppliers before the project begins

Outcome of the project

- Research reports and design rules of the keep-out distances of step stencils.
- The investigation report of the new paste deposition technologies.
- Promoting the research of new paste deposition technologies to find an effective and low-cost solution to components with different requirements of solder paste volumes on the same board.

NOTE: All changes to SOW must be approved by the TC (version control)