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iNEMI Statement of Work (SOW) Board Assembly TIG iNEMI Pb-Free Early Failure Project

Version # 3.2

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Project Leader: Joe Smetana, Alcatel-Lucent

Co-Project Leader: TBD

TC Coach: TBD

Basic Project Information

Scope of Work

To test the sample size hypothesis and to attempt to determine the underlying causes of observed early failures, a basic thermal cycling test is proposed using up to three components each with a target sample size of 256. The sample size of 256 is roughly an order of magnitude greater than typical sample sizes (16-32) and it will conveniently require exactly one event detector. It is recommended that all other typical Pb free test parameters such as alloy, SMT process conditions, PCB thickness, preconditioning, thermal cycling test parameters, and surface finish be either fixed or eliminated. If early failures occur, the samples should be removed for immediate failure analysis. Additional criteria for testing need further discussion by the Project Formation Team.

Testing Overview (Components, Sample Size, Thermal Cycle, & PCB)

- **Components**
 - Components
 - 360 I/O Daisy Chain SAC405 Pb-free CBGA (NTK substrate – must be balled)
 - 84 I/O 0.5mm pitch Daisy Chain, SAC405 Pb-free CABGA, 7mm body size (Practical Components – www.practicalcomponents.com)
 - 192 I/O 0.8mm pitch Daisy Chain, SAC405 Pb-free CABGA, 14mm body size (Practical Components – www.practicalcomponents.com)
 - Failure Criteria:
 - First 2 components should be components that fail relatively quickly (to keep test times reasonable). One should have a large ball size and one should have a small ball size to see the different grain structures associated with different ball sizes
 - SAC 405 alloy
 - CBGA – with nickel interface
 - Third component
 - Another BGA – with a “little longer” life – such that there is more chance of seeing a group of early fails
- **Sample Size per component type**
 - Must be large
 - Target – 256 (1 event detector) per component
 - May be modified slightly if data loggers are used
- **Thermal Cycle**
 - Proposed per IPC-9701A, 0-100C, 10 minute dwell, 10 minute ramp
 - -40 to +125C thermal cycle - Possible for a follow-on project

- **PCB Design**
 - Designed to enable removal of individual component on failure without requiring removing entire board
 - Designed to simplify cabling/wiring (make number of parts per board – evenly divisible by number of test wires per cable i.e. 32 for 37 wire event detector cable)
 - .093 thick – with Pb-free compatible FR-4
 - 8 layers (minimum 2 internal planes)
 - Daisy chains on layer 1 wherever possible (vias may be required in a few locations – use multiple internal return connections and as large a via size as possible to minimize concerns with via fails)
 - Components on topside only
 - Components have been finalized and component data has been supplied
 - Agilent, Alcatel-Lucent, and Cisco will finalize on wiring requirements, board size, and number of components per board

Purpose of Project (Problem Statement)

1. Determine if a large sample size exposes Pb free early failures in accelerated thermal fatigue testing of Pb free solder joints.
2. If early failures are not observed in an experiment with small sample size, the solder joint assessment may result in an over estimation of the reliability of the Pb free solder.
3. If early failures are detected, work to understand the root causes so that Pb-free assembly can better meet the needs of mission critical applications.

What this project does/doesn't do

This Proposal	
Enables:	Does Not Enable:
Relatively easy failure isolation	Testing all possible combinations of board and component finishes
Individual failed part removal	Very large sample size at similar DNP/Strain
Multiple component types and associated stress strain characteristics	Complete evaluation of strain interaction with ball size
Multiple interface metallurgies	Multiple daisy chains per component
Multiple solder ball sizes and associated microstructures	
Sample size of 256 components ~4-8 solder balls at similar DNP/Strain per component	
Single daisy chain per component – designed to optimize testing (this could change if additional event detectors become available)	

Previous Related Work

Accelerated temperature cycling is an accepted reliability test method for measuring and characterizing the thermal fatigue reliability of SnPb surface mount solder attachments. The large body of SnPb test data and thorough understanding of SnPb soldering processes developed over decades has provided a suitable foundation for model validation and lifetime predictions of SnPb solder joints. The transition to Pb free manufacturing in the electronics industry has created a need to modify and adapt SnPb test methods to enable similar evaluations of Pb free solders. This task has proven to be challenging due to the uncertainty in establishing test methods and the subsequent interpretation of Pb free test data. In general, this problem is attributed to the significant physical and metallurgical differences between the SnPb and Pb free solders.

A topic that recently has generated interest is the interpretation of early failures or outliers in the thermal fatigue testing of Pb free solders. Outliers that occur in SnPb testing most commonly are attributed to assembly quality defects rather than the thermal fatigue (wear out) mechanism. Outliers caused by defective solder joint formation (inadequate wetting, poor printing, misalignment) can be identified and characterized, and those data points can be censored with confidence. However, the properties and failure behavior of Pb free solders cause complications in the analysis and interpretation of early failures or outliers. Figure 1 shows a Weibull plot of thermal cycle results that contains Pb free early failures.

Thermal Cycle Results: BGA-225 test results - Manufactured test vehicles (170°C Tg)

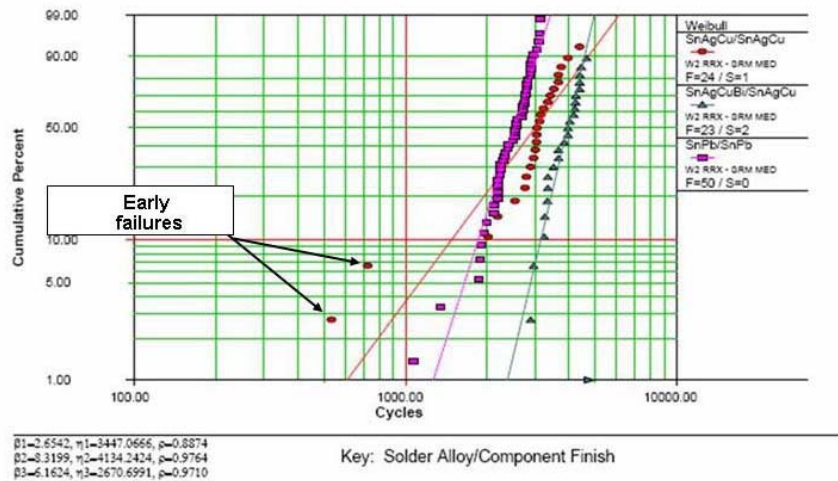


Figure 1. Thermal cycling results comparing Pb-free and SnPb BGAs. The Pb-free (SnAgCu) BGA shows two early failures (from Hillman and Wilcoxon [1])

It is possible that Pb free outliers could be a manifestation of structure/property relationships of the solder that are not traceable to assembly defects. Some suggested causes of Pb free outliers include: the influence of Sn grain orientation on CTE mismatch [2], interactions between Ag₃Sn platelets and propagating cracks [3], multiple crack initiation sites within the solder joint [4, 5], interfacial cracking modes (not found in SnPb solder joints) [6], and inherent microstructural variations related to SMT processing or aging conditions [7,8].

It has been difficult to assess the scope and significance of the Pb free early failure issue because early failures and outliers are not reported in all Pb free tests. If outliers indeed result from one or more of the subtle structure/property interactions, it has been hypothesized that the outlier incidence is low enough that outliers may not always appear with the relatively small sample size used in thermal cycling tests. If this proves to be true, it would imply that the traditional SnPb sample size (~32) is inadequate to characterize the reliability of Pb free solders. More specifically, if using inadequate sample sizes could mask early Pb free failures, then using the existing body of Pb free test data could result in erroneous, over predictions of reliability. Therefore, it is important to test the hypothesis that Pb free early failures will be observed if a larger sample size is employed in a thermal cycling test.

References:

IPC-9701A, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments," February 2006.

[1] David Hillman and Ross Wilcoxon, "JCAA/JG-PP Lead free Solder Testing for High Reliability Applications: -55 °C to +125 °C Thermal Cycle Testing," *Proceedings of SMTAI 2006*, 836-860, Chicago, IL, September 2006.

[2] T. R. Bieler, H. Jiang, L. P. Lehman, T. Kirkpatrick, and E. J. Cotts, "Influence of Sn Grain Orientation on the Thermomechanical Response of Pb-free Solder Joints," *Proceedings of Electronic Components Technology Conference 2006*, 1462-1467, June 2006.

[3] W. Henderson, T. Gosselin, A. Sarkhel, S. K. Kang, W. K. Choi, D.Y. Shih, C. Goldsmith, K.J. Puttlitz, "Ag₃Sn Plate Formation in the Solidification of Near Ternary Eutectic Sn-Ag-Cu Alloys", *J. of Materials Research*, Vol.17, No.11, 2775-78, November, 2002.

[4] Brian Vaccaro, Dan Gerlach, Richard Coyle, John Manock, Richard Popowich, Heather McCormick, George Riccitelli, and Debra Fleming, "Influence of Package Construction and Board Design Variables on the Solder Joint Reliability of SnPb and Pb-free PBGA Packages," *Proceedings of SMTAI 2006*, 272-282, Chicago, IL, September 2006.

[5] Dong Hyun Kim, Andrew Mawer, Tess J. Moon, and Glenn Y. Masada, "Crack Propagation Modeling and Analysis of SnPb and SnAg Solder Joints: Part II", 2003 ASME international mechanical engineering congress and R&D Expo, November 2003.

[6] D. Li, Changqing, and Paul P. Conway, "Characteristics of intermetallics and micromechanical properties during thermal aging of Sn-Ag-Cu flip-chip solder interconnects," J. Materials Science & Engineering A, Vol. 391, 95-103, 2005.

[7] Steve Dunford, Sridhar Canumalla, Puligandla Viswanadham, "Intermetallic Morphology and Damage Evolution Under Thermomechanical Fatigue of Lead (Pb)-Free Solder Interconnections," Electronic Components Technology Conference 2004, 726-736, June 2004.

[8] Hongtao Ma, Jeffrey C. Suhling, Pradeep Lal, and Michael Bozack, "Reliability of the Aging Lead Free Solder Joint," *Proceedings of Electronic Components Technology Conference 2006*, 849-864, June 2006.

Participants

Project Leader: Joe Smetana, Alcatel-Lucent

Board Design: Dong Hyun Kim, Cisco

Component/Board Procurement:

- Plan to split costs between team members (iNEMI to coordinate material acquisition)
- Current estimate \$12 - \$15K
- Low cost per company to participate

PCB Assembly: Celestica

Wiring List: Cisco

Thermal Cycling: Agilent – using data loggers

Weibull Analysis: Various (Alcatel-Lucent; Delphi)

Failure Analysis: Sub-team to be formed to address FA plan

- Richard Coyle (Alcatel-Lucent) to lead sub-team to address the FA plan
- Possibilities include:
 - Die Penetration and Pry
 - Cross-sections
 - Orientation analysis (EBSD)
 - Other

Final Report: Team

Possible Participants: Alcatel-Lucent, Celestica, Agilent, Cisco, HP, Delphi, Boston Scientific, Cookson Electronics, Flextronics, Huawei, Indium, Intel, Jabil, Kester, Nihon Superior, Plexus, Sanmina-SCI, Senju Comtek, STATS/ChipPac, Sun, TI, Tyco Electronics

Issues

- **Component and Board Acquisition**
 - No volunteers at this point
 - Plan to split costs (current guesstimate of around \$12k) between project team members
 - Low cost per company to participate
 - iNEMI to coordinate component and board acquisition
- **Failure Analysis**
 - Richard Coyle (Alcatel-Lucent) to lead sub-team to address the FA plan
 - Possibilities include:
 - Die Penetration and Pry
 - Cross-sections
 - Orientation analysis (EBSD)
 - Other

Project Plan

Schedule with Milestones

Project Tasks	Q1 2008			Q2 2008			Q3 2008			Q4 2008			Q1 2009			Q2 2009		
	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J
1. Complete Project Plan (03/15/2008)																		
2. Component Procurement (3 months) (Start - 03/15/2008)																		
3. Test Board Design (2 months) (Start - 05/15/2008)																		
4. Component Procurement Complete (06/12/2008 - includes ball attach if applicable)																		
5. Bare Board Fabrication (4 weeks) (Start - 06/12/2008)																		
6. PCB Assembly (4 weeks – EQ) (Start - 07/10/2008)																		
7. Wiring for T/C (3 weeks) (Start - 07/31/2008)																		
8. Thermal Cycling (Start - 08/21/2008)																		
9. Thermal Cycling (~4 month placeholder) (Amount of time from T/C/ depends on final components and T/C conditions.)																		
10. Failure Analysis (Start as failures occur with expected completion by 1/30/2009)																		
11. Final Report at APEX 2009? (April 2009)																		

Project Tasks – Detailed Information

1. Complete Project Plan (03/15/2008)

- **Resources**
 - Project Formation Team
- **Materials and Processes**
 - Not applicable
- **Testing Procedures**
 - Not applicable

2. Component Procurement (3 months) (Start - 03/15/2008)

- **Resources**
 - Project Team
 - No volunteers at this point
 - Plan to split costs between project team members
 - Current estimate is ~\$12k per company for component and board acquisition
 - Low cost per company to participate
 - iNEMI to coordinate component and board acquisition

- **Materials and Processes**
 - Not applicable
- **Testing Procedures**
 - Not applicable

3. Test Board Design (2 months) (Start - 05/15/2008)

- **Resources**
 - Cisco
- **Materials and Processes**
 - Designed to enable removal of individual component on failure without requiring removing entire board
 - Designed to simplify cabling/wiring (make number of parts per board – evenly divisible by number of test wires per cable i.e. 32 for 37 wire event detector cable)
 - .093 thick – with Pb-free compatible FR-4
 - 8 layers (minimum 2 internal planes)
 - Daisy chains on layer 1 wherever possible (Vias may be required in a few locations – use multiple internal return connections and as large a via size as possible to minimize concerns with via fails)
 - Components on topside only
 - Components have been finalized and component data has been supplied
 - Conference call with Agilent will finalize details on wiring requirements and decide on the number of components per board/board size (to keep wiring as simple as possible) –
- **Testing Procedures**
 - Not Applicable

4. Component Procurement Complete (06/12/2008 - includes ball attach if applicable)

- **Resources**
 - Project Team
 - No volunteers at this point
 - Plan to split costs between project team members
 - Current estimate is ~\$12k per company for component and board acquisition
 - Low cost per company to participate
 - iNEMI to coordinate component and board acquisition
- **Materials and Processes**
 - Not applicable
- **Testing Procedures**
 - Not applicable

5. Bare Board Fabrication (4 weeks) (Start - 06/12/2008)

- **Resources**
 - Project Team
 - No volunteers at this point
 - Plan to split costs between project team members
 - Current estimate is ~\$12k per company for component and board acquisition
 - Low cost per company to participate
 - iNEMI to coordinate component and board acquisition
- **Materials and Processes**
 - Not applicable
- **Testing Procedures**
 - Not applicable

6. PCB Assembly (4 weeks – EOQ) (Start - 07/10/2008)

- **Resources**
 - Celestica (Thilo to confirm)
- **Materials and Processes**
 - TBD

- **Testing Procedures**
 - TBD

7. Wiring for T/C (3 weeks) (Start - 07/31/2008)

- **Resources**
 - Agilent
- **Materials and Processes**
 - TBD
- **Testing Procedures**
 - TBD

8. Thermal Cycling (Start - 08/21/2008)

- **Resources**
 - Agilent using data loggers
- **Materials and Processes**
 - Data logging hardware to be supplied by Agilent
- **Testing Procedures**
 - Single event detector per component using data loggers

9. Thermal Cycling (~4 months?) (Amount of time from T/C/ depends on final components and T/C conditions. Current set of components are expected to fail quickly, which could shorten this time)

- **Resources**
 - Agilent using data loggers
- **Materials and Processes**
 - Proposed per IPC-9701A, 0-100C, 10 minute dwell, 10 minute ramp
 - -40 to +125C thermal cycle – possible follow-on project
- **Testing Procedures**
 - Single event detector per component using data loggers

10. Failure Analysis (Start as failures occur with expected completion by 1/30/2009)

- **Resources**
 - HP, Alcatel-Lucent, Celestica, Delphi, Cisco, HP (to be confirmed)
 - Others TBD
- **Materials and Processes**
 - Richard Coyle (Alcatel-Lucent) to lead sub-team to address the FA plan
- **Testing Procedures (possibilities)**
 - Die Penetration and Pry
 - Cross-sections
 - Orientation analysis (EBSD)
 - Other

11. Final Report at APEX 2009? (April 2009)

- **Resources**
 - Project Team
- **Materials and Processes**
 - Not Applicable
- **Testing Procedures**
 - Not Applicable

Project monitoring plans

- Bi-weekly conference calls
- More often if needed

- Progress reports will be generated by team as data becomes available
- Dates of technical reviews and progress reports
 - Project Initiation – 3-15-2008
 - Thermal Cycling start – 8-21-2008
 - Provide project progress to Technical Committee
 - TC Meeting (9-22-2008) - IPC Midwest Conference Schaumburg
 - TC Conference Call (12-4-2008) – Year end conference call
- Practice risk analysis by anticipating problems and having alternate solutions ready
- Use opportunity analysis to identify new areas or topics that might be addressed in additional projects. This will prevent the scope of the current project from expanding and keep the project focused on original goals
- Review project requirements with suppliers before the project begins

Outcome of the project

- Define project success, including what gaps will be closed

Summary

- There are significant physical and metallurgical differences between SnPb and Pb-free solders. This has a direct effect on thermal cycle performance.
- In SnPb assembly, where there is a large body of data, outliers are commonly attributed to assembly quality defect rather than the thermal fatigue (wear out) mechanism.
- There are complications in extending the SnPb behavior to SAC solders as the properties and failure behavior are markedly different
- It is possible that Pb-free outliers are a manifestation of structure/property relationships that are not traceable to assembly defects. Suggested possible causes include
 - Influence of Sn grain orientation on CTE mismatch and/or fatigue crack propagation
 - Interactions between Ag₃Sn platelets and propagating fatigue cracks
 - Multiple crack initiation sites within a solder joint
 - Interfacial cracking modes not found in SnPb solder joints
 - Inherent microstructure variations related to SMT processing and/or aging conditions
- If the outliers identified in Pb-free soldering thermal fatigue studies are a function of the structure/properties as noted above, this may not be visible in the relatively small sample size used in thermal cycling tests
- If this is true, it would imply that that traditional SnPb sample size (32) is inadequate to characterize the reliability of Pb-free solders, and test data using these sample sizes could result in over predictions of reliability
- List all deliverables
 - Detailed data on the time to failure for the 3 components
 - Failure analysis results indicating root cause of failure
 - Weibull analysis of failures
 - Other data, as determined by the Project Team members, to provide a better understanding of the failure mechanisms
- State which project results will be shared, with whom, and by what means
 - Detailed project results will only be available to the Project Team Members
 - iNEMI member companies will be provided a summary of data collected. Information to be shared will be determined by the Project Team
 - External presentations will be made based on the results. The information contained in the presentations will be determined by the Project Team

NOTE: All changes to SOW must be approved by the TC (version control)