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Advancing manufacturing technology
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iNEMI Statement of Work (SOW)
Board Assembly TIG
iNEMI Board Coplanarity in SMT Project

Version #5.0
Date: May 8, 2008
Project Leader: John Davignon, Intel Corporation
Co-Project Leader:
TC Coach:

Basic Project Information

Scope of Work

1. **Determine metrologies needed to measure board flatness in land area of components and connectors at both room and elevated temperature.**
    a. Compare available techniques and set minimum metrology requirements including accuracy & calibration standards. Collect existing data from the project participants as to establish repeatability, reproducibility, and capability. If necessary, the project group will use a third party (NIST, iNEMI, Academic) to collect and sanitize the data.
    b. Establish knowledge base of board flatness by board features (thickness, materials, and design) through data collection and sampling of multiple board technologies supplied by members of the project team.
    c. Identify sources of warpage during board processing and assembly via experimental data collection. Data collection will be completed at sites volunteered by members of the project team.
    d. Establish a correlation between room and elevated temperature flatness.
    e. Identify best points during processing to monitor for flatness.

2. **Develop strategy on requirements for differing board features to recommend to IPC, using the following as possible baseline:**
    a. How best to deal with multiple components on the same board of varying sizes
    b. Localized vs full board requirements
    c. Impact of using reflow jigs and/or pallets
    d. Correlation of various package sizes and board thickness

3. **Recommend acceptance criteria for board flatness, and conditions for sampling and measurement requirements.**

4. **Collect data on and list, First Pass Yield and solder joint quality / reliability based on package and board interaction.**

5. **Summarize the above in a white paper.**

Phase II - Need for a Phase II would be evaluated during Phase I, if a need is identified for data collection at multiple sites under more controlled conditions.

Purpose of Project

This project will identify limitations of systems that currently exist today and in addition, will propose new metrologies or test methods if needed.
In addition, the project will propose recommendations to enable the measurement and specification for board land coplanarity to ensure high quality, high yield SMT processes for current and next generation components and boards.

- The work will provide a foundation for future specifications by IPC for board flatness
- It is anticipated that this project will provide:
    - List of metrologies for characterizing board flatness in standardized way
    - Understanding of the causes and source of board warpage during fabrication and processing (requires input from suppliers)
    - Recommendations for process improvements in SMT assembly to improve quality and yield, reducing rework, scrap, and waste

Previous Related Work

Both JEDEC and JEITA have research in this area, focusing on the component and total allowable coplanarity tolerance.
Paper by Mike Varnau (not published)
Board level – References from Cisco

- The current specifications for component lead coplanarity and board bow and twist have not kept pace with the developments in packaging and board technology. Currently some system manufacturers are experiencing poor SMT yields using materials that meet the current specifications.
- The converse is also true. Some of the newest component technologies are hampered as they fail to meet the current component standards; however have demonstrated high yields in SMT assembly.
- It is clear that updated standards are needed that can provide the needed assurance of quality while maintaining the continuous innovation that is basis of the industry.
- New measurement techniques have enabled the measurement of flatness during simulated SMT conditions allowing more relevant standards to be developed.
- Several Standards bodies have already issued standards using these new measurement techniques for components. These standards efforts could be extended to ensure the flatness of system boards as well.

Project Formation Participants

AkroMetrix, LLC*	Patrick	Hassell
Cisco Systems*	James	Henzi
Delphi Electronics & Safety*	Douglas	Boyd
Delphi Electronics & Safety	Fred	Kuhlman
Delphi Electronics & Safety	Jim	Spall
Delphi Electronics & Safety	Michael	Varnau
Freescale Semiconductor	Paul	Galles
Flextronics*	David	Mendez
Huawei	Xi	Angzhao
Huawei	Ding	Dongqing
Intel Corporation*	Steve	Cho
Intel Corporation	John	Davignon
Intel Corporation	Marilyn	Nowakowski
IPC	Tom	Newton
IPC	John	Perry
Texas Instruments Inc	Kurt	Wachtler
Tyco Electronics	Kevin	Leibold

* Project Formation Company, which has indicated their intent to participate in the iNEMI Board Coplanarity in SMT Project and provide data.

Project Plan

Phase 1 **Project Start June 2008** **Duration 12 Months**	**June -08**	**July -08**	**Aug -08**	**Sept -08**	**Oct -08**	**Nov -08**	**Dec -08**	**Jan -09**	**Feb -09**	**Mar -09**	**April -09**	**May -09**
Task 1 – Identify metrologies	X	X	X									
Task 2 – Comparison of available techniques and set minimum metrology requirements	X	X	X									
Task 3 – Data Collection	X	X	X	X	X	X	X	X	X			
Task 4 – Establish knowledge base of board flatness by board features				X	X	X	X	X	X			
Task 5 – Understand sources of warpage during board processing and assembly using experimental data collection at volunteer sites				X	X	X	X	X	X			
Task 6 – Establish a correlation					X	X	X	X	X			
Task 7 – Develop strategy for setting requirements for differing board features to recommend to IPC	X	X	X	X	X	X	X	X	X			
Task 8 – Recommend acceptance criteria for board flatness and conditions for sampling and measurement requirements										X	X	
Task 9 – APEX 2009 Paper Presentation											X	
Task 10 – Final Project Reports and Publications and Membership Webinar												X

Phase II

Validation and verification using targeted experiments to address identified gaps

Need for a Phase II would be evaluated after Phase I results.

Outcome of the project

- Successful completion of this project will include the publication and presentation of the knowledge gap analysis in the public domain.
- Deliverables of this project include the following.
    - Workshop & associated slides for project members summarizing preliminary assessment of the state of knowledge
    - Final slides and publication of our knowledge assessment
    - Project results will be shared with the industry in order to drive alignment throughout the supply chain.
    - Knowledge assessment results will be shared through presentations and industry meetings and publication in an archival journal
    - Updated standards will be shared through publication of the new standards

NOTE: All changes to SOW must be approved by the TC (version control)