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Hello, Valued Industry Leader,

The iNEMI SMT Coplanarity Working Group (WG) has recently added another section of investigation to its Dynamic PCB Coplanarity/Warpage evaluation. The WG has decided to baseline the present status of the PCB industry dynamic warpage for a few specific market sectors and PCB envelopes. Please see Table #1 for the specific PCB envelope we are evaluating.

The iNEMI Board Coplanarity in SMT WG consists of members from Intel Corporation; Flextronics; Cisco Systems, Inc.; STATS ChipPAC; Huawei Technologies Co., Ltd.; Akrometrix, LLC; and IPC.

This project is designed to:

- Establish metrologies needed to measure board flatness in land areas of components at both room and elevated temperatures.
- Develop strategy for setting requirements for differing board technologies and categories.
- Recommend acceptance criteria for board flatness and conditions for sampling and measurement requirements.

We are in the process of asking specific OEM/ODMs if they can assist with supplying the PCBs for our evaluation. These PCBs should fit within the design envelope of Table #1, and they can be electrically good PCBs or ones that have failed at Electrical Test. We do not need them to be electrically perfect; we only ask that they be representative of products that are being built at this time. They can have hammer marks (except in the BGA area) or other “Scrap” indicators as long as it does not affect the structural integrity of the PCB for warpage measurements. We will be using the Shadow Moiré technique for the Dynamic Warpage measurement.

**We would like you to provide:**

- 10 to 30 PCBs from any single design (square or rectangular shaped, no odd shapes or large cut outs).
- The Construction or Stack-up of the PCB (Layer count, Glass Styles, Copper weight).
- The PCB Fabricator and laminate material used in the construction would be appreciated (Laminate supplier trade name).
- As many designs, in as many design envelopes/market sectors as you can supply.

**There will be no:**

- Reverse engineering of the design or PCB (only used for Dynamic Warpage measurements).
- No mention of your company in relationship to any design or set of PCBs (blind test).
- All PCBs will be destroyed after measurement / data collection.

**You will receive in return:**

- The Dynamic Warpage of your PCBs (including room temperature through assembly temperatures and back down again).
- The Dynamic Warpage of all PCBs within your design envelope (blind test, no names of companies).

**How the data will be used:**

- This data will be included in the iNEMI study of Dynamic Warpage of PCBs and used in the assessment of the need for a Dynamic Warpage Methodology and/or Specification for PCBs.
- This data will also be provided to IPC as a baseline of PCB warpage for inclusion into various design guidelines.

**Table #1: Design Envelope for PCB Dynamic Warpage Measurement**

<b>Market Sector</b>	<b>Thickness</b>	<b>Layers</b>
Server (Extreme)	.093"-.135"	14 - 32
Server / Workstation	.062"-.093"	8 - 12
Desktop	.062"	4 - 6
Nettop	.062"	4 - 6
Notebook	.040"-.062"	6 - 10
Netbook	.040"-.062"	6 - 10

**Timeline:**

	<b>Schedule</b>
Baseline the present status of PCB Dynamic Coplanarity	
Procure real products from the Client Market Sector	Q2, 2010
Measure the PCBs w/ iNEMI Coplanarity WG test method	Q3, 2010
Analyze the data and write report	Q4, 2010
Return data to PCB Supplier	Dec 2010

The iNEMI Coplanarity WG wants to thank you for your help and assistance in this effort. Please contact the name(s) below for shipping instructions and to answer any questions.

Regards,

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