

**Statement of Work (SOW)  
Test TIG  
Boundary Scan Phase 2: Structural Test of  
External Memory Devices Project**

**Testing DDR Memory Task  
Addendum to Scope of Work**

**Version 4.1**

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**Boundary Scan Phase 2: Structural Test of External Memory Devices Project**

**Project Leader: Chair: Phil Geiger, Dell, Inc**

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**Testing DDR Memory Task**

**Chair: Kenneth Parker, Agilent**

**Executive Summary:**

Complex Printed Circuit Assembly (PCA) designs are using direct soldered DDR memory packages, instead of SIMMs or DIMMs. Many DDR memory packages are BGAs, which precludes visual inspection.

The elimination of board-level structural test methods and the lack of IC DFT (Design for Test) results in non efficient methods to precisely diagnose structural solder faults.

The members of the Boundary Scan Phase 2: Structural Test of External Memory Devices Project have agreed to address this industry gap, by adding an additional task, the **Testing DDR Memory Task (Task P5)**, to the project's SOW.

The additional task will establish a Design of Experiments (DOEs) to validate multiple solutions from technology, deployment and effectiveness perspectives.

To this end, the Testing DDR Memory Task group's goal is to organize an industry response that includes PCA OEMs (needing solutions) and DDR IC OEMs (solution providers).

In addition, the Sub-Working group plans to work with Memory vendors to add appropriate DFT.

Current Project Member agreement and understanding:

- The original project's work as stated in the project's SOW will conclude first quarter 2012.
- The project will be opened to the iNEMI's membership to join the Boundary Scan Phase 2: Structural Test of External Memory Devices Project to address the Testing DDR Memory Task, by signing the project's original Project Statement Document, those members who do sign will be considered a founding member of the original project.
- Original and new project members will be bound by the project's Project Statement Document therefore, the data, information, and conclusions developed during this project will be available only to participating members of iNEMI who have formally joined this project by signing this Project Statement.

## **Basic Additional Task Information**

### **Background**

Complex Printed Circuit Assembly (PCA) designs are using direct soldered DDR memory packages, instead of SIMMs or DIMMs. Many DDR memory packages are BGAs, which precludes visual inspection. Density and Signal Fidelity bed-of-nail probing access testing is eliminated since no test points are provided. Therefore, traditional PCA in circuit testing is not possible. Function-level testing cannot discern structural faults on bussed address / data / signal interconnects.

Lack of static-test-mode or test modes precludes usage of boundary-scan from the CPU or memory controller to test DDR memory during PCA test.

DDR IC Packaging of stacked die and shields frustrate capacitive-opens test methods (e.g. TestJet).

In addition, boundary-scan-enabled capacitive opens test methods are becoming more difficult as memory devices get smaller and are placed in BGA packages, as these trends reduce capacitive coupling efficiency.

## **Situation Analysis**

The Elimination of board-level structural test methods and lack of IC DFT results in no efficient method to precisely diagnose structural solder faults, resulting in replacing all devices to correct for even one bad solder joint which demands repair for high yields.

## **Purpose of Task**

To organize an industry response that includes PCA OEMs (needing solutions) and DDR IC OEMs (solution providers).

To establish Design of Experiments (DOEs) to validate multiple solutions from technology, deployment and effectiveness perspective. In addition, the group plans to work with Memory vendors to add appropriate DFT, considering:

1. IEEE 1149.1 Boundary Scan
2. IEEE 1581 test mode
3. JEDEC Standard 21-C “Boundary Scan” for 512Mb GDDR3 memory
4. Built-in “Capacitive Opens Test” leveraging Agilent IP (See USPTO Document US 2005/0253616 A1)

## **Scope of Additional Work**

### Tasks

1. Develop team of memory users with test problems (OEMs, Test Engineering Managers, DFT consultants, Component Engineers, Corporate buyers, JEDEC representatives).
2. Develop "cost of test" model to show positive impact of DFT in DDR memories.
3. Output:
  - a. Launch “cost of test model”
    - Publish - "cost of test"
    - Schedule - face-to-face Meeting
    - Identify target list of memory vendors to invite to public presentation of the cost model
    - Make case to memory vendors, face-to-face

## Task Plan

Structural Test of External Memory Devices Project		Quarters				
Task		1Q	2Q	3Q	4Q	
P5.1	Develop team of memory users with test problems	█	█	█		
P5.2	Develop "cost of test" model	█	█	█	█	
P5.3	Launch "Test Cost Model"			█	█	█
P5.4	Face-to-face meeting with Memory Vendors					█