BA-BIST: Board Test from Inside the IC Out

Zoë Conroy, Cisco
Al Crouch, Asset InterTech
iNEMI BIST Project
About this Presentation

- Board-Assist (BA-BIST) is enhanced IC BIST functionality for board testability and fault isolation.

- Why is this needed?
  - Increasing chip interface speeds and board integration (HDI*) make traditional board manufacturing test less capable.

- BA-BIST requirements are presented from board test engineers for their fellow IC designers!

* High Density Interconnect
Outline

- INEMI’s ‘BIST Project’ and contributing companies.
- Defects targeted by IC BA-BIST.
- Industry ‘use-cases’ for Board Test IC BA-BIST standardization.
- “Standardization” examples.
About Us

The International Electronics Manufacturing Initiative (iNEMI) is a not-for-profit, highly efficient R&D consortium of approximately 100 leading electronics manufacturers, suppliers, associations, government agencies and universities.

Our Mission
Forecast and accelerate improvements in the electronics manufacturing industry for a sustainable future.

What We Do
iNEMI roadmaps the future technology requirements of the global electronics industry, identifies and prioritizes technology and infrastructure gaps, and helps eliminate those gaps through timely, high-impact deployment projects. These projects support our members’ businesses by accelerating deployment of new technologies, developing industry infrastructure, stimulating standards development, and disseminating efficient business practices. We also sponsor proactive forums on key industry issues and publish position papers to focus industry direction.

Focus Areas
iNEMI implements a full global agenda that is manifested through proven collaboration methods to deliver lasting results. Our R&D efforts focus on four key technology areas:
- Miniaturization
- Environment
- Medical electronics
Purpose of iNEMI’s BIST Project

• Why?....
  – Most “chip” level BISTs are designed for IC manufacturing,
  – Tests and algorithms are often not optimized to run at board test,
  – No standard way to test chip level interfaces or algorithms.

• Develop and promote board/system test adoption of IC BIST.

• Steer IC providers toward BIST functions helpful for board/system test.

• Provide standardization for BIST interfaces and algorithms.

• Encourage IC and ATE/Instrument vendors to provide standardized products and tools.
# Major Contributors

<table>
<thead>
<tr>
<th>Company</th>
<th>Participants</th>
</tr>
</thead>
<tbody>
<tr>
<td>Agilent</td>
<td>Hui Li, Jun Balangue</td>
</tr>
<tr>
<td>Alcatel Lucent</td>
<td>Brad van Treuren</td>
</tr>
<tr>
<td>Asset InterTech</td>
<td>Al Crouch</td>
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<tr>
<td>Cisco</td>
<td>Zoë Conroy, Rob Pike</td>
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<tr>
<td>Corelis</td>
<td>Harrison Miles</td>
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<tr>
<td>Dell</td>
<td>Phil Geiger</td>
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<tr>
<td>EMC</td>
<td>Jeffrey Moore</td>
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<tr>
<td>Hewlett Packard</td>
<td>Skip Myers</td>
</tr>
<tr>
<td>IBM</td>
<td>Derek Robinson</td>
</tr>
<tr>
<td>Intel</td>
<td>James Grealish,</td>
</tr>
<tr>
<td>Teradyne</td>
<td>Tony Suto</td>
</tr>
</tbody>
</table>
Industry Surveys on IC BIST Usage

Objectives:

• Gauge how much component BIST is currently run at board test.

• Evaluate its usefulness.

• Get board/system test/debug engineers to identify what their problems are and what may be solved with a “BIST function”.

• Agreement on a board BIST definition.

• Identify BIST Use Cases for board test standardization.
How did the Industry Respond?

• Many IC BISTs are available and run at board level
  • 60% Board designers are requesting access to IC BIST
• BIST run at the board level is good at catching defects
  • Seen to be critical for future fault isolation
  • Would like BIST coverage to be > 80% at board test
  • Currently run at many different board/system test steps
• Access to BIST is predominantly via IEEE1149.1 TAP
  • > 75% respondents see BIST coupled with boundary-scan replacing lack of test point access.
BA-BIST Use Case Requirements

- BA-BIST needs to SOQ-FAM* interconnect between 2 ICs.
- Existing IC BIST can be used, with features for board test.
- Test steps are manufacturing board test, NPI, board debug and diagnosis.

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* Shorts, Opens, Quality – Function, At-speed, Measure
Board-Assistance BIST is an embedded capability within an IC that is fully or partially self-contained, and incorporates some or all of the following:

- pattern/signal generation,
- pattern/signal delivery,
- response or data capture,
- response evaluation functions.
## Board Defects covered by BA-BIST

<table>
<thead>
<tr>
<th>Fault Model Category</th>
<th>Traditional Test Type</th>
<th>Typical Use Environment</th>
<th>Defect Classes</th>
<th>BA-BIST coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trace stuck-at-1,0</td>
<td>ICT, boundary scan</td>
<td>NPI, mfg test, debug, yield</td>
<td>Signal trace shorted/open to power/GND, bridged to signal</td>
<td>yes</td>
</tr>
<tr>
<td>Trace transitions randomly</td>
<td>ICT, boundary scan</td>
<td>NPI, mfg test, debug, yield</td>
<td>Broken trace, open trace, undriven open</td>
<td>yes</td>
</tr>
<tr>
<td>Trace impedance</td>
<td>ICT, boundary scan</td>
<td>Mfg test</td>
<td>Malformed trace</td>
<td>no</td>
</tr>
<tr>
<td>High speed trace specification</td>
<td>At-speed functional</td>
<td>NPI, debug ,yield</td>
<td>Chip drive, malformed trace</td>
<td>yes</td>
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<td>Signal integrity</td>
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BA-BIST Use Case Standard Scenarios

- IC1 BA-BIST communicates to IC2 IO.
- IC1 BA-BIST communicates to IC2 IO and loops back.
- IC1 and IC2 have BA-BISTs that work together.
**BA-BIST Requirements Template**

<table>
<thead>
<tr>
<th><strong>Given two connecting chips:</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Goal:</strong> To provide a test that exercises board level nets to identify faults.</td>
</tr>
<tr>
<td><strong>Assumptions:</strong> Board test assumptions on pre-testing, board state, board config.</td>
</tr>
<tr>
<td><strong>Pre-requisites:</strong> Board conditions needed to set up and run the BA-BIST</td>
</tr>
<tr>
<td><strong>Dependencies:</strong> Links to other chips, tests, or board conditions.</td>
</tr>
<tr>
<td><strong>Consequences:</strong> From assumptions, pre-requisites and dependencies.</td>
</tr>
<tr>
<td><strong>Target:</strong> Manufacturing test step and debug/diagnosis requirement.</td>
</tr>
<tr>
<td><strong>Action:</strong> To enable BA-BIST(s) within one chip that is connected to a 2nd chip.</td>
</tr>
<tr>
<td><strong>Sequence:</strong> To write to n-locations using k-data (0, F, 5, A, etc.) in the following address sequence (addr&lt;0&gt;, addr&lt;5&gt;, etc.)</td>
</tr>
<tr>
<td><strong>Metric:</strong> Fail test data that provides correct diagnosis can be retrieved.</td>
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</table>
Source Chip that contains a BA-BIST Memory Test Function

Clock Gen

Template Example: Memory Test

1 G-bit x 64
1 G-bit x 64
1 G-bit x 64
1 G-bit x 64
Completed Template: BA-BIST Instrument to Memory

**Goal:**
To provide a test that will exercise all nets (signals, clocks, power, ground) to identify faults (shorts, opens, bridges) on the interface from an ASIC, uP or FPGA to a DRAM.

1. To verify mfg process
2. To diagnose fail. The fault/fail will be diagnosed/isolated to the component and to the bad net or pin,
3. To verify timing problem on the net or do an at-speed test to assist with (1) and (2).
Completed Template: BA-BIST Instrument to Memory

<table>
<thead>
<tr>
<th>Given a Memory:</th>
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<tbody>
<tr>
<td>Goal:</td>
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<td>Metric:</td>
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### Assumptions:

- No test point access on these nets.
- Memory has no boundary scan on this interface.
- Board passes ICT power test.
- All analog and low speed IO’s on components can still be ICT tested prior to BA-BIST.
- Board had an unpowered shorts tests of power rails.
- Devices in BA-BIST test have been verified as live - PCOLA is already done.
- Any pins needing termination are terminated according to the chip specification.
- Not proving chip specification, but verifying ‘structure is correct’.
**Completed Template:**
**BA-BIST Instrument to Memory**

<table>
<thead>
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<th>Assumptions:</th>
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<td>Board test assumptions on pre-testing, board state, board config.</td>
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<table>
<thead>
<tr>
<th>Pre-requisites:</th>
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<tr>
<td>Conditions of the board needed to be able to set up and run the BA-BIST</td>
</tr>
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<tr>
<td>To enable a BA-BIST within a chip that is connected to the memory</td>
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**Pre-requisites:**
- Chip is already correctly powered.
- Able to do global reset.
- BA-BIST has access to Address, Data, Control lines,
- Access to JTAG port on chip with embedded instruments.
- Access to compliance pins.
- Ability to deliver Clock. BIST clocks (crystals, clock buffers) provided externally are running.
- Clock frequencies on BA-BIST components are validated before BA-BIST is run.
- PLLs are set up and running.
- Test is able to run outside BIOS.
### Completed Template:
**BA-BIST Instrument to Memory**

<table>
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</table>
| **Dependencies:**| - On other components needed to support BA-BIST function.  
- That these components can be run in a state to support BA-BIST. |
| **Consequences:**|  |
| **Target:**     | Manufacturing test step and debug/diagnosis requirement. |
| **Action:**     | To enable a BA-BIST within a chip that is connected to the memory |
| **Sequence:**   | To write to n-locations using k-data (0, F, 5, A, etc.) in the following address sequence (addr<0>, addr<5>, etc.) |
| **Metric:**     | Test data provides correct diagnosis. |
Completed Template: BA-BIST Instrument to Memory

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**Target #1:**
Manufacturing Test: Provide only pass/fail data.

**Target #2:**
Debug-Diagnosis: Provide data that identifies failing chip, pin or net.

**Target #3:**
Validation-Characterization: Performance fail data with respect to specs.
# Completed Template: BA-BIST Instrument to Memory

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Goal:
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Assumptions:
Board test assumptions on pre-testing, board state, board config.

Pre-requisites:
Access to Address lines, Data lines, Control lines, ability to deliver clock, and Power, access to JTAG port on chip with embedded instrument.

Dependencies:
Links to other chips, tests, or board conditions.

Consequences:
Impact to test coverage, or items not covered by this method.

Target:
Manufacturing test step and debug/diagnosis requirement.

Action:
To enable a BA-BIST within a chip that is connected to the memory

Sequence:
To write to n-locations using k-data (0, F, 5, A, etc.) in the following address sequence (addr<0>, addr<5>, etc.)

Metric:
Fail test data that provides the correct diagnosis can be retrieved.

Complete Template:

```
FAST;
IC( CE, WE, OE, ROW, COLUMN, DATA, BLE, BHE )
II( CE, ROW, COLUMN, DATA, BLE, BHE ) IH( WE, OE );

initialize all signals = 0,
Except Write-Enable, Output-Enable = 1

Data Line Test: Write Address 0 with 5; Read Address 0 for 5
Then: Write Address 0 with A; Read Address 0 for A

Address Line Test: Write Column Address 1 with a 5;
Then: Read Address 1 for a 5
Then: Read Address 0 for an A
Then: Write Address 1 with an A
Then: Read Address 1 for an A
Then: Change Address (Walk a 1 across Address Lines)

Address Line Test: Write Row Address 1 with a 5;
Then: Read Address 1 for a 5
Then: Read Address 0 for an A
Then: Write Address 1 with an A
Then: Read Address 1 for an A
Then: Change Address (Walk a 1 across Address Lines)
```
Completed Template: BA-BIST Instrument to Memory

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**Metric:**

To provide read data associated with failing locations to JTAG TDO port, (or all reads to TDO to allow software to assess mis-comparis/fails).
**BA-BIST to DDR Memory Demo**

**Goal:**
To provide a test that exercises board level nets from FPGA to DDR at speed.

- **BA-BIST Logic**
  - BA-BIST to DDR Memory Demo
  - Data and Complement
  - Read Delay Pipeline
  - Algorithm CTR’s & FSM’s
  - Registered Comparator
  - Addr CTR
  - FAIL
  - DONE
  - RST_OFF
  - BIST_ON

- **FPGA, uP or ASIC used as MMU**
  - Functional MMU Unit
  - JTAG TAPC

- **On-Board Memory**
  - DRAM

- **JTAG Interface**
  - I J T A G

- **PHY Layer**
  - To_Data_in
  - From_Data_out
  - To_ADDR
  - To_Read
  - To_Write

**Goal:**
To provide a test that exercises board level nets from FPGA to DDR at speed.
Assumption:
Can use JTAG in FPGA to run test.

Pre-requisites:
Add JTAG header, access to USB, Tck is supplied.
BA-BIST to DDR Memory Demo

Dependency
Onboard clocks, power and memory

Sequence:
Walk data through each address to isolate bad address or data net.
Memory BIST Example with P1687

Inside the Chip

TAP Controller

Outside the Chip

1149.1 BSDL
P1687 Access Link

P1687 Network ICL

P1687 Instrument ICL

P1687 Instrument PDL

Schematic File of Board

DRAM

DRAM

DRAM

DRAM

DRAM

Chip Signals

TMS
TCK
TDI
TDO

Signals

TCK
TMS
TDI
TDO

TAP Controller

BSR
BYP
ID Code
IR

T
D
R
W

(SIB)

TCK
TMS
TDI
TDO

TCK
TMS
TDI
TDO

M B I S T

Done
Fail
Reset
Run
Algo-Select
Data-Select
Read-Delay

M B I S T

MBIST

MBIST
P1687 End To End BA-BIST Use Model

End-to-End 1687 Ecosystem Support

**Design-Side**
- IP Instruments
- Network Creation
  - RTL-Insertion
  - Network Synthesis
  - Documentation Gen
  - BSDL/ICL/PDL

**IC Test-Side**
- IC Test Generation
- Embedded Instrument
  - Access
  - Vector Retargeting
  - Vector Translation
  - SVF/PDL to STIL

**Board Test**
- Embedded Instrument
  - Access
  - Configuration
  - Vector Retargeting
  - Operation

**Chip Providers**
- EDA Tools

**ATE Testers**
- Translation Tools

**JTAG Testers/ Functional Testers**
Conclusion and Ask

- Defined Industry Usable BA-BIST.
- Proposed Standardization Template.
- Publishing an iNEMI Position Paper.
- Being adopted by EDA and design/system companies.
- Keep socializing concepts and benefits.
- Implement Tools for Next Project Phase?