Boundary Scan Phase 2: Structural Test of External Memory Devices

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Advancing manufacturing technology

Structural Test of External Memory Devices

Basic Project Information

Gap Identified by Boundary-Scan Survey:

- **Over 80% of board test engineers today struggle to implement boundary-scan based connectivity testing on memory devices with no on-chip testability.**
  - **SRAM/DRAM interconnects were cited most often for causing problems when tested with boundary-scan.**
    - 58% said they occasionally encountered problems
    - 28% said they frequently encountered problems
  - **FLASH memory interconnects were the next most cited item.**
    - 62% said they occasionally encountered problems
    - 20% said they frequently encountered problems

Structural Test of External Memory Devices

Basic Project Information:

- **What is "Structural Test"?**
  - **Structural test verifies that a circuit board assembly is assembled correctly – i.e. it's "structure" is correct.**
    - **Short circuits**
    - **Open circuits**
    - **Part presence**
    - **Part orientation/alignment**
    - **Correct part installed (value and/or type)**
    - **Connectivity**

Structural Test of External Memory Devices

Basic Project Information:

- **Equipment typically used for Structural Test verification:**
  - Inspection
    - Solder Paste Inspection (SPI)
    - Manual Visual Inspection (MVI)
    - Automated Optical Inspection (AOI)
    - Automated X-ray Inspection (AXI)
  - Electrical Test
    - In-Circuit Test (ICT)
      - Flying Probe (fixtureless ICT, typically unpowered testing)
      - Manufacturing Defect Analyzers (MDA) – unpowered ICT
      - Powered ICT
    - Boundary Scan (IEEE 1149.x – power applied test)
    - Functional Test (FT – power applied test)

Structural Test of External Memory Devices

Basic Project Information:

- **What is "Fault Coverage" for Structural Test?**
  - Failures, Faults, and Defects
    - A "failure" is a deviation outside the expected parameters of success
      - nonperformance of something due, required, or expected
    - A "fault" is a manifestation of a defect, a flaw
    - A "defect" is an unacceptable deviation from a norm
      - an imperfection that requires remedial action
      - The root cause of a failure!
  - Fault coverage is, given a defined collection of potential structural defects, a measurement of how well your tests will detect those defects.

Structural Test of External Memory Devices

Basic Project Information:

- **Defect detection vs. isolation**
  - **Structural test defect detection – typically "easy" to do – a "failure" symptom is observed**
  - **Structural test defect isolation – very difficult to do at FT, could be many reasons (defects) that can cause the symptom detected,**
    - **Easier and cheaper as you "shift left" through the assembly process**

- **In order to maximize defect coverage and isolation, several of the inspection/test methods must be used.**
  - **None of them alone provide sufficient or adequate fault coverage due to limitations in their respective technologies.**

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Structural Test of External Memory Devices

Basic Project Information:

- **Venn diagram inserted here**
- **Maybe talk about gaps with each type of test**

Structural Test of External Memory Devices

Basic Project Information:

- **Structural test of external memory devices is a "crisis in waiting" as memory devices get larger and faster.**
  - **Loss of standard test point access due to circuit density and signal integrity concerns**
  - **Memory signal/speed timing requirements exceed capability of test equipment**
  - **No "test mode" designed into memory devices to allow easy, straightforward generation of a structural test**

Structural Test of External Memory Devices

Basic Project Information:

- **These issues, individually and in combination, contribute to significant loss of structural test coverage.**
  - **Functional test must take up the slack – at higher cost!**
    - **Functional test debug and repair process becomes much more complex**
      - **Significant reduction in test failure diagnosis**
        - » **Significant debug time added**
        - » **Higher skilled debug technicians/engineers required**
        - » **Additional capital equipment may be required**

Structural Test of External Memory Devices

Basic Project Information:

- **There are several possible solutions via boundary-scan:**
  - **P1581**
    - **I/O loopback test enablement, without adding pins to a device**
  - **Powered Opens @ ICT (Cover Extend/Digital Framescan/Toggle Scan)**
    - **Capacitive opens/shorts testing using Boundary-scan device pins as a driver source.**
  - **Stand-alone boundary-scan based test methods**
    - **Boundary-scan driven memory device test vector generation by boundary-scan test equipment supplier native software.**
  - **Processor controlled test (Control on-board processor via 1149 TAP)**
  - **P1687 (methodology for access to embedded test and debug features via the IEEE 1149.1 Test Access Port)**
    - **Can provide access to external interconnect BIST methods**

Structural Test of External Memory Devices

Scope of Work:

- **Examine and evaluate solutions to the structural test of external memory devices issue and determine what the current and future industry best practices are.**
  - **Feasibility of P1581 to actually help solve this issue**
    - **Standard completion status/schedule**
    - **Evaluate semiconductor industry interest in standard adoption**
      - **Poll semiconductor memory companies**
  - **Evaluate capabilities of existing Powered Opens test solutions**
  - **Evaluate capabilities of existing stand-alone boundary-scan test solutions**
    - **Boundary-scan driven memory device test vector generation by boundary-scan test equipment supplier native software.**
  - **Evaluate capabilities of processor controlled test**
  - **Feasibility of P1687 to actually help solve this issue**

Structural Test of External Memory Devices

Scope of Work:

- **Goals:**
  - Determine and compare pros and cons of potential solutions
  - Identify gaps in technology to structural test memory devices
  - Determine industry Best Practices
  - Increase industry awareness and adoption of P1581 and P1687
- **Output:**
  - Technical paper/whitepaper
    - Summary of evaluations of potential solutions
    - Description of Best Practices
      - Current and Future (5 years out)
  - Presentations at major test conferences
    - IEEE Board Test Workshop
    - International Test Conference

Structural Test of External Memory Devices

Purpose of Project:

- **The 2009 iNEMI roadmap gap analysis determined that one of the greater risks to High Volume Manufacturing (HVM) board test was the continuous erosion of testpoint access due to:**
  - **increasing bus signal speeds**
  - **higher component densities**
  - **shrinking PCB and component form factors.**
- **Situations currently exist where traditional cost efficient structural inspection and test methods can not deliver the necessary structural coverage required.**
- **The frequency and complexity of these situations will continue to increase over time!**

Structural Test of External Memory Devices

Purpose of Project:

- **Evaluate current and potential solutions**
- **Define pros and cons of current and potential solutions**
- **Identify gaps in technology to structural test memory devices**
- **Determine current and future Best Practices for structural test of memory devices**
- **Increase industry awareness of this issue**
- **Increase industry awareness of P1581 and P1687**

- **This project will provide part of a complex solution to the issue.**

Project Plan *Schedule with Milestones*

	Structural Test of External Memory Devices Project	Quarters						
Task		1	2	3	4	5	6	7
	Define Feasibility Studies							
	P1581 Feasibility Study							
	Powered Opens Test Capability Study							
	Stand-alone Boundary-Scan Test Capability Study							
	Processor Controlled Test Capability Study							
	P1687 Feasibility Study							
	Evaluate Results of Capability and Feasibility Studies							
	Document Results of Capability and Feasibility Studies							
	iNEMI End of Project Webinar							
	Presentation at IEEE Board Test Workshop							
	Presentation at International Test Conference							