BIST Project

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Cisco

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APEX 2010
BIST Project - Scope of Work and Phase 1

This project’s focus is on “Chip” Built in Self Test (BIST) study and its promotion for board and system-level applications.

**Purpose of Project**
- Presently, there are no Standard Chip level interfaces or algorithms for Built in Self Test (BIST), which limits the introduction of BIST at board level test. Most “chip” level BISTs are designed to aid IC manufacturing; these algorithms may not be suitable or available to run at the board level.
- The goal of this project is to:
  - develop and promote the adoption of IC BIST at the board/system level,
  - encourage IC vendors to provide standard chip BIST interfaces and algorithms
  - encourage ATE/Instrument providers to develop products based on existing related standards for BIST design. For example, an IEEE 1500/P1687 globalized Test Cost Model useful throughout the industry.
The project is divided into 3 phases:

**Phase 1**
- This phase is being presented as a “standalone project” and will be used as the baseline in defining the second and third phases.
  - This phase is a survey of the industry on current BIST capabilities and future requirements.
  - The goal of this phase is to get feedback from the industry on board level BIST that will assist in fine tuning the scope of Phase 2.
Phase 2:
Per SOW, the second phase is currently comprised of 3 parts:

1. Identification of Chip BIST, which can be migrated to run at board/system-level test.

2. Investigation of BIST tests that enable PCBA testing without or minimal use of fixture/ICT (In Circuit Test) system to lower cost of test and enhance test coverage for high speed interconnects.

3. Promotion of the development of existing related standards for BIST design.
Phase 3 (will take place if the Phase 2 outcome recommends it)

- The development of guidelines and recommendations for a new standard for PCBAs to run BIST tests, and the transfer of the implementation to the appropriate standards body.
# Schedule with Milestones

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<thead>
<tr>
<th>Task</th>
<th>Months</th>
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<td></td>
<td>1* 2</td>
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<tr>
<td><strong>Phase 1 Survey</strong></td>
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<tr>
<td>1.0 Plan the survey</td>
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<td>1.1 Define questionnaire (questions)</td>
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<td>1.2 Define survey hosting and data analysis method</td>
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<td>1.3 Prepare survey recipient list</td>
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<td>2.0 Prepare logistics of survey (post/host survey, notify recipients)</td>
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<td>3.0 Conduct survey / Distribute Questionnaire</td>
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<td>4.0 Collect and analyze data</td>
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<td>5.0 Review/Share survey data with project members</td>
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<td>6.0 Identify the key areas for further discussion</td>
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<td>6.1 Identify data to support scope for items in Phase 2</td>
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<td>7.0 Prepare report of the survey result</td>
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<td>7.1 Internal report for iNEMI Project team</td>
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<td>7.2 Summary report for iNEMI membership</td>
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<tr>
<td>8.0 Phase 2 preparation, project plan, SOW (output from Phase 1)</td>
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*Nov 16, 2009 = month 1 start*
<table>
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<tr>
<th>Name</th>
<th>Company</th>
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<tbody>
<tr>
<td>Zoë Conroy (chair)</td>
<td>Cisco</td>
<td>James Grealish</td>
<td>Intel</td>
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<tr>
<td>Jun Balangue</td>
<td>Agilent</td>
<td>Tony Taylor</td>
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<td>Hui Li</td>
<td>Agilent</td>
<td>TH Tan</td>
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<td>Mark Lau</td>
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<td>Rosa Reinosa</td>
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<td>Zihua Jiang</td>
<td>Alcatel-Lucent</td>
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<td>Arden Bjerkeli</td>
<td>Asset</td>
<td>Skip Meyers</td>
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<td>Bill Eklow</td>
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<td>Jin Wu</td>
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<td>Harrison Miles</td>
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<td>Eric W</td>
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<td>Phil Geiger</td>
<td>Dell</td>
<td>Anthony Suto</td>
<td>Teradyne</td>
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<td>Michael Reagin</td>
<td>Delphi</td>
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Phase 1 Survey

- BIST Survey released Dec 22\textsuperscript{nd}, closed Jan 19\textsuperscript{th}.
- 220 respondents started, 140 completed it
- 42 Questions

Survey Results
1. Survey demographics

- [Bar chart showing percentages for different categories]
- [Bar chart showing categories such as BIST end user, System-level BIST development, IC BIST test development, BIST provider (E.g., ASIC designer), etc.]

- [Additional bar charts for different categories like OEM (original equipment), IC designer, EMS/CIM (electronics manufacturing), ODM (original design manufacturer), etc.]

[INEMI logo]
Phase 1 Survey Question Areas

• What BIST is available, is it proprietary?

• How is it accessed, is board access same as chip, are board designed requesting access?

• What BISTs are used at the board level, are they effective, what test steps, problems.

• How is the coverage, would you like more coverage?

• Future role of BIST and standards.
Gaps and Highlights
What BIST is available, is it proprietary?

- Many different BISTs available at IC and board level.
- Most BIST is designed in house. Some is by 3rd parties and commercial IC provider.
- Designs not consistently implemented across products for IC (63%). Design are consistently implemented for EU (53%) (no 20%).
- BIST is proprietary for IC (yes/some 55/23%), EU(41/16%).
Phase 1 Survey 1st look at Data

Qu: Please indicate what types of IC BIST are used and whether they are available to run at the board level.
Phase 1 Survey 1st look at Data

Qu: Are BIST Tests proprietary to your company?

![Graph showing the percentage of respondents who answered Yes, No, Do not know, and Some are.

Options: Yes, No, Do not know, Some are.}

- Yes: IC: 60%, EU: 60%
- No: IC: 40%, EU: 40%
- Do not know: IC: 10%, EU: 10%
- Some are: IC: 5%, EU: 5%
Gaps and Highlights

How is it accessed, is board access same as chip, are board designed requesting access?

- BIST access is via JTAG or EJTAG (EU@ 82%; IC @90%)
- Board access to BIST mostly same as for IC (IC same/sometimes 54/32%, EU 40/29%)
- Access by dedicated or muxed pins ~ 20-30% of replies (1687 may close gap)
  - This access may also be via JTAG too
  - They may be control pins for BIST enablement
  - May be test pins that become inaccessible at board level
  - May be multifunctional pins with limited access
- Board designers are requesting access to BIST (60%)
- Specific BISTs mostly LBIST, MBIST or IOBIST
- Small amount of functional test still being done instead of BIST
Qu: How are BIST tests usually accessed within the IC?

- JTAG (1149.1 TAP) or EJTAG (emulator JTAG debug port)
- Part of a power-on self-test
- By dedicated test pins
- By IC multiplexed pins (pins are used as another function when in normal application mode)
- Run as part of the application
- Processor control interface (e.g., local bus, IIC, PCI, etc.)
- Other
- Do not know

Bar chart showing the percentage of responses for each method.
Gaps and Highlights

What BISTs are used at the board level, are they effective, what test steps, problems.

- BIST future use for field, SI and performance measurement. Shift from ‘current’ use of test time/cost, ease of test and at-speed test.
- Agree BIST good at catching memory, logic, interconnect, high speed IO defects
- BIST is used at every board test step, would like to use more in field and environmental testing.
- High percentage ‘don’t know’ how much BIST is used at the board level.
- Why BIST is not run at board and system:
  - Strong majority agree major barrier is lack of BIST supporting a standard.
  - Near majority agree few IC devices support IC BIST functions in general.
  - Commercial ICs do not open BIST function to bd/sys users.
  - Description of BIST fn in manual unclear or incorrect.
  - Lack of access when IC is mounted on PCB
  - Lack of bd DFT
Gaps and Highlights
How is the coverage, would you like more coverage?

• Future ICT coverage is not as good as with traditional methods according to survey responses.
• Future functional test BIST coverage is hoped to be high
• Comments on what stops you getting the coverage needed:
  • Educating our board designers to use BIST capable ICs, understanding the cost/benefit return.
  • Educating the business partners.
  • Circuit density and design cycle time / cost; Schedule, Real-estate, $
  • Lack of BIST features.
  • Time and cost add to BIST to IC design.
  • Components with poor test / bist capabilities
  • Designers focus on the performance of cards, not on the test coverage level at the manufacturing level. They are not aware of the improvements that BIST could bring in their validation tests.
  • Design for test requirements in an early stage (mostly ideas/realization pressure come in too late)
Gaps & Highlights
Future role of BIST and standards.

• Do see BIST and bscan as closing structural test lack of coverage gap, but may be need some education on standards.

• Observation: stds are often used before board is fully functional. Need to bring out info before and after board is operational.

• Most see BIST as very important for future coverage and fault isolation and will play a big role in Co’s future test.

• Most actively involved in looking at standard and/or planning to adopt – equally among 1149.7, 1687 and 1581 (some SJTAG and 1532)
**Question:** If standards are established on IC BIST design and its application in board and system level test, what do you think should be standardized?

![Chart showing responses to the question.](chart.png)

- **Access interface and method**
- **BIST description language and files**
- **Compatibility of the interface between different ICs**
- **Interface(s) to instruments and ATE.**
- **BIST instructions**
- **Test algorithms**
- **Other (please specify)**

**Legend:**
- EU8
- IC8
- EU7
- IC7/EU7
Verbatim comments to question: “Explain HOW BIST tests should be standardized”

Answers broke down into 3 areas:

1. Description language, command sets
   - Instruction and description language independent of JTAG as BIST, as also accessed by other means
   - Through description languages and procedures
   - Command set with common high level control command words followed by optional parameters
   - Default command sets and data protocols, Manufacturers can extend beyond the standard but must include applicable defaults from the standard.
   - simple command language
   - All access to IC BIST information should be via XML.
   - Define a description language that allows the description of the access mechanism to the BIST engine(s)

2. Interfaces
   - Chip to chip i/f, as processor vendors not compatible
   - How to get in/out of test mode
   - One standard at interface, connectivity and software so that different types of devices can communicate to one another with same protocols.
   - hardware adapter (TAP) usage across different vendors needs to be standardized.
   - BIST related to DDR3 SDRAM interfaces. These account for a high # of external interconnect on most boards and are difficult/impossible to debug when manufacturing defects (shorts, opens, etc) are present.
   - Both physical interface and instruction sets
   - Start with standard JTAG i/f, provide guidelines for implementation of BIST specific op-codes
### Verbatim comments to question: “Explain HOW BIST tests should be standardized”

#### 3. Leveraging IEEE standards

- P1687 is addressing this issue and should move BIST usage forward.
- Access BIST test results through 1149.1 or .7 TAP. Create BIST Description Language to interact with P1687 ICL code. Treating as an instrument will allow for unique BIST configurations which are call-able through 1149.1 or .7 TAP.
- Formal standards built on 1149.1. The interface must build on what is already available and widely used. BIST should be readily usable, but the actual tests and algorithms may be proprietary.
- Access interface should be compliant to IEEE1149.x, means that test access interface is compatible with different ICs. Everything on list should be standardized to a certain extent by defining a "framework" in which to work. E.g. some BIST instructions should be standardized, such as ones needed for initial set-up and retrieving the results.
- Std that can automate testing (1149.1 defines the Test Data Registers and values, which are different for each IC)
- Same kind as STIL (IEEE 1450)
- IEEE TTSC Standards Working Groups.
## Next Steps and Phase 2

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<tr>
<th>Activity</th>
<th>Date</th>
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<tbody>
<tr>
<td>Continue survey data analysis for key learnings and gaps</td>
<td>March 2010 - complete</td>
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<tr>
<td>Draw up proposals for Phase 2 scope based on survey findings</td>
<td>April 2010 – in progress</td>
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<tr>
<td>Present survey findings and Phase 2 proposals to iNEMI membership</td>
<td>May 2010</td>
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<tr>
<td>Phase 2 preparation, project plan and SOW</td>
<td>May 2010</td>
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