

**iNEMI Statement of Work (SOW)**  
**Packaging TIG**  
**Package Qualification Criteria to Ensure Acceptable Warpage**  
**Performance at 2nd Level Assembly**

**Version 3.0**

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**Basic Problem Statement**

The packaging workshop held in Japan in 2009 clearly identified problems with the existing warpage evaluation criteria for organic package assembly to printed circuit boards. The inadequacy of currently used evaluation criteria constitutes one of the risks to volume manufacturing and field reliability. Many organizations have experienced warpage issues due to improperly formed solder joints. Package component and system board manufacturers are working diligently to establish warpage characteristics using existing methods; however, current methods do not adequately prevent SMT yield issues.

In addition, the definitions of the existing warpage specifications need to be clarified to prevent differences of interpretation. Input from the industry reflects this confusion, with statements such as “package met the coplanarity specification, but still faced low level SMT yield loss” and “there is no robust method to quantify the risk of the warpage characteristic ahead of time until the product is being shipped to the customer in volume manufacturing” being common. The frequency and complexity of these situations will continue to increase over time as new packaging technologies and SMT requirements are introduced.

The scenarios below depict common warpage issues.

Example 1:

- **Package Type** – “Chip Scale” flip chip area array
- **Interconnection Technology** – Flip chip
- **Solder Type** – Pb Free (SAC305)
- **Body size** – Proprietary (not for public disclosure)
- **Product Service Life** – 3-5 years, intermittent operation
- **Failure Type** – System level Accelerated Life Testing
- **Mean Time to Failure** –200-300 hours during qualification testing (primarily during power cycling)
- **Substrate Technology** – Double sided coreless substrate
- **Substrate to Die Ratio** – 1.3/1
- **Failure Rate** – 10%
- **Failure Analysis** – One corner of CSP consistently showed opens
- **Root Cause Analysis** – Large ground circuits in one corner cause package to bow away from system board during reflow; system board warpage determined to be a factor
- **Solution** – Minimize differences in top and bottom layers in offending corner
- **Result** – Corrected ALT issues and subsequent analysis of assembled product shows no sign of marginal joints
- **Qualification Criteria Used** – Unknown/not provided - package qualifications passed with no issues reported

Example 2:

- **Package Type** – BGA
- **Interconnection Technology** – Flip chip
- **Solder Type** – Pb Free (SAC305)
- **Body size** – Proprietary (not for public disclosure)
- **Service Life** – 5-7 years; intermittent operation
- **Failure Type** – Field
- **Mean Time to Failure** – 3000-4000 hours
- **Substrate Technology** – Multilayer laminate core with build-up layer on die surface for signal/ground redistribution
- **Substrate to Die Ratio** – 2/1
- **Failure Rate** – 3-5%

- **Failure Analysis** – Fractured peripheral solder joints causing intermittent opens during operation; system board warpage at failure locations determined not to be significant
- **Root Cause Analysis** – Package warpage at periphery warping away from system board during reflow causing incomplete and weakened solder joints which passed static room temperature and elevated temperature system tests; product passed normal ALT qualification testing
- **Solution** – Adjust manufacturing operation to increase solder paste volume at periphery and reduce solder paste volume in the under die to compensate for package warpage
- **Result** – Field failures due to poor solder joints eliminated
- **Qualification Criteria Used** – Unknown/not provided - package qualifications passed with no issues reported

Example 3:

- **Package Type** – POP, BGA
- **Interconnection Technology** – Wirebond
- **Solder Type** – Pb Free (SAC405)
- **Body size** – Proprietary (not for public disclosure)
- **Service Life** – 5-7 years continuous operation except for routine hardware and software maintenance (system is taken out of service during maintenance)
- **Failure Type** – Manufacturing
- **Mean Time to Failure** – Post assembly test
- **Substrate Technology** – Multi-layer laminate core with build-up layer on die surface for signal/ground redistribution
- **Substrate to Die Ratio** – 1.75/1
- **Failure Rate** – 5%
- **Failure Analysis** – Fractured solder joints in center of package
- **Root Cause Analysis** – Package and system board warpage in opposite directions
- **Solution** – Added additional solder to central pads
- **Result** – Manufacturing failure rates fell within acceptable limits; field reliability data is being collected; no failures occurred during ALT
- **Qualification Criteria Used** – Unknown/not provided - package qualifications passed with no issues reported

As demonstrated by the above examples, current warpage qualification criteria and standards are not adequate to ensure good yield results at 2nd level assembly. There is a definite need to improve the packaging design and subsequent test/modeling/qualification methods to ensure that new packages meet the yield and quality expectations at SMT assembly and in the field. This

project will focus on the criteria for assembled packages and PCBs, which may affect the SMT quality for 2<sup>nd</sup> level interconnects and the subsequent solder joint reliability in the field.

Package qualification criteria to ensure acceptable warpage performance (also known as package warpage criteria) are complicated due to the variety of packaging technologies and the inherent interaction with the system board warpage during the assembly process. In developing the warpage criteria, a partial list of items that needs to be considered is the following:

- Complexity of dependent factors, e.g., package, board, SMT process (flux activation temperature) – knowing all the variables is key to derive the specs suggest to remove this
- Package construction, size and pitch – may show different allowable warpage
- Board construction
- Warpage Measurement and Test methods, e.g., Peak and Valley; warpage shapes
- Preconditioning, e.g., bake effects
- SMT parameters and materials
- Sampling plan from Volume Manufacturing
- Number of reflows and other environmental changes.

There is a need for more discussion/evaluation in these areas in the development of a warpage qualification criterion that can be evaluated.

### ***Scope of Work***

The scope of work for this project will be to examine packages assembled to PCBs and evaluate proposed warpage qualification criteria targeted to meet the current and future needs. This will be a multi-phase project where the analysis and results from one phase will be used to define the project elements of subsequent phases.

Topics WITHIN the scope are:

- Identify and define the basic criteria needed for qualification of organic substrate based packages including the following:
  - Wire Bond BGA packages
  - Flip Chip BGA packages with and without molding
    - Chip Scale Packaging (CSP)
      - Coreless Flip Chip BGA packages with and without molding
    - Package on Package (POP) BGA assemblies
    - Thru Silicon Via (TSV) packages with BGA
    - Embedded Chip BGA Packages
  - Other packaging technologies as identified by the project participants

- Identify and assess the applicability of existing standards including JEDEC, IPC, etc.
- Derive a qualification methodology that can be widely used among the supply chain partners
  - Warpage qualifications involve many other parameters from packaging to SMT processes including the board warpage and other factors that influence the SMT margins.
  - Deriving clean cut go / no go warpage criteria will need to be a function of SMT process windows and other mitigation methods that are commonly used.
- Evaluate potential cost benefits of all possible solutions
  - Use real work scenarios wherever possible to show the potential or actual value-add to each viable solution.

Topics OUTSIDE the scope are:

- The packaging reliability with respect to warpage is not covered here because warpage may not directly translate to stress generated and should be treated separately
- First Level Interconnects that involve internal proprietary assembly processes
- Lead frame based packages

Subsequent project phases will focus on the development and evaluation of the effectiveness of package warpage qualification criteria developed for various package types and on proposed revisions to the current standards on warpage, e.g., JEDEC standard.

An improved or unified warpage qualification methodology is critical to streamlining acceptance criteria across the industry with respect to SMT yield and acceptance. The purpose of this project can be divided into three phases:

### **Phase 1: Establish technical gap assessment**

This phase is intended to provide a baseline in the development of qualification criteria as a partial solution to this complex issue as listed below:

- Evaluate current warpage qualification criteria gap based on existing specification and actual cases – identify the key package design and material characteristics that affect warpage.
- Identify the SMT parameters that interact with warpage (e.g., reflow profile, paste volume, etc.).
- Gathering more information from industry regarding current warpage criteria using on-line survey.
- Identify gaps in the existing measurement tools and analytical calculation to quantify the acceptable warpage and its applicability to represent SMT yield.
- Outline the improved warpage qualification criteria and framework to be developed for Phase 2.
- Identify critical resources and sponsor to support Phase 2 activities.

## **Phase 2: Demonstrate the improved warpage qualification framework:**

- Increase industry awareness of the issues and risks by reporting the survey and the next step needed.
- Develop feasibility study and validate the proposed unified warpage qualification criteria. Evaluate case study to establish the workability of the proposed warpage qualification criteria.
- Evaluate proposed improved measurement methods and analytical tools to describe the SMT yield performance.
- Report out the case study and establish more data points for complete envelope of a given packaging technology.
- Define Phase 3 activities to address different emerging packaging technology like Package on Package BGA packages, Embedded chip BGA package, Thru Silicon Via (TSV) packages with BGA.

## **Phase 3: Extending the applicability of warpage qualification to emerging technology:**

- Establish warpage qualification criteria for emerging technology like Package on Package BGA packages, Embedded chip BGA package, Thru Silicon Via (TSV) packages with BGA.
- Evaluate proposed improved measurement methods and analytical tools to describe the SMT yield performance.
- Report out the case study and establish more data points for complete envelope of a given packaging technology.

## ***Business Impact***

This project will provide the following benefits to participating companies and the industry in general (cost, quality, efficiency gained, resource reduction/savings in people and equipment).

- **Environment Scan:**

Emerging packaging technology demands highly integrated IC design with thinner packages and lower production cost. Such demands can pose significant challenges in managing warpage in large packages with thin substrates. This, in turn, results in higher propensity for defects to occur, which increases the overall cost of PCBA and increases field related incidents. Furthermore, the aggressiveness in down scaling the 2nd Level BGA pitch can reduce the warpage tolerance and increase the risk of SMT adoption. Some cost adders are:

- Additional process development (customized manufacturing solutions focused on problems as they occur) may be required to ensure adequate assembly yields and increased field performance.
- Increasing warpage risk management that can be vital for general adoption in SMT industries.

- Significant increase in the diagnosis of PCBA defects leads to:
  - Additional debug time
  - Higher skilled debug technicians/engineers are required
  - Possible replacement of “good” devices (“shotgun debug”)
  - PCBAs cycle through test/debug/repair process several times
  - PCBAs that are difficult to diagnose will accumulate as scrap
  - Additional customized capital equipment (and attendant production floor space) may be required
- This team will drive to measure average actual Defect per package rates that are being seen at SMT assembly and at subsequent test steps due to warpage with the existing criteria. This will constitute the current state or capability level. The team will then follow through and collect post criteria change data once the new warpage qualification criteria are established and a statistically significant data set has been collected. The difference in these two sets of quality performance data will be the gain made in quality as a result of this project.
- **Tangible Benefit:**  
To align to the environment changes and shorter product development cycle, it is more cost effective to identify potential problems earlier in the design and/or initial package sample test, resulting in smoother NPI ramps, better product quality and prevention of failures. It would be beneficial to derive a unified set of criteria that enable industry to risk assess the performance of the warpage with respect to SMT assembly and field failure risk. This will establish a collaborative environment in which to work on warpage prevention and solving SMT issues prior to product launch.

***Prospective Company Participants***

AkroMetrix	Guangdong Shengyi Sci. Tech
ASE	Hewlett-Packard
Alcatel-Lucent	IBM
Boston Scientific	Intel
Cisco Systems	NGK
Dell	Quanta
Doosan Electro-Materials	Rogers Corporation
Dupont	SEMCO
Fujitsu	Zygo Vision Systems



structures, including PC form factors. Section 5.2.4, refers to “Proper PB design, with respect to balanced circuitry construction distribution and component placement, is important to minimize the degree of bow and twist of the PB.”

- **Standard Practices and Procedures - Reflow Flatness Requirements for Ball Grid Array Packages:** Item 11.2-783 SPP-024A Mar 2009. This document states the procedures for using component land side flatness during simulated reflow as an alternative to coplanarity in certain limited cases for BGA components. Download SPP-024A [not covered POP].
- **Package Warpage Measurement of Surface-Mounted Integrated Circuits at Elevated Temperature:** JESD22-B112A Oct 2009. The purpose of this test method is to measure the deviation from uniform flatness of an integrated circuit package body for the range of environmental conditions experienced during the surface-mount soldering operation. Download JESD22-B112A.
- **Coplanarity Test for Surface Mount Semiconductor Devices:** JESD22-B108A Jan 2003. The purpose of this test is to measure the deviation of the terminals (leads or solder balls) from coplanarity for surface-mount semiconductor devices. Download JESD22-B108A.
- **JEITA ED-7306:** Measurement methods of package warpage at elevated temperature and maximum permissible warpage. This standard stipulates the package warpage criteria and the package warpage measurement methods at elevated temperature for BGA, FBGA, and FLGA.

**Task P1.2 – Assess applicability of existing standards**

- Resources
  - Project team members from participating companies
- Sub-tasks:
  - Analyze capability of each identified standard
  - Provide written summary for each with and pros and cons and opportunities for improvement as outlined in the following table

Existing Spec	Summary	Pros	Cons	Opportunity
Twist and Bow IPC-TM-650				
Thermal Stress, Convection Reflow Assembly Simulation: IPC-TM-650				
Performance Specification Printed Wiring Board, Rigid, General Specification for Dept. of Defense MIL-PRF-55110G w/AMENDMENT 3				
Generic Standard on PB Design 4th Working Draft IPC-2221B				

Existing Spec	Summary	Pros	Cons	Opportunity
Standard Practices and Procedures - Reflow Flatness Requirements for Ball Grid Array Packages. Item 11.2-783 SPP-024A Mar 2009				
JESD22-B112A Oct 2009 Package Warpage Measurement of Surface-Mounted Integrated Circuits at Elevated Temperature				
JESD22-B108A Jan 2003: Coplanarity Test for Surface-Mount Semiconductor Devices				
JEITA ED-7306 Measurement methods of package warpage at elevated temperature and maximum permissible warpage				

**Task P1.3 – Identify tools and test methods that are currently used for warpage qualification**

- Resources
  - Project team members from participating companies
  - Identify common tools currently used.

**Task P1.4 – Assess each tool / test method for its applicability**

- Resources
  - Project team members from participating companies
  - Analyze results and summarize for final report integration

Existing Tools	Summary	Pros	Cons	Opportunity
Shadow Moiré				
BGA Coplanarity Tools				
Dimensional tools like (CMM)				

**Task P1.5 – Produce an interim report summarizing the assessments**

- Resources
  - Project team members from participating companies
  - Prepare summary for final report integration

**Task P2.1 – Develop methodology and format for the criteria, e.g. sample size, preconditioning, variations of material and processes**

- Resources
  - Project team members from participating companies
  - Analyze results and summarize for final report integration

Existing Spec	Summary	Pros	Cons	Opportunity / what is the ideal requirement
Sample size of X				
Sampling methods				
HVM monitoring				
Preconditioning, Bake or No Bake				
Skew Design for simulating extreme distribution behavior				
Peak and Valley				
Temperature Profile used in measuring tool				
Data analysis methods				
Assumptions				

**Task 3.1 – Develop and publish project plan for Phase 2**

- Resources
  - Project team members from participating companies
- Sub-tasks:
  - Prepare Phase 2 project plan for final report integration

**Task P4.1 – Document Results of investigations and present summary to iNEMI membership**

- Resources
  - Project team members from participating companies

## ***Project Monitoring Plans***

This is a Research project, i.e., given an idea or concept, research projects explore and investigate new processes. The outcome is a set of processes that could be used in a production environment if proven to be production worthy. These projects may include some preliminary reliability testing; however, the main focus is on identifying and demonstrating the feasibility of a process.

Project monitoring plans are as follows:

- Ensure open lines of communication among participants
  - Weekly or bi-weekly conference calls as needed
  - Meeting minutes provided through e-mail
  - Follow-up with individuals on an as-needed basis
- Technical review at end of second month.
- Track and document approximate Man-Months per quarter per team member (this will require the active members of the team to provide estimates).
- Track and document approximate number of people on the project per quarter (this can be tracked through iNEMI's WebEx account).
- Project results, including Best Practices Guidelines, test conference presentations, technical papers, end-of-project webinar, etc., will be published on the iNEMI website.

## ***Outcome of Project***

- Technical paper/whitepaper
  - Summary of evaluations of potential solutions
  - Phase 2 project plan integrating the output from the Primary Factors project into actionable set of evaluations to validate the applicability of the criteria identified
- Presentation(s) at major conferences as determined by the project team

## ***General and Administrative Guidelines***

General and Administrative Guidelines for this project and all other iNEMI Projects are documented at [http://thor.inemi.org/webdownload/join/gen\\_guidelines.pdf](http://thor.inemi.org/webdownload/join/gen_guidelines.pdf).