



iNEMI[®]

International Electronics Manufacturing Initiative

iNEMI
Test TIG

Rosa Reinosa
James Grealish
APEX 2008
April 1, 2008

Advancing manufacturing technology

iNEMI Test TIG Agenda

Toll Free: 1 888 727 6732

Toll: 1 719 867 3417

Participant Passcode: 188119

Islander B Room

Meeting Agenda:

10: 00 am – 11:15 am PST Board and Systems Manufacturing Test TIG Meeting
Chair: Rosa Reinoso, Hewlett Packard Company
Co-chair: JJ Grealish, Intel Corporation

11:15 am – 12:00 noon Board Flexure Standardization Project
Chair: Rosa Reinoso Hewlett Packard Company
Co-chair: Alan McAllister, Intel Corporation

12:00 – 12:45 pm Break

12:45 pm – 2:00 pm Boundary Scan Adoption Project
Chair: Steve Butkovich, (Cisco Systems)

Closure



Board & Systems Test TIG Agenda

- **iNEMI updates (Rosa)** • **5 min**
- **Test Project Leadership & Active Participation (JJ, Rosa)** • **5 min**
- **iNEMI Roadmap Update (Mike Reagin, Delphi)** • **15 min**
- **Update from current projects** • **30 min**
 - Boundary Scan (Phil Geiger - Dell)
 - Board Flexure (Alan McAllister - Intel)
 - Functional Test Coverage (Tony Taylor - Intel)
- **Bead Probe Learnings (Paul Berton, Apple)** • **15 min**
- **Other project/topics of interest (All)** • **10 min**
- **Closure**

Board & Systems Manufacturing Test TIG Initiatives Update

- On February 20 the Technical Committee reviewed the proposed “Statement of Requirements” of both the Boundary Scan Adoption and Board Flexure Standardization initiatives and gave approval to these project formation groups to proceed in the development of their SOW and Project Statement documents

Proposed Timelines for Official iNEMI Project Launch

- **Board Flexure Standardization Project**
 1. April 25 - Finalized and Project Formation group approved SOW and Project Statement documents submitted to Technical Committee for approval
 2. May 2 - Approved documents sent out to Membership – Project Sign-up period starts
 3. June 2 – Project Sign-up ends – Project Official Starts

Board & Systems Manufacturing Test TIG Initiatives Update

Proposed Timelines for Official iNEMI Project Launch

- **Boundary Scan Adoption Project**
 1. May 2 - Finalized and Project Formation group approved SOW and Project Statement documents submitted to Technical Committee for approval
 2. May 12 - Approved documents sent out to Membership – Project Sign-up period starts
 3. June 13 – Project Sign-up ends – Project Official Starts

Project Leadership & Participation

- **Current Challenges**
 - project leadership
- **Active Participation**
 - What does this mean?
- **iNEMI membership**

**Test Inspection Measurement
TWG Status Report**

**Mike Reagin
APEX T.C. Meeting
April 4, 2008**



TWG Status Issues

- **TWG Group Participants**

- **2007 Test Inspection Measurement TWG Members**

- Mike Reagin, Delphi (chair) North America*
 - Michael Smith, Teradyne (co-chair) European*
 - Bob Stasonis, Pickering Test European Company
 - Dan Helein, Plexus North America*
 - David Anthus, Jabil North America*
 - Gerald Fitzpatrick, NIST North America
 - James Grealish, Intel North America*
 - Kenneth Parker, Agilent North America*
 - Mike Dewey, GeoTest inc North America
 - Rosa Dolores Reinosa, HP North America*
 - Stig Oresjo, Consultant (Ex Agilent) European
 - Tim Kruse, Plexus North America*

- **Current TWG Status**

- Initial discussions during 2009 Roadmap kick-off in Cupertino on 21Feb08.
 - 2007 TWG Members solicited for participation and feedback on 25Mar08.

TWG Status Issues (2)

- **Chapter Status**
 - **Status of completion**
 - **Still collecting feedback on required updates to 2007 TIM chapter**
 - General Comments
 - Areas of the TIM chapter which need little / no update
 - Areas where the TIM chapter was incorrect
 - Topics which are inadequately addressed / missing from the TIM chapter
 - Industry wide issues
 - Sector specific issues
 - Identify additional individuals which would be willing to provide input to the chapter.
 - **Scheduled meetings**
 - Test Inspection Measurement Roadmap status reviewed with Test TIG on 01Apr08.
 - Test Inspection Measurement Conference Call scheduled for 15Apr08.
 - **Required help to complete**
 - TWG chair (Mike Reagin) will be unable to attend Roadmap Workshop @ iNEMI headquarters (May 14th)
 - Will need to find someone to present update and record participant feedback.
 - **Estimated completion date**
 - Chapter draft to TC before July 1st

TWG Status Issues (3)

- **2007 TIM Chapter Updates that have been identified so far....**
 - **System in Package Testing**
 - **Ability to Test Vacant Connectors and Sockets**
- **Cross Cutting Issues**
 - *Interconnection Substrates*
 - *Digital Silicon Technology*
 - *Board Assembly*
 - *Final Assembly*
 - *Modeling Simulation and Design Tools*
 - *RF Components and Subsystems*
 - *Product Lifecycle Information Management*
 - *Packaging*
 - *Connector*

Format for Test Inspection Measurement TWG Chapter - Cross-Cutting Technologies

- Executive Summary (1 page)
- Introduction
- Situation (Infrastructure) Analysis
 - Benchmark state of art
- Roadmap of Quantified Key Attribute Needs
- Critical (Infrastructure) Issues - Identify Potential Revolutionary Shifts
- Technology Needs:
 - Research, Development Priorities - Grouped Into Categories: Mfg. Processes, Environment & Energy, Systems Integration, Materials and Energy. Category Subheadings; Areas For Innovation, Implementation Tools and Cross Cutting System Issues.
 - Implementation
- Gaps and Showstoppers
- Recommendations on potential Alternative Technologies
- Contributors

Test Inspection Measurement TWG: Changes from previous Roadmaps

- **2002 Roadmap – Looked at Alternative Technologies**
- **2004 Roadmap – Focused on newer technologies**
 - Automatic Optical Inspection (AOI), Automatic X-Ray Inspection (AXI), Boundary Scan
- **2007 Roadmap planned additions:**
 - Coverage of Business Issues related to test
 - Improved coverage of PEG specific test issues
 - Added cost of test as a Quantified Key Attribute Need
 - Discussion of Verification, Validation, versus Manufacturing Testing
 - Chapter will focus on Manufacturing Testing
 - Design Verification, Validation very product specific
 - Impact of new design / process technologies
 - Ability to detect device level defects
 - Difficulty in test development when product defect modes are not easily mapped into a detection strategy (example: what if you can't use current strategies such as AOI or In-circuit Test (ICT) to detect defects)
 - Test may need to be better integrated into the design environment.
- **2009 Roadmap Under Construction**

Test Inspection Measurement TWG: Situation Analysis

- **Overview**
- **Current Design / Test Requirements**
 - Typical Test process flows for PEG products
 - Test Coverage
 - Test Cost
- **PEG Specific Analysis**
 - NetComm
 - Automotive Current Design / Test Requirements
 - Consumer / Portable
 - Medical
 - Office / Large Business

Test Inspection Measurement TWG: Roadmap of Quantified Key Attribute Needs

- ***Lead Edge Electrical Access Trends***
- ***Clock Speed and Serial Data Rates***
- ***Maximum I/O per package***
- ***I/O per cm²***
- ***Leading Edge Boundary Scan Adoption***
- ***Leading Edge Built in Self Test Adoption***
- ***Product Mechanical Interface / Fixturing Requirements***
- ***Cost of Test***

Test Inspection Measurement TWG: Critical Issues

- ***Cost of Test***
- ***Test Coverage, Defect Detection / Prevention***
 - ***High Density Interconnect***
 - ***Smaller Vias, Blind Vias, Buried Vias, Higher layer counts***
 - ***Embedded Components***
 - ***All the above source of reduction in test access***
- **Issues associated with outsourcing of functional test development**
- **OEM ability to proactively evaluate test coverage effectiveness at supplier / remote site in real-time**
- ***Global Test Development / Implementation***
 - **Common Solutions versus regional solutions**
 - **Training and support issues**
 - **Impact of tariffs and regulations on test equipment costs**
- ***Lead free Impact on Test***

Test Inspection Measurement TWG: Technology Needs

- **Metrology for Nanotechnology**
- **Tools that help identify mapping between component level faults and system (functional) testing**
- **Tools that integrate test development with product development similar to those in the IC world.**
- **Ability to probe on smaller vias**
- **Ability to test vacant connectors and sockets**

Test Inspection Measurement TWG: Cross Cutting Issues Discussion

- ***Overview***
- ***Interconnection Substrates***
- ***Digital Silicon Technology***
- ***Board Assembly***
- ***Final Assembly***
- ***Modeling Simulation and Design Tools***
- ***RF Components and Subsystems***
- ***Product Lifecycle Information Management***
- ***Packaging***
- ***Connector***

Test Inspection Measurement TWG: Gaps and Showstoppers

- ***R&D Funding for new TIM Technologies***
 - *Source of funding*
 - *Protection of intellectual property*
- ***Solutions for SIP testing***
 - *IC Test problem?*
 - *Board Test problem?*
- ***Capital Equipment Cost***
- ***High Speed Signal Testing***
- ***Test Fixturing Design***
- ***Test technologies to address product miniaturization***



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www.inemi.org

Email contacts:

j.michael.reagin@delphi.com

michael.j.smith@teradyne.com

iNEMI
Boundary Scan Adoption
Project Status

Philip B. Geiger
APEX 2008
April 1, 2008



Current Status

- **What has been done so far....**
 - **Proposed Boundary Scan Adoption Project under the Board and Systems Manufacturing Test TIG**
 - **Preliminary SOW generated**
 - **Project phases defined**
 - **Collected initial input for survey of Boundary Scan users/developers**
- **What is being done now and in the near future**
 - **Finalize the SOW**
 - **Develop Boundary Scan Survey**
 - **Recruit members for the Boundary Scan Adoption Project to get the widest possible industry representation**

Boundary Scan Adoption Project

Phase 1

- **Survey users of Boundary Scan devices and development tools and identify the current level of Boundary Scan implementation, use in the industry today, and projected short term future use.**
- **Gather ideas / Brainstorm**
- **Share available data from participating companies**
- **Identify areas of focus**
- **Develop Results/Output in White Paper**

Boundary Scan Adoption Project

Phase 2 and 3

- **Phase 2**
 - Identify areas where the electronics industry needs to see improvement in Boundary Scan implementation
 - Define “compliance” for .bsdl files
 - Define methods for encouraging .bsdl file compliance
 - Develop Results/Output in White Paper
- **Phase 3**
 - Define follow-on projects/next steps

Board Flexure Project Update (Alan McAllister)



Functional Test Coverage Assessment Project

Speaker Name
APEX 2008
April 1, 2008



Agenda

- **Status**
- **Evaluations**
- **Schedule**
- **Summary**

Status

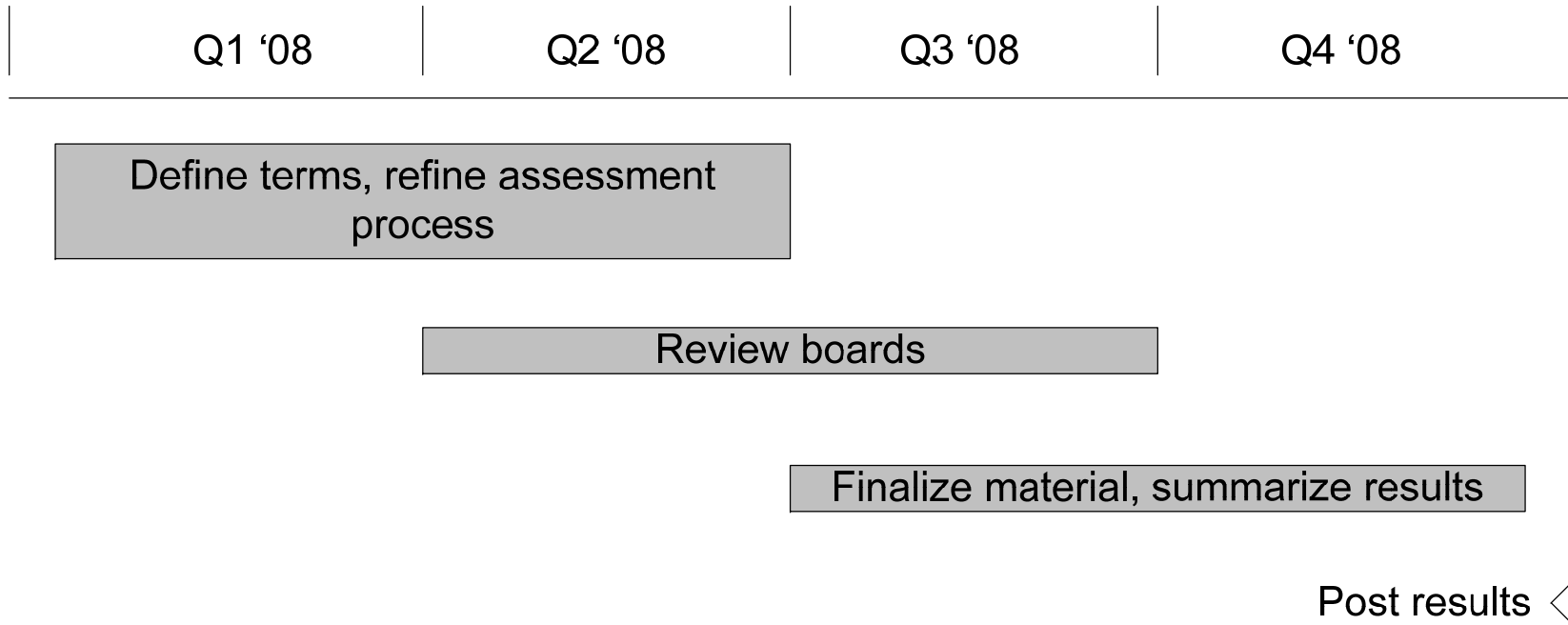
– Status

- **Project participants are taking ownership of defining terms and processes of the functional test coverage assessment process**
 - **Examples:**
 - » **What is a feature vs. a functional block? How will these definitions be used to create a list of items that will be assessed for coverage?**
 - » **At-speed testing: How many speeds should be tested? How is this definition used to assess coverage?**
- **Material is reviewed bi-weekly in the project team conference call**
- **After reviewing all material in group meetings, boards will be evaluated using the defined process**
 - **Currently two boards are slated for review: one from Boston Scientific, one from Intel**

Evaluations

- **Several boards will be reviewed by the group using the proposed coverage assessment process**
 - **Team is ensuring IP concerns are addressed**
 - **Terms and processes need to stabilize prior to using for the board assessments**
 - **Using the process will be key to understanding the advantages and disadvantages of what the team creates and provide opportunity to fine tune prior to releasing outside the project team**

Schedule



Summary

- **Still a lot of work to do in finalizing material**
- **Boards reviews will hopefully provide an opportunity to exercise the assessment process and help tune the usability**

Bead Probe Learnings (Paul Berton)

Other projects/topics of interest

Closure

- **Thanks for attending**
- **Would like to encourage project participation**
- **Contact David Godlewski to get on specific project distribution list [dgodlewski@inemi.org]**
- **Questions??**