

**iNEMI Statement of Work (SOW)
Board & Systems Manufacturing Test TIG
iNEMI Boundary Scan Adoption Project**

Version # 3.0

Date: May 8, 2008

Project Leader: Steve Butkovich, Cisco

Co-Project Leader:

iNEMI Coach:

Basic Project Information

Background

Increasing circuit densities and speeds are quickly reducing electrical test point access for printed circuit assembly test. Boundary scan is a technology which will allow continued testability of printed circuit assemblies, but its use requires that it be designed into semiconductor devices. Currently not all semiconductor vendors support boundary scan, or they do so incorrectly, or they use flawed tools to implement their designs, or they lack industry-approved and proven processes for verification.

Wider availability of complying devices is necessary to enable cost efficient and effective board test for future designs. In addition, tools to support boundary scan based test need to be developed and integrated into manufacturing test equipment.

Purpose of Project

Promote wider adoption of boundary scan (for example: IEEE 1149.1, 1149.6, P1581 and others) throughout the industry. Encourage semiconductor vendors to include the technology in their products. Promote the development of tools by ATE vendors to support boundary scan based board test. Promote the development, refinement and adoption of synthesis and verification tools to assist in implementing to the standards.

Prospective Participants

- Semiconductor manufacturers
- Original equipment manufacturers
- Contract manufacturers
- Other: Reliability engineers, manufacturing engineers, test engineers, research and development, quality assurance, procurement, standards bodies

Project team members are expected to participate by sharing knowledge on board flexure and FA methods. The team will draft a recommendation for the IPC/JEDEC committee on proposed changes or additions to the current standards.

Project Formation Participants:

Agilent	Ken	Parker
Alcatel-Lucent	Chen-Huan	Chiang
Alcatel-Lucent	Brad	Van Treuren
Apple	Paul	Berton
Apple	John	Martin
Apple	Bob	Oakes
ASSET InterTech, Inc.	Adam	Ley
ASSET InterTech, Inc.	Alan	Sguigna
Boston Scientific	Max	Cortner
Cisco Systems Inc.	Steve	Butkovich
Cisco Systems Inc.	Zoe	Conroy
Cisco Systems Inc.	Varoujan	Malian
Cisco Systems Inc.	Thomas	Wong
Corelis	Andrew	Levy
Dell Inc.	Philip	Geiger
Dell Inc.	Eddie	Maruri
EMC Corporation	Mark	Bisceglia
EMC Corporation	Jeffrey	Moore
EMC Corporation	Dave	Nelson
Flextronics	Victor	Orona
GOEPEL Electronics	Heiko	Ehrenberg
Guidant	Max	Cortner
HP	Jay	Blue
HP	Fred	Hartnett
HP	Skip	Meyers
HP	Carlos	Michel
HP	Rosa	Reinosa
Huawei	Victor	Chen
Huawei	Li	Yingwu
Huawei	Xu	Zhen
Huawei	Chen	Quang
IEEE	Steve	Scheiber
Intel Corporation	Victor Marc	Casas
Intel Corporation	Kevin	Daverin
Intel Corporation	James	Grealish
Intel Corporation	Binh Ngoc	Nguyen
Intel Corporation	Marc	Pepin
Intel Corporation	Tony	Taylor
Intel Corporation	Bill	Van Dick
JTAG Technologies	Anthony	Sparks
KLA Tencor	Nimesh	Shah
National Instruments	Adam	Gage
Sanmina-SCI	Mitchell	Roberge
Sun	Leon	Yang
Teradyne	Alan	Albee
Teradyne	Charles	Robinson
Test Research, Inc.	Floyd	Conner

Test Research, Inc.	Paul	Lin
Test Research, Inc.	Jeff	Lin

Scope of Work

Phase I

Conduct Industry Survey

- Survey users of Boundary Scan devices and board test development tools. Identify the current levels of Boundary Scan implementation, used in the industry today, and projected short term future use, for example:
 - Processor
 - Chipsets
 - Memory
 - Video
 - Programmable Logic Devices
 - Other Boundary Scan devices
- Gather ideas / Brainstorm
- Share available survey data from participants
- Identify areas of focus
- Develop Results/Output in White Paper
- Present Results to iNEMI Membership – Webinar
- Present Results to industry – APEX 2009 – Paper - Presentation

Phase II

- **Initiate project based on results of survey**
 - Present Phase II project's SOW to Technical Committee for Review February 2009
 - Proposed Scope of Work:
 - Define total “goodness” of Boundary Scan Description Language (BSDL) files
 - Develop Results/Output in White Paper
 - Survey users of Boundary Scan devices and board test development tools. Identify the current levels of Boundary Scan implementation, used in the industry today, and projected short term future use, for example: Processor

Project Plan

Schedule with Milestones

Phase 1	May-08	Jun-08	Jul-08	Aug-08	Sep-08	Oct-08	Nov-08	Dec-08	Jan-09	Feb-08	Mar-08	Apr-08
Duration 11 Months												
Create Boundary Scan survey		X										
Survey users of Boundary Scan devices and board test development tools			X	X	X							
Analyze survey results						X	X	X				
Share survey data with team/identify areas of focus									X			
Report results in white paper										X		
Present Results to iNEMI Membership – Webinar											X	
Present Results to industry – APEX 2009 – Paper – Presentation												X
Phase 2	Feb-09											
Duration TBD												
Initiate project based on survey results – Present Phase II project’s SOW to Technical Committee for Review February 2009	X											

NOTE: All changes to SOW must be approved by the TC (version control)