System in Package: Identified Technology Needs from the 2004 iNEMI Roadmap

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The New Volume Drivers for the Electronics Industry

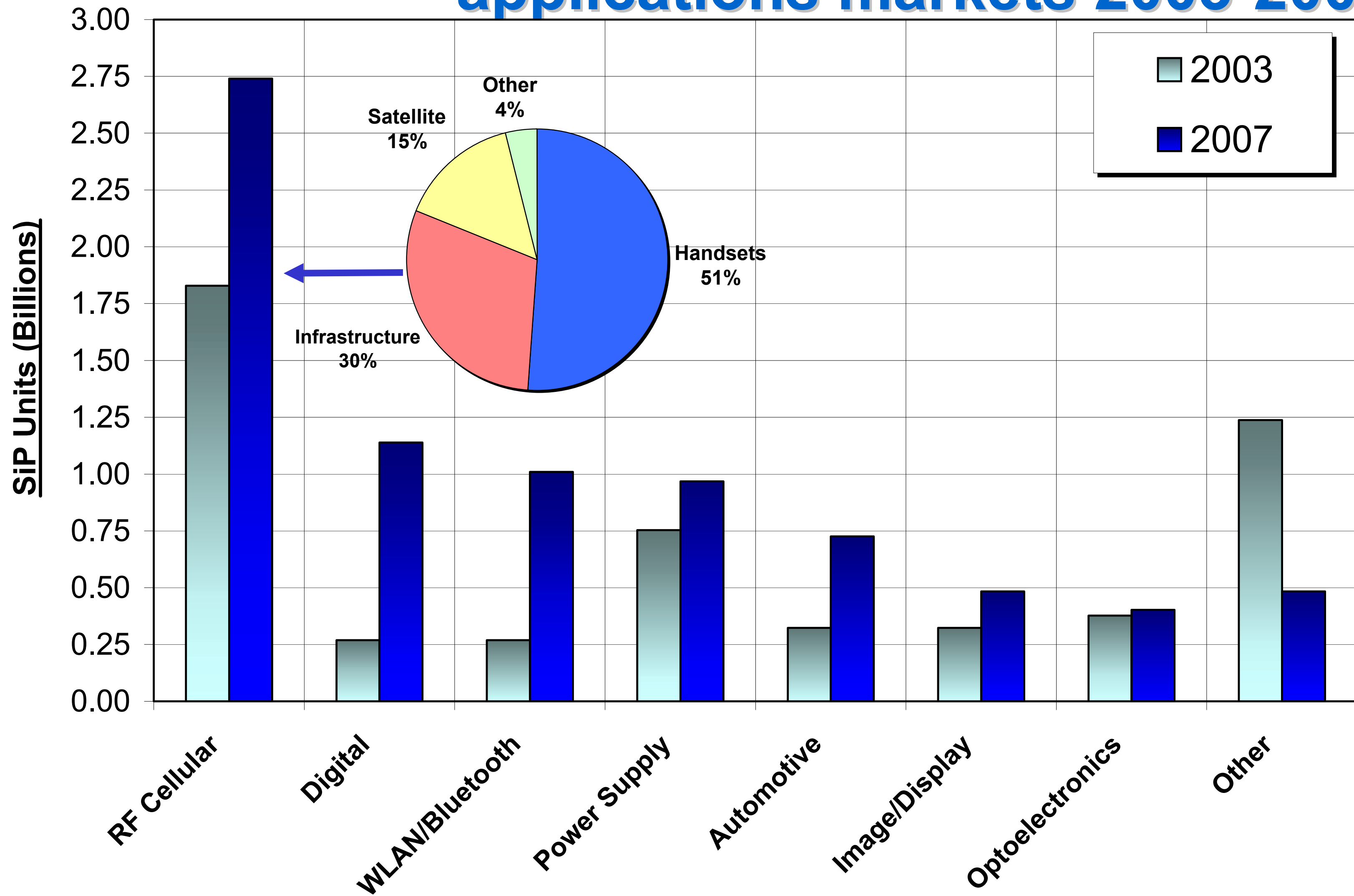
- Communications products continue to replace computers as key driver of volume manufacturing.

- New products, enabled by new technologies, are creating a pronounced shift in the industry:
  - Blurring of the lines: computers & communications
  - Cell phone market growth
  - Emergence of Wireless Products (Bluetooth, 802.11)
  - Optoelectronics – long term
  - Automotive electronics (adding functionality of home & office to your car).

The Changing Landscape

- New Volume Drivers
  - 1 billion cell phones by 2007/8 likely
    - Cell phone innovation slowdown has led to standard I/C's and commoditization of the technology
    - Cell phones will overtake PCs as the tool for web access by 2006
    - 2 billion Bluetooth Devices by 2007 forecast
  - Optoelectronics growth stopped through 2003
    - Isolated areas of strong growth emerging
  - PC growth resuming, market share shifting
  - Automobiles increasing electronics content

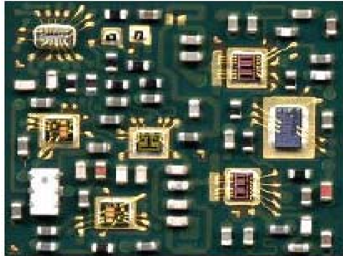
Projected growth for SiP in key applications markets 2003-2007



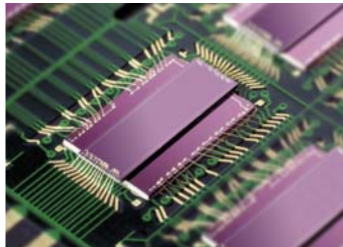
Sources: Prismark (primary), Deutch Bank, Credit Suisse First Boston, Allied Business Intelligence.

SiP Technology Definitions

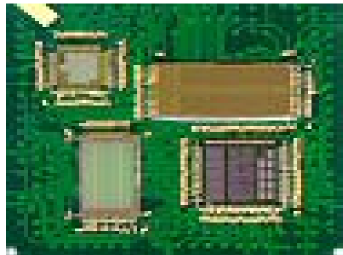
SiPs are segmented into four technology types: Modules, Stacked-Die, MCM, and 3D packaging



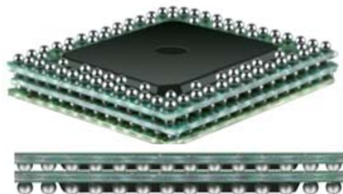
(1) Module: **Any fully-functional subsystem package (LGA, BGA or PGA type) consisting of a substrate (laminate, ceramic, flex or lead-frame), one or more die, chip-level interconnects (wire-bond or flip-chip), integrated or surface-mounted passive and active components, and a protective casing (shield, lid, over-mold etc).**



(2) Stacked-Die Package: **Any standard package format incorporating two or more vertically-stacked die, chip-level interconnects (wire-bond or flip-chip) on a laminate, ceramic, flex or lead-frame substrate.**



(3) Multi-Chip Module (MCM): **Any standard package format incorporating two or more horizontally-arranged die, chip-level interconnects (wire-bond or flip-chip), and optional passive components on a laminate, ceramic, flex or lead-frame substrate.**

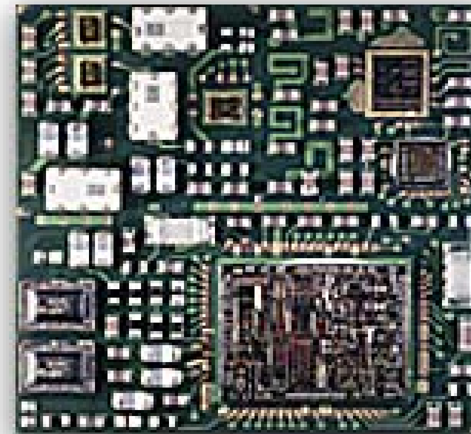


(4) 3D Packaging: **Any combination of standard pre-packaged devices or components using laminate, ceramic, flex or lead-frame substrates stacked vertically with package-level interconnects (LGA, BGA, PGA etc).**

System in Package Highlights

- **The broadest adoption of SiP has been for stacked memory/logic devices and small modules (used to integrate mixed signal devices and passives) for mobile phone applications**
- **SiP provides more integration flexibility, faster time to market, lower R&D cost, and lower product cost for some applications than SOC.**
- **Infrastructure issues facing SiP implementations include:**
  - **Need for low cost higher density substrates**
  - **High speed simulation tools for electrical and mechanical analysis**
  - **Lower cost Wafer Level Packaging**
  - **Lower cost Assembly Equipment**
  - **Lower cost improved materials for encapsulation**
  - **Skill set and business models vary for EMS/SAS**

Example of a module based SiP with radio functions for a GSM mobile phone radio



SiP - Situation Analysis

- **Market: In 2004, 1.89 Billion SiPs are expected to be assembled. By 2008, this number is expected to reach 3.25 Billion, growing at an average rate of about 12% per year.**

- **Technology: SiP applications have become the technology driver for small components, packaging, assembly processes and for high density substrates.**

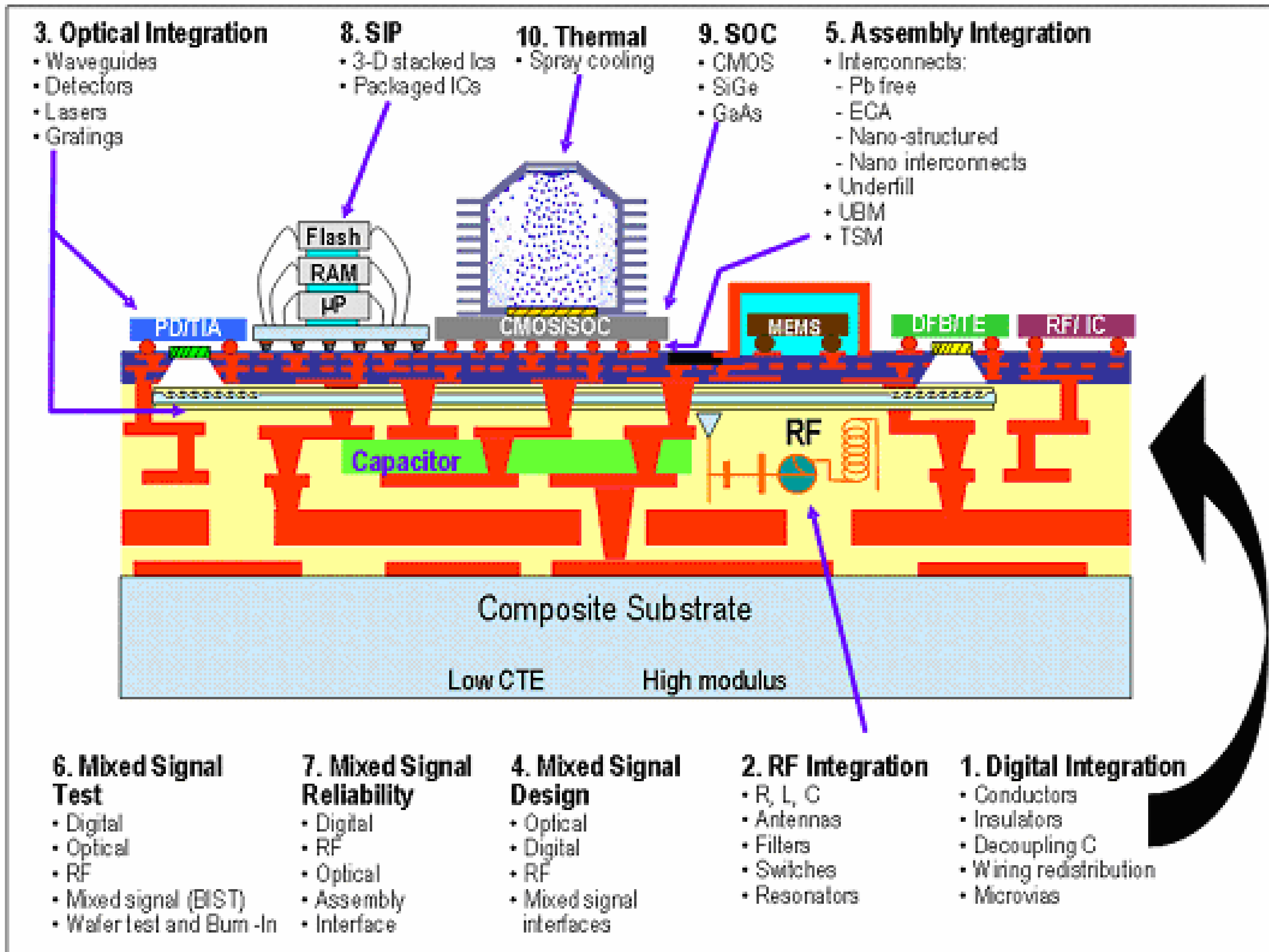
- **Growth: System in Package (SiP) has emerged as the fastest growing packaging technology segment although still representing a relatively small percentage of the unit volume.**

SiP - Situation Analysis

- **System in Package (SIP) architectures (based on both organic and ceramic substrate materials) have been developed and are now in full production.**

- **This same architecture, with capability for buried cavities and channels, allows for MEMS device construction with a variety of new applications in Fuel Cells and Life Sciences (DNA/Blood testing).**

Vision of the Evolution of SiP



Source: Professor Rao Tummala, Georgia Institute of Technology-Packaging Research Center.

SiP Critical Requirements Forecast

System In Package (SiP) Critical Requirements Forecast											
Year of Production	**2005**	**2006**	**2007**	**2008**	**2009**	**2010**	**2011**	**2012**	**2013**	**2014**	**2015**
Number of Terminals-Max MCM	2000	2000	2000	2000	2000	2000	2000	2000	2000	2000	2000
Number of Terminals-Max RF Module	80	100	120	140	160	160	160	?	?	?	?
Max number of stack die	7	7	7	7	9	9	9	9	9	9	9
Max number die in Module	10	10	10	8	8	8	6	6	6	6	6
Minimum Component size in.	0201	01005	01005	01005	01005	01005	01005	01005	01005	01005	01005
Embedded Passives in Laminate	L	CL	CL	CL	CL	CL	CL	CL	CL	CL	CL
Embedded Passives in Ceramic	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C
MSL Level	2a	2a	2a	2	2	2	2	2	2	2	2
Max Reflow temp C	260	260	260	260	260	260	260	260	260	260	260

Table taken from the NEMI Roadmap for 2004, Page 6, Product Emulator Groups, System in Package (SiP) Product Section

Strategic Concerns

- The segmented supply chain is leading to non-optimized cost effective packaging solutions and delaying the introduction of technology.
- The present materials supplier base does not have adequate demand (at a high enough sales revenue) to drive many of the needed new R & D materials developments.
- The mechanisms for cooperation between industries and among researchers working in all advanced technologies must be strengthened.
- Cooperation between OEMs, EMS Firms, and component suppliers is needed to focus on the right technology and to find a way to deploy it in a timely cost effective manner.

Recommendations

- The rapid market growth and technology advancement in RF subsystems is constrained by the pace of research and development of new designs, design tools, materials, and manufacturing processes for semiconductors, SiPs, RF components, and RF MEMS. Government, consortium, and academia needs to focus funding to address these research and development needs.

- Improved design tools for emerging technologies like embedded passives and optoelectronic PWBs.

- Development of automated printing, dispensing, placement, and rework equipment capable of the finer pitch requirements for SiP package assembly at current process speeds.

Recommendation and Next Steps

- Development of Low cost, higher thermal conductivity, packaging materials, such as adhesives, thermal pastes, and thermal spreaders.
- Development of new approaches to organic substrate fabrication which address needs for dramatic increases in density, reduced process variability, improved electrical performance, and radical reductions in cost.
- Establish an iNEMI SiP Technology Implementation Group (TIG) to develop a research and development plan for closing the SiP gaps identified in the roadmap
    - Met Wednesday Morning at APEX

- Presentations by attendees on their interests and needs
- Chair: Joe Adam, Skyworks
- Developed focus areas for Gap Analysis
  - Reliability
  - Substrates
  - Materials
  - Equipment
  - Design Tools
  - Standards
- Next Steps
  - Attract additional participants
  - Fill in Gap Structure
  - Prioritize Gaps

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Helping you connect with and strengthen your supply chain

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