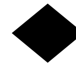
NEMI Cost Analysis: Optical Versus Copper Backplanes



Presented on behalf of project members by Adam Singer

ECWC / APEX

February 22, 2005

OE TIG Projects

Optoelectronics Substrates Project

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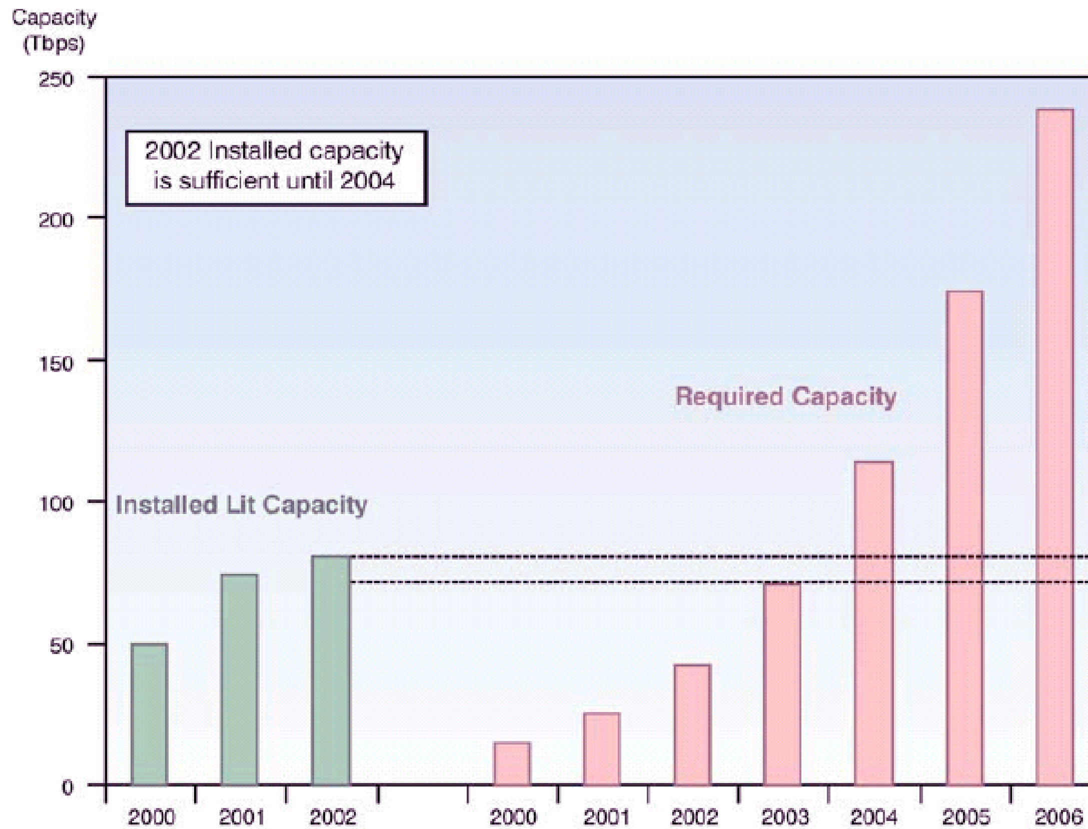
Agenda

- Background / reason for iNEMI project
- Updated goal
- Status report
  - Cost modeling
  - System descriptions
  - Optical connector challenges
  - Optical waveguide technologies
- Conclusions

OE Trends & Drivers

- Starting to see OE equipment revenue growth, e.g. access & FTTP, PONs
- Traffic continues to grow 50-100% pa, triple play (data, VoIP, video), retail, file swapping...
- Distributed systems (1000s servers) require high speed interconnects
- Copper can support up to 10G over 1m, 40G in some cases, at increased cost: mtrls, line spacing, signal conditioning...
- Emerging OE technologies: reconfigurable/active systems, polymer waveguides & substrates, Si optical emission & modulation (Intel), optical band gaps...
- Although fiber interconnects will be continue to be used, optical functions, initially transmission, will co-exist with electrical in the printed wiring board
- COST reduction of pkg, assembly & test, remains significant driver

Market Status

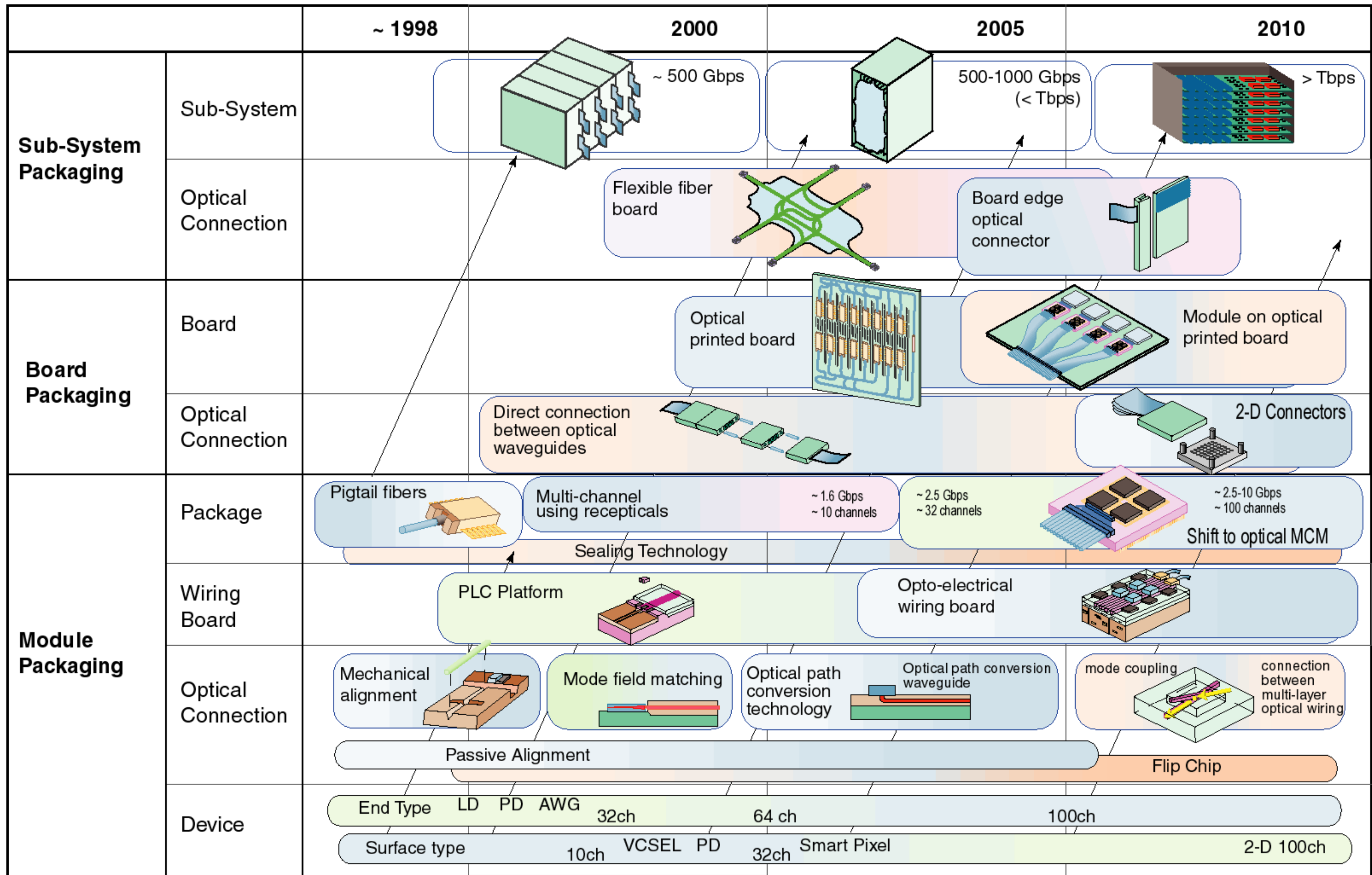


Courtesy of Prismark, September 2002

Current Interconnect Bottleneck

- Increasing chip-performance leads to problems with conventional electrical intrasystem interconnection technologies (Siemens SBS C-LAB, 2002):
  - Increasing electromagnetic radiation
  - Limited bandwidth due to high frequency skin effect
  - High pin-count through limited bandwidth
  - Increasing signal integrity and timing problems
  - Increased data rate leads to disproportional increased costs per bit
- Transmission speeds reach their physical limits when power consumption is increased and there is no obvious increase in the propagation speed
- It is the ability of optical interconnections to operate at high data rates (>2.5 GHz) with superior signal integrity that makes them an exploitable alternative

JIEP Optical Packaging Roadmap



Source: Japan Institute of Electronics Packaging & SEMI

CONNECT WITH AND STRENGTHEN YOUR SUPPLY CHAIN

Copper Roadmap

Generic Copper Backplane Bandwidth Technology Roadmap

		1 Gbps — 2.5 GBPS — 3.125 Gbps — 4.0 Gbps — 6.125 Gbps — 10 Gbps - 40Gbps					
PCB Technology	Materials	FR-4, Df = 0.020	PPO / CE, Df = 0.015-0.008	BT / APPE, Df = 0.010	PTFE, Df = 0.009 - 0.003	PTFE / Ceramic,	Df = 0.002 - 0.0009
	Processes	Standard processes	Backdrilling — Dual density drilling?				
	Transmission Line Design	Single transmission line, Length management	Differential pair, length, type (Surface microstrip, embedded microstrip, stripline, edge coupled, broadside coupled), location in stack				
	Via Design	Decrease PTH diameter, Remove non-functional pads, Increase anti-pad diameter (Clearance ring)					
	Connector Launch Design	Pad in via or PTH, micro vias, buried vias					
Connector Technology	Teradyne connectors	HDM	VHDM & VHDM L-series	VHDM-HSD	Gbk	GBx	
	ERNI connectors	ERmet	Ermet	Ermet ZD	ERmetZD	Ermet Zero XT	
	Tyco connectors	HM-ZD	Z-Pack HM-ZD MultiGig RT-1	Z-Pack HM-ZD	MultiGig RT-2	MultiGig RT-3	
	FCI	Metral 2000	AirMax VS Metral 4000	AirMax VS	AirMax VS	AirMax	
	Fujitsu		FCN-261Z00x		FCN260D		
	Winchester		Xcell			SIP-1000 I platform	
	Molex	Molex is a Teradyne licensee					
Receiver / Transmitter Signal Conditioning Chip Set	Taps required	None Required		One	Two	Multiple	
	Velio		GigaCore		GigaCore2		
Bus Architecture		Shared Bus ? Point to Point ? Multi point ? Sub type?					

Optoelectronics Concepts

Photons

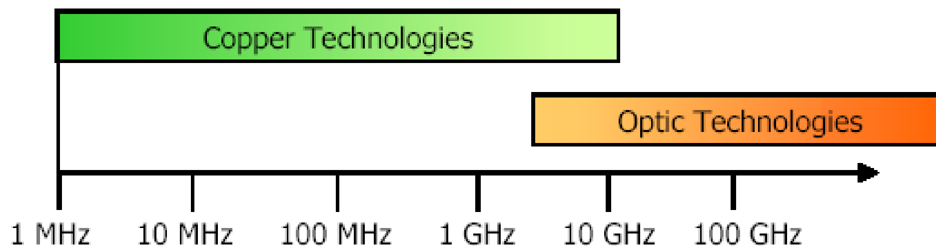
- **Zero Rest mass**
- **FxD > 10^{14} Hz x 100km**
- **Boson => Mult. Signals**
- **OE Conversion needed**

Best for long distance, high speed

Electrons

- **9.11 x 10^{-31}kg**
- **FxD > 10^{10} Hz x 0.001km**
- **Fermion: One Signal**
- **No OE Conversion**

Best for very short distance (<5 meters) at moderate to high speed



Original Purpose Statements:

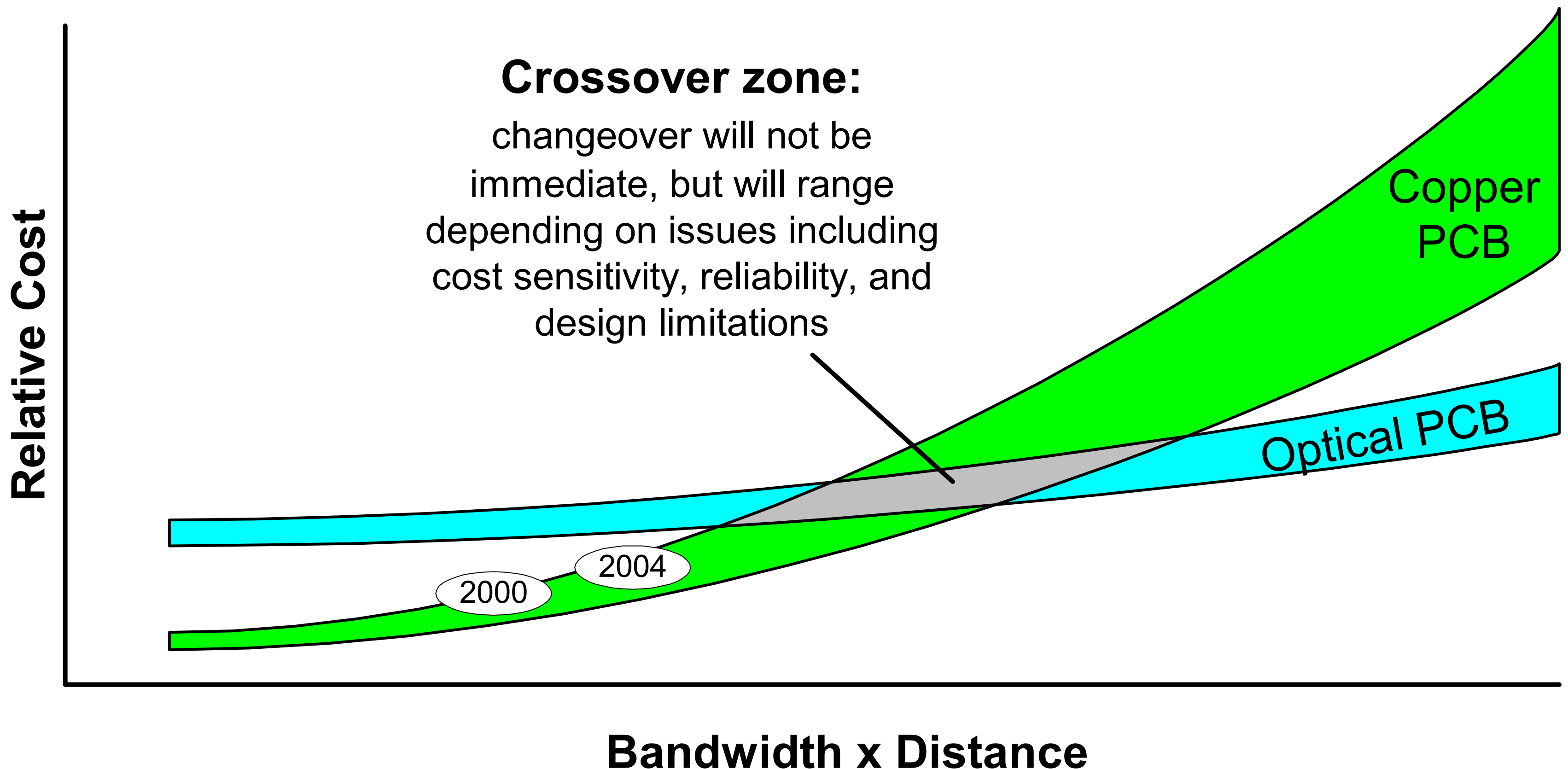
- This purpose of this group is to addresses the implementation of optical and optoelectronic technologies in printed wiring boards (PWB's) used for packaging, or for other applications.

The areas to be addressed include:

- An understanding of the drivers and the constraints of producing optoelectronic PWB's including cost analysis and tradeoffs.
- Design considerations for materials used for PWB fabrication and assembly, including material properties
- Manufacturability of waveguides and the integration of waveguides in PWB's
- Component mounting and interconnecting structures
- Performance and testing of waveguides and connector attachments

Optical Backplane Cost

Cost-performance is the key driver; we need an industry metric to compare optical vs. Cu-based, e.g. $/(Gb/s/channel/m)



Current Statement:

- Initial investigation (2002) indicated that the OEMs were not planning to use optoelectronics in their next generation machines
- The OEMs were all working on internal analysis of optoelectronic solutions and were all interested in participating in a NEMI technology analysis activity
- There are numerous estimates of how far copper can be pushed to increase data rates. The estimates range from 2.5 Gb/s to 40 Gb/s.
- It was decided to do a business analysis of copper vs. optoelectronics
- The product to be analyzed will be a communications industry backplane, e.g. Terabit router

Optoelectronics Substrates Project

- Project Objectives:
  - Develop cost models, including assembly and test, of a high performance "product" (black box emulator)
  - Copper and optical backplane versions
  - Run cost models for various speeds and system configurations, using appropriate sets of components and technologies

- Project Benefits:
  - Information exchange between suppliers (component, technology..), assemblers and system OEMs
  - Define industry relevant cost-performance metric(s)
  - Identify technology gaps and barriers to implementation
  - Roadmaps and cost models will be available for industry use

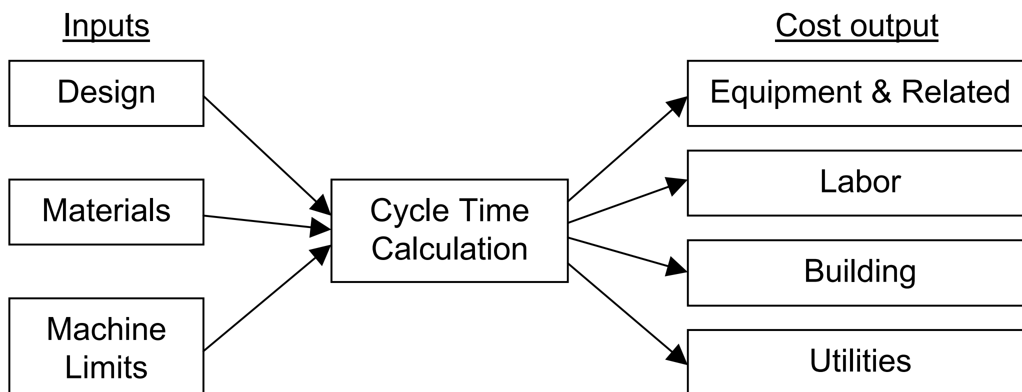
- Meeting Objectives:
  - Report work-in-progress
  - Promote awareness, attract new participants

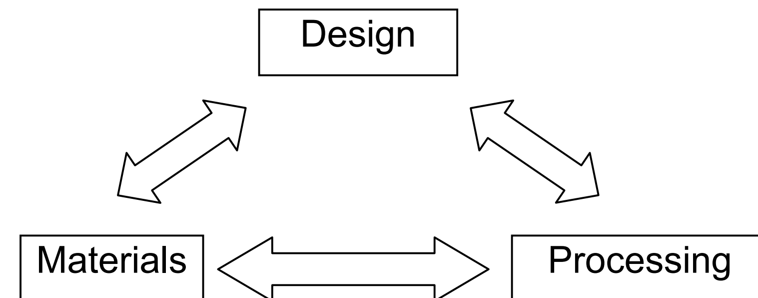
Optoelectronics Substrates Project

- Project started in June 2003, in open/forming stage
- Bi-weekly telecons
- Very good participation
  - Several OEMs, fabricators, CMs, material suppliers
- First pass output of copper backplane model run and validated by 3 fabricators
- Draft electrical technology road map,1-10(40) Gbps, includes connectors, signal conditioning, chip-sets and high performance substrates
- Starting to develop connector input to the model
- Discussing the optoelectronic technology alternatives
  - Fiber, Waveguide, Polymer
- Developing list of optical attributes and performance issues
- Draft optical roadmap by June

Cost Modeling Method

- Based on Technical Cost Modeling, as developed by IBIS Associates / MIT
- Activities Based Costing, plus engineering relationships
  - Assembly cycle time = f(design, mtrls, equipment)





iNEMI

Electrical Backplane Cost Model

Context

- North American facility
- Equipment assumes max 24 inch width conveyors
- Yields reflective of 8 mil line / space
- Drilling reflects 20 mil minimum diameter
- Medium throughput (350Ksqft/yr top surface)

Product

- 32 metal layers, no buried vias
- FR-4, 24x20 inch panel, 20x18 inch finished board
- 5,000 drilled holes per board
- ~1-3 Gbps performance

Back Plane Cost Model

Microsoft Excel - PCB Model v4

File Edit View Insert Format Tools Data Window Help Acrobat

A1 =

	A	B	C	D	E	F	G	H	I
1									
2	DESIGN ISSUES								
3	Product Name	Cu backplane			PROD				
4	Annual Production Volume	117	(000) board per year		VOL				
5								Other assumptions:	
6	Panel Length	24	inch		PLEN			8	mil lines
7	Panel Width	20	inch		PWID			8	mil spaces
8								20	mil minimum drill diameter
9	Finished Board Length	20	inch		BLEN			24	in max conveyor width
10	Finished Board Width	18	inch		BWID			[the inputs above do not yet affect the model]	
11	Number of Drilled Through-Holes	5,000	per board		NHOLES				
12									
13	Minimum Panel Edge Margin	0.8	inch		PMARGIN				
14	Minimum Space Between Boards	0.1	inch		BMARGIN				
15	Boards Per Panel	1			BPPAN				
16									
17				Wgt Price				Lam Price/sqft	
18	Number of Innerlayer Pairs - FR-4	15	100%	$2.17			FR-4	$2.17	
19	Number of Innerlayer Pairs - Type 1	0	0%	$0.00			Type 1	$6.00	
20	Number of Innerlayer Pairs - Type 2	0	0%	$0.00			Type 2	$0.00	
21	Number of Innerlayer Pairs - Type 3	0	0%	$0.00			Type 3	$0.00	
22	Number of Innerlayer Pairs - Type 4	0	0%	$0.00			Type 4	$0.00	
23	Number of Innerlayer Pairs - Type 5	0	0%	$0.00			Type 5	$0.00	
24	Number of Innerlayer Pairs - Type 6	0	0%	$0.00			Type 6	$0.00	
25	Number of Innerlayer Pairs - Type 7	0	0%	$0.00			Type 7	$0.00	
26	Number of Innerlayer Pairs - Type 8	0	0%	$0.00			Type 8	$0.00	
27	Number of Innerlayer Pairs / Avg Price	15	NIP	$2.17					
28									
29	Yield of Innerlayer Pairs	94.0%			INNERYIELD				
30									
31	Yield of Boards, Post-Lamination	99.2%	^ number of innerlayer pairs						
32	Yield of Boards, Post-Lamination	88.0%			TOTYIELD				
33									
34									
35	PROCESSING ISSUES								
36		*Sequence of Operations*							

Cost Preview

Product Description / Facility Description / Operation Database / Cost Summary / Co:

Ready NUM

Strategy for System Cost Models

- Seek input from relevant experts:
  - Technology and hardware selection, identify gaps (white paper)
  - Issues & concerns, e.g. manufacturing yield, reliability
  - Requirements for performance, application, future system (IP, confidentiality issues)
- Define detailed sets of attributes, electrical & optical
- Draft roadmaps: understand which and how the attributes change with performance
- Define 1st generation black box system (top down approach)
- Choose logical set(s) of the key attributes (80/20)
- Obtain cost data, build initial cost model
- Verify and improve model with actual costs, expert input
- Run what if sensitivities: speed, no. lines, hardware variation, yields, …
- Repeat for 2nd generation system

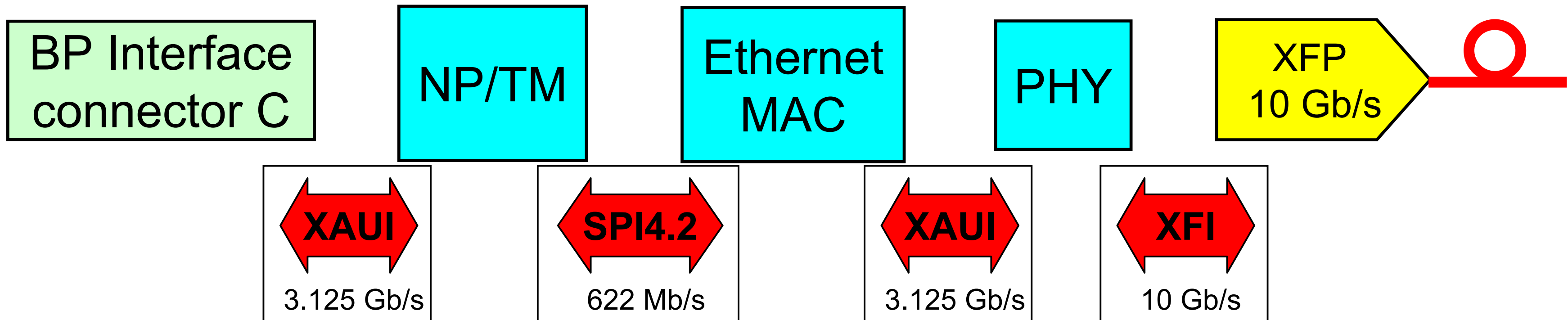
Electrical Backplane Attributes 1-40G (Partial)

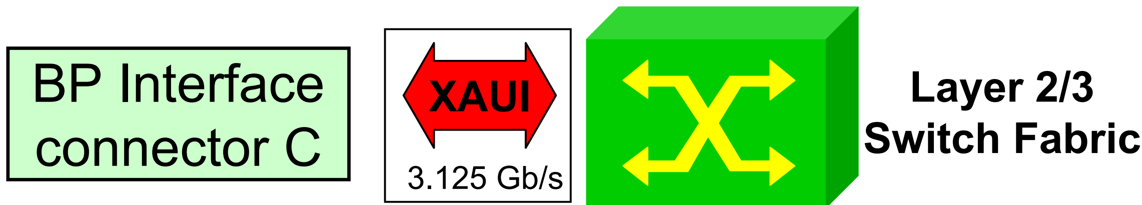
- Receiver/Transmitter signal conditioning chip set:
  - Bus type: multipoint, point-to-point
  - Signaling: single-ended, differential, CML NRZ, 4PAM
  - Standard: DDR2/3/4, LVDS, XAUI, CEI-6G-SR/LR, CEI-11G-SR
  - Equalisation: 400 mV emphasis, DFE 5/8 tap, duobinary
- PCB Technology:
  - Materials: FR4, PPO/CE, FR4013, BT/APPE, PTFE
  - Loss: Df = 0.02 - 0.002
  - Processes: standard, backdrilling, dual density drilling
  - Transmission line: single-ended, loosely coupled, broadside
  - Distance: up to 1m
  - Via/connector launch: PTH, pad in via, micro, buried, differential anti-pad
- Connector Technology:
  - Several vendor types

iNEMI Optical Backplane Attributes 1-40G (Partial)

- Receiver/Transmitter:
  - Link loss budget: 0.5 dB per channel
  - Source/modulation: < 5G VCSEL, <10G F-P(int), >10G DFB (ext)
  - Channel density: transceivers, VCSEL / PD arrays
  - Multiplex: serial (TDM), parallel (12-72 channels), CWDM
- Light coupling:
  - Type: butt coupled, index matched, lens, mirror/grating, free-space
- Optical carrier technology:
  - Fiber: single, ribbon, flex/laminated (shuffle), MM or SM
  - Waveguide: surface, embedded, organic, silica, PLC
  - Impact on PCB design rules, electrical layer reduction
- Connector:
  - Coupling losses: tolerance, cleanliness (contamination has critical impact on yield & costs, but hard to quantify)
- Assembly & Test

ETHERNET (Layer2/3 Switch)
WB #1 Electrical, XAUI over the backplane

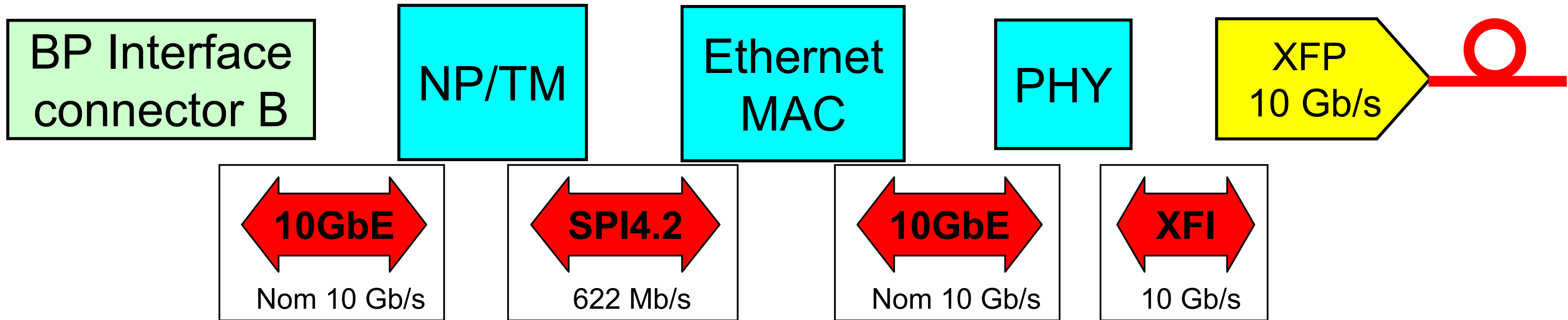


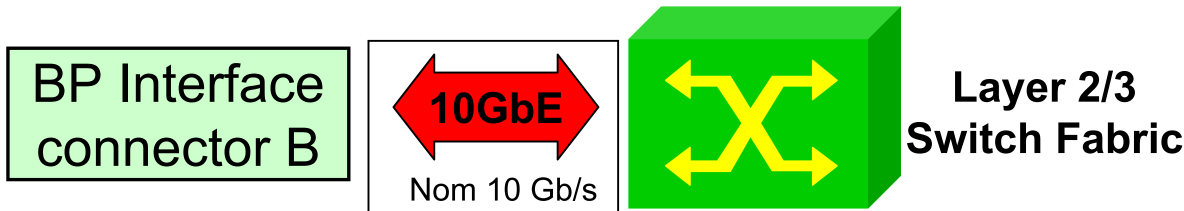


FIC: Fabric Interface Chip
NP/TM: Network Processor/Traffic Manager
MAC: Medium Access Controller .
PHY: Physical Interface

ETHERNET (Layer2/3 Switch)

WB #1 Electrical, 10G Native over the backplane





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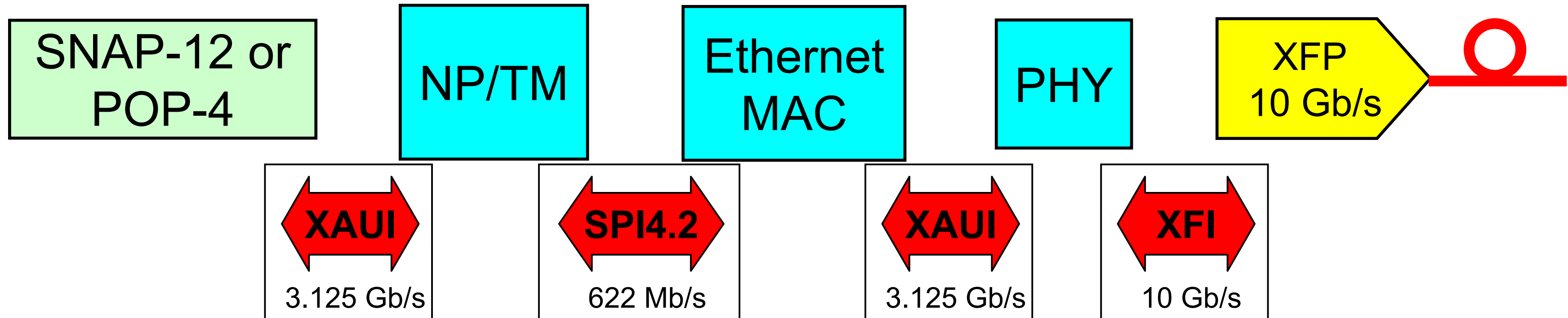
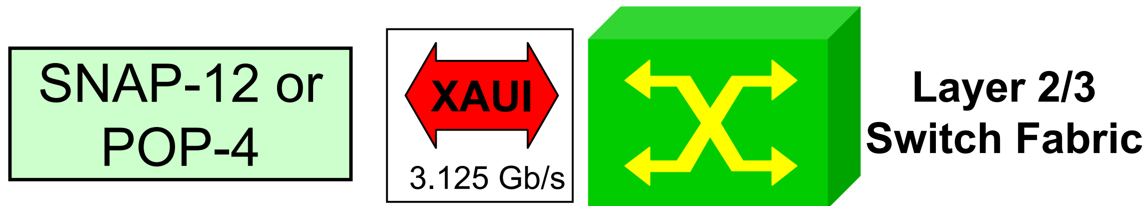
ETHERNET (Layer2/3 Switch)
BB #1 Optical, XAUI rate over the backplane





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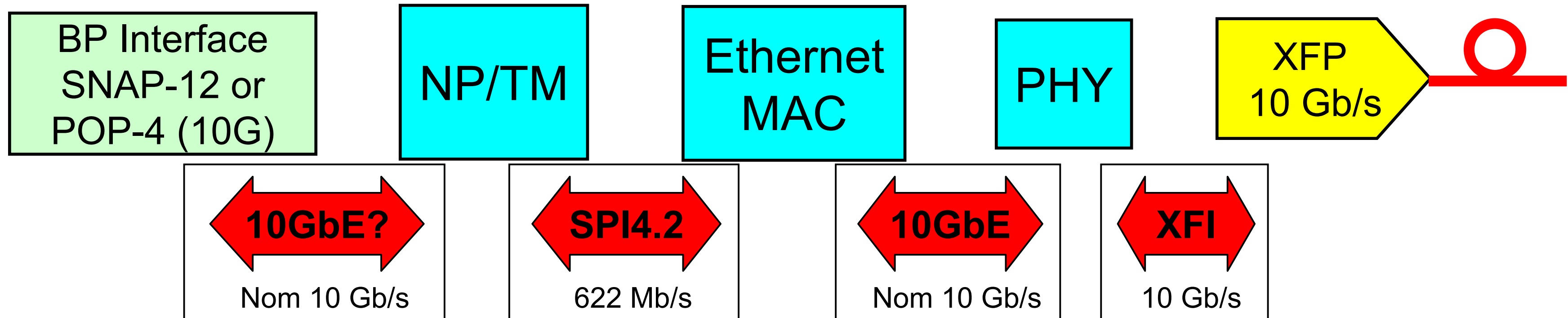
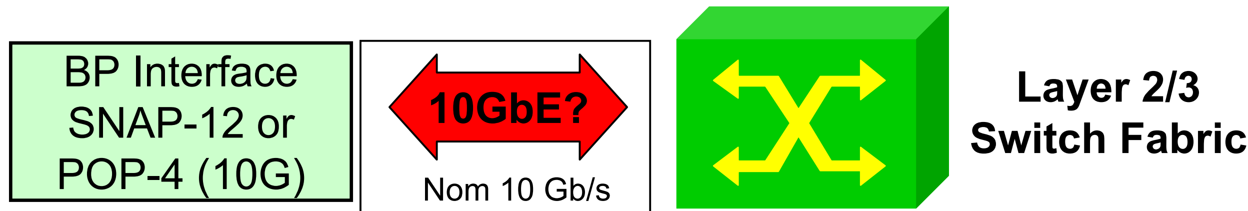
CONNECT WITH AND STRENGTHEN YOUR SUPPLY CHAIN

ETHERNET (Layer2/3 Switch)
BB #1 Optical, 10G Native over the backplane





FIC: Fabric Interface Chip
NP/TM: Network Processor/Traffic Manager
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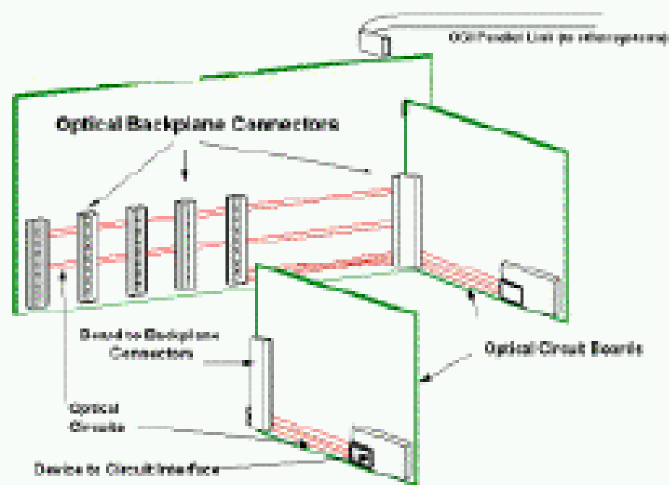
Future Optical Black Boxes

- Optical Black Box #2:
  - 40G implementation of BB#1, and/or fully populated frame (3 ATCA shelves, 16 cards per shelf), and/or full mesh system (high channel count) TBD
  - Fiber based
  - Possibly use CWDM optical multiplexed signals within the fabric to overcome space restrictions
- Optical Black Box #3:
  - Fiber Flexplane version of BB#2 (TBD)
- Optical Black Box #4:
  - Organic embedded waveguide in backplane, version of BB#2

Optoelectronics Circuits



3rd Generation Optical Circuits

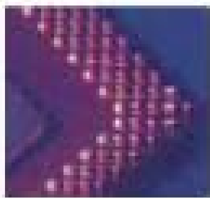
2nd Generation Hybrid Fiber Cables

1st Generation Discrete Fiber Interconnect

2000

2010

Courtesy: JWatson, 3M Optical Comm Tech Center



Board-to-Board Optical Interconnects

Daughterboard

Optical and Electronic Interconnects

Backplane

Optical Transmitter, Receiver or Transceiver Modules

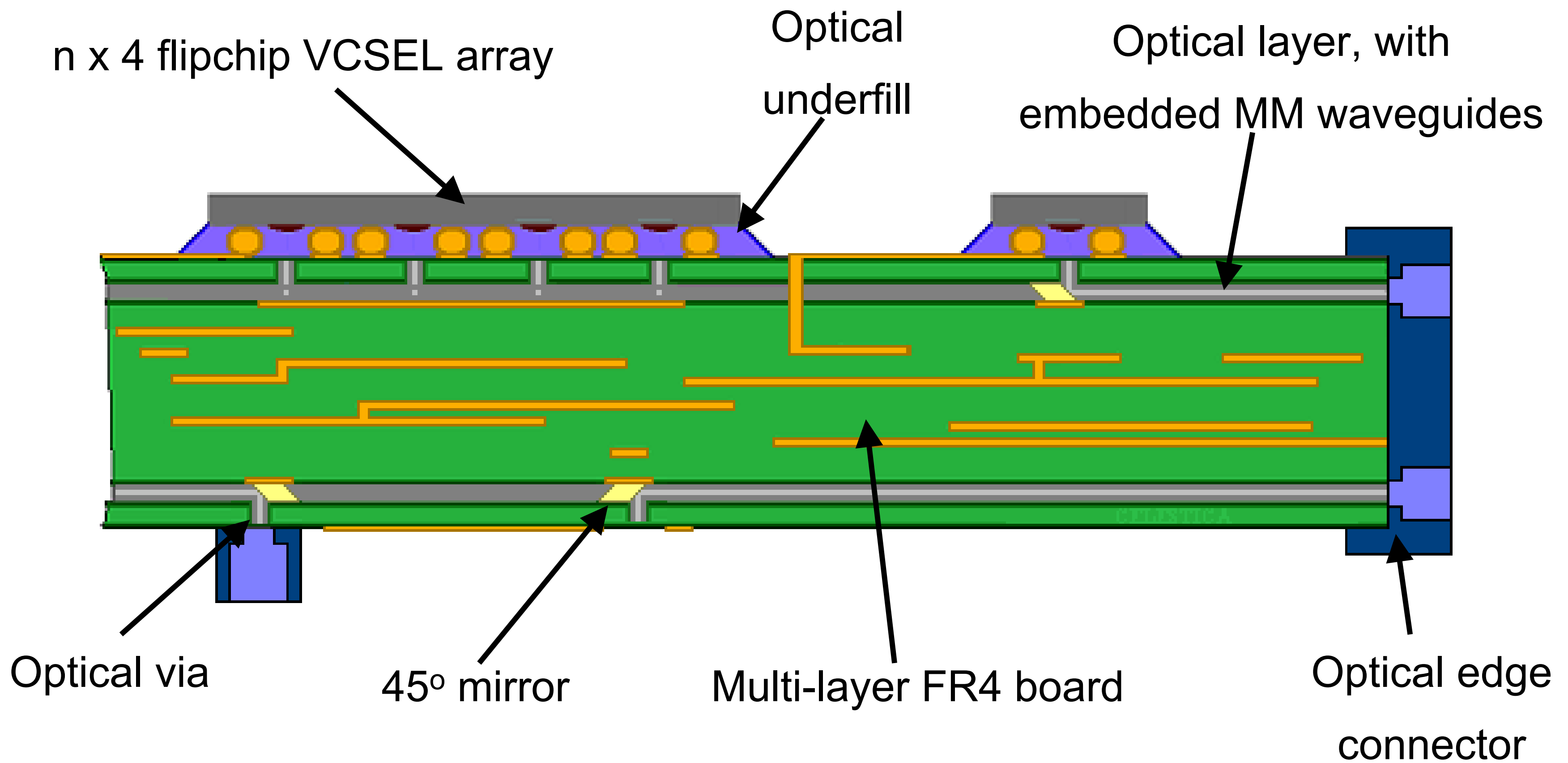
Optical/Waveguide and Electrical Conductors

Blind-Mating Optical Backplane Connectors

Motherboard

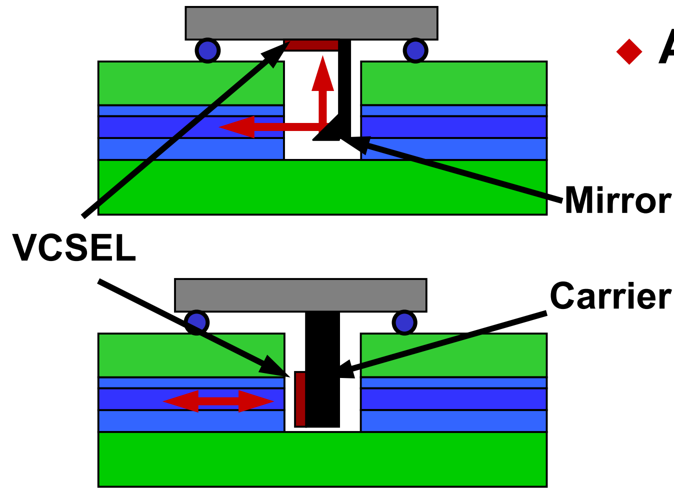
iNEMI

OECB Technology Challenges



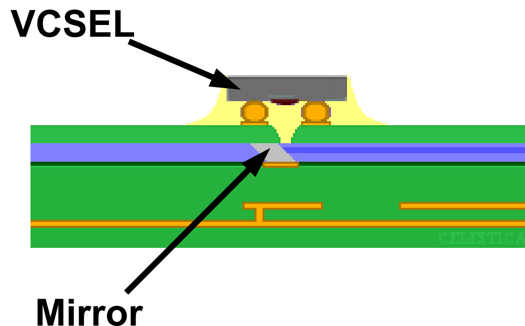
- Choice of Glass or Polymer optical layers
- Choice of embedded or overlaid waveguides
- Choice of assembled or integrated mirrors

Coupling Challenge



Source: Siemens SBS C-Labs

- **Assembled Mirror ?**
  - Several research avenues involving the insertion of mirrors or carriers.
  - Large alignment tolerance stack-up.
  - High cost issues due to small parts, and tight alignment tolerances.



- **Integrated Mirror ?**
  - Ideal process route is to combine mirror into board during PCB fabrication, for direct active component attach.
  - Limited alignment tolerance stack-up.
  - Low cost assembly achievable.

Optical Material Characteristics

	Coupling Methods (3)	Applications	Producer	Status
Optical Waveguides				
Polymer				
Deposited	Fiber + Free Space	Backplanes, General interconnect		R&D
Photoimaged	Direct fiber/component, I/O mirror arrays, Array connectors, single/stacked layers	Stand alone flex or board/substrate interconnects-chip, component, functions, links, fully connectorized, stacked or single layer.	Optical CrossLinks	Custom Prototyping & Production
Embossed				
Press	Fiber + Surface (4)	WDM, Splitters, Couplers, ADM	OptoFoil - Fraunhofer Institute	Production
Roll	Fiber + Surface (4)	Ribbon Cables, Backplanes	3M, Promerus	Production
Trench & Fill	Fiber + Surface	DWDM, VOA, ADM, Splitters, Couplers	Shipley, DuPont Photonics, NTT, Neophotonics	R&D
Micromolded	Fiber/F.S./Surface (4)	Light Pipes, Backplanes, Passive Interconnect	Promerus	Production
Molded	Fiber + Free Space	Light Pipes, Backplanes		?
Inorganic				
Silica on Silicon	Fiber end	DWDM, ADM, AWG	Neophotonics, Symmorphics	Production
Polysilicon	Fiber end	Chip Switches, Modulators	Intel	Research
Hybrids (6)	Fiber end	VOA, ADM	Lightwave Microsystems, Neophotonics	Production
Optical Fiber				
Embedded Fiber				
Glass	Fiber + Surface	Backplanes, Lightpipes	Hitachi Chemical (Wire Wrap)	R&D
Polymer	Fiber + Surface	Backplanes, Lightpipes	Northrup-Grunman	R&D

Optical Material Characteristics (2)

	Field Size in.	Attenuation, dB/cm 830 nm	1550 nm	WG Type	Mode Structure	Waveguide Pitch (2)	NRE Cost $/Layer (5)	Cost $/ft^2/Layer (5)
Optical Waveguides								
Polymer								
Deposited	12 X 18	0.1	0.5	Rib	Multimode	Coarse	1K	5 - 10
Photoimaged	12 X 18, 13" reel to reel	0.08	0.7	Rib & Embedded	Single Mode & Multimode	Hyperfine	100 to~2500	30-50
Embossed								
Press	Wafer (1)	0.1	0.1	Embedded	Single/Multi	Fine	10K	1,500
Roll	36 X 36	0.1	0.3	Rib & Embedded	Single/Multi	Fine	20K	5 - 10
Trench & Fill	Wafer	0.1	0.1	Embedded	Single/Multi	Fine	10K	1,500
Micromolded	36 X 36	0.1	0.3	Rib & Embedded	Single/Multi	Fine	12K	10
Molded	24 X 24	0.1	0.5	Rib	Multimode	Coarse	>50K	5
Inorganic								
Silica on Silicon	Wafer	< 0.1	< 0.1	Rib & Embedded	Single/Multi	Fine	10K	1,500
Polysilicon	Wafer	?	?	Embedded	Single Mode	Fine	15K	3000
Hybrids (6)	Wafer	< 0.1	< 0.1	Rib & Embedded	Single	Fine	15K	1,700
Optical Fiber								
Embedded Fiber								
Glass	18 X 24	< 0.1	< 0.1	Embedded	Single/Multi	Coarse	5K	50
Polymer	18 X 24	< 0.1	< 0.1	Embedded	Multimode	Coarse	5K	30

Next Steps

- Run multiple copper sensitivities
  - Materials, via qty. and types,
  - Layers counts, etc.
- Develop connector data base
  - Cost, type, application
- Add signal conditioning, bus chip-sets, ASICs
  - May need resource assistance
- Complete optical attributes and optical technology roadmap
- Determine the copper / opto architectures to be modeled for high performance
  - Difficult because it is often proprietary information

Conclusions

- Performance of copper backplanes will continue to improve, at increased cost to achieve signal integrity
- Benefits of optical outweigh cost for critical applications, e,g, avionics, clock distribution in high perf systems
- Future generation, high bandwidth telecom/office systems likely to have optical distribution
- The problems of assembling and handling fiber/connectors are drivers for integrating optical waveguides in the PWB
- Improved coupling and light-turning technologies are required
- The initial choices of optical technology and component set have major impact on overall costs
- Cost-performance models of emulator systems are useful way to understand the (relative) costs, test different choices
- Immediate need for practical cost-performance metric(s), e.g. $/bit, $/(Gbps/m/channel)

Contacts

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Thank You
Optoelectronics Substrates Project

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