



International Electronics Manufacturing Initiative

**SMT Reel Labeling
Project Workshop
iNEMI Process**

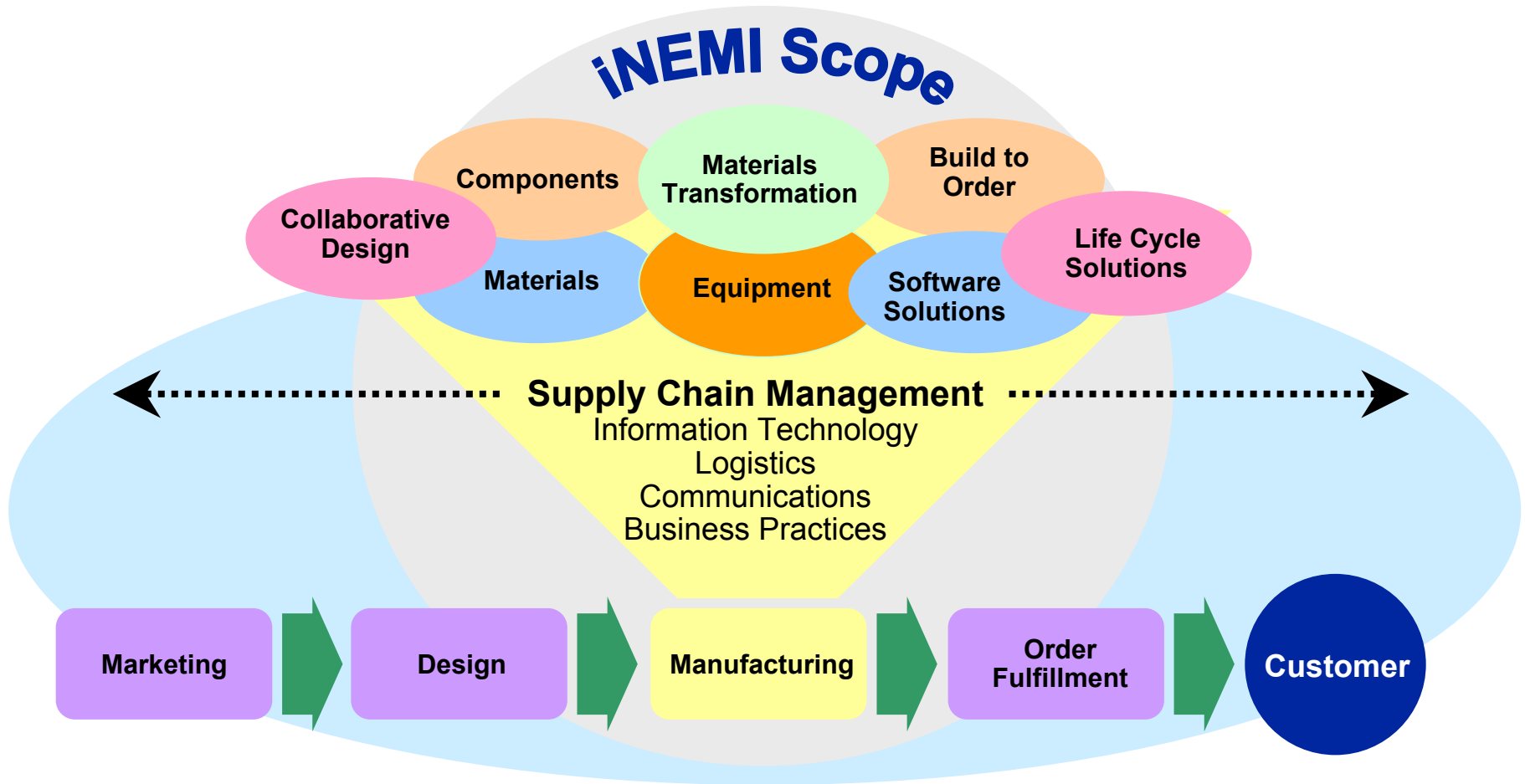


David Godlewski, iNEMI

April 27, 2005

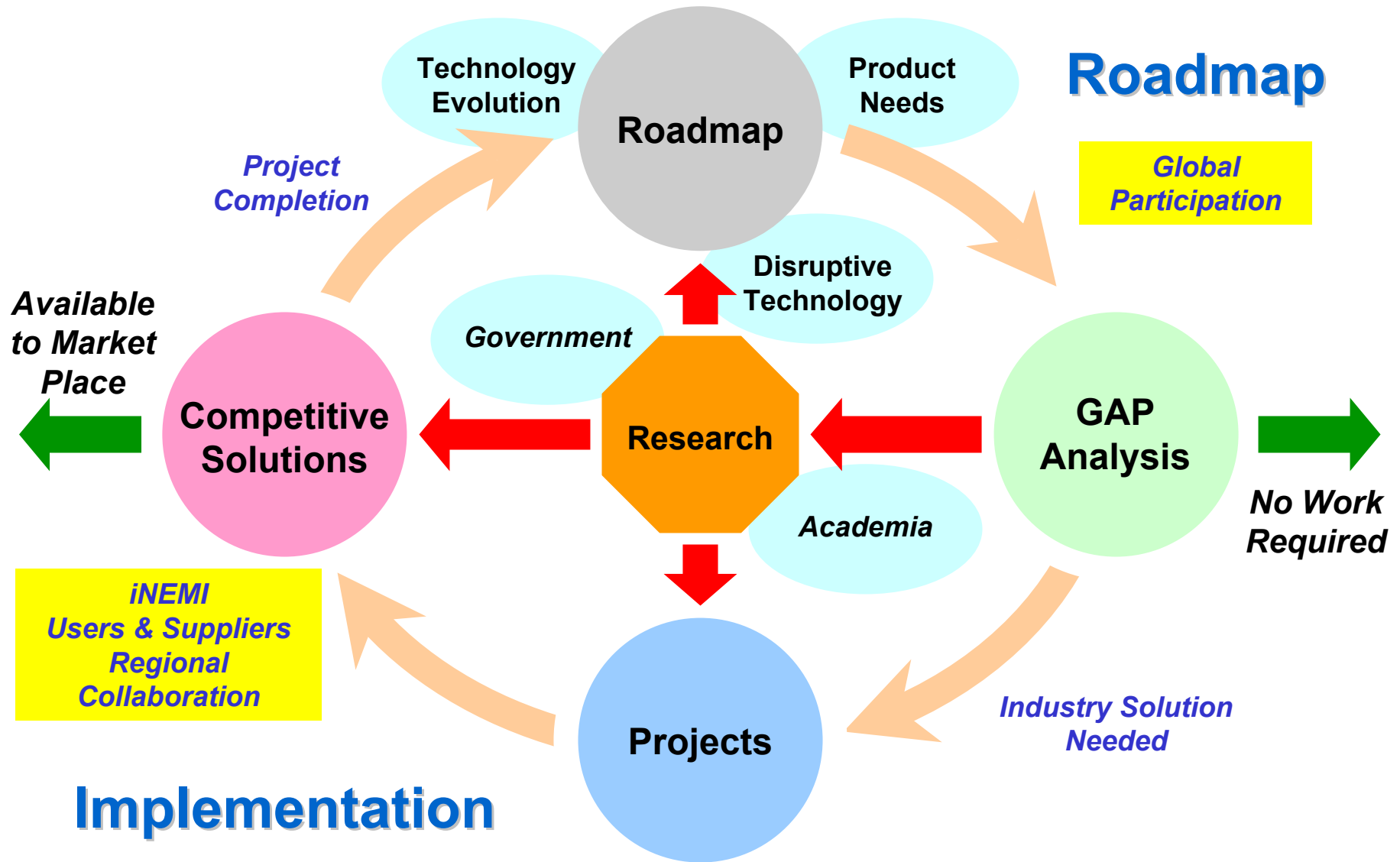
**Texas Instruments Alliance Product
Distribution Center
Fort Worth, Texas**

*Assure Leadership of the Global Electronics Manufacturing Supply Chain
for the benefit of members and the industry*



Leverage the combined power of member companies to provide industry leadership

- **iNEMI roadmaps the global needs of the electronics industry**
 - **- Evolution of existing technologies**
 - **- Prediction of emerging/innovative technologies**
- **iNEMI identifies gaps (both business & technical) in the electronics infrastructure**
- **iNEMI stimulates research/innovation to fill gaps**
- **iNEMI establishes implementation projects to eliminate gaps**
- **iNEMI stimulates worldwide standards to speed the introduction of new technology & business practices**
- **iNEMI works with other organizations to ensure that government policy recommendations are aligned with our mission.**



- **Distribute Schedule and Template to TIG Chairs / TC 2/1/05**
- **TIG Chairs Hold Gap Analysis Meetings as Follows:**
 - **iNEMI Board Assembly and Substrates TIG Meeting @ APEX 2/22/05**
 - **iNEMI SIP TIG Meeting - NEW @ APEX 2/23/05**
 - **iNEMI Environmental TIG Meeting @ APEX 2/24/05, @ ISEE 5/16-19/05**
 - **iNEMI PLIM TIG Meeting @ Intel 3/1-3/05**
 - **iNEMI OPTO TIG Meeting @ OFC 3/6-10/05**
- **TIG Chairs / TC Discuss Gaps / Technical Plan at APEX 2/25/05**
- **Research Committee Telecons 3/3/05, 4/7/05**
- **Drafts from TIGs and RC due 6/17/05**
- **T.C. Face to Face on Technical Plan / Research Priorities in Herndon 6/23-24/05**
- **Release 2005 Research Priorities @ BOD/EI Meetings in Herndon 9/14-15/05**
- **Release 2005 Technical Plan to Members @ SMTAI 9/25-29/05**

- **Outline for each TIG's Technical Plan input**
 - **Introduction**
 - **Gap Analysis and Five-year plan**
 - **What has changed**
 - **TIG Plan**
 - **Projects/programs to focus on short term -prioritize**
 - **Identify areas where research is needed -prioritize**
 - **Summary**

Drivers

Low volumes
Low cost
Bandwidth
Part # red'n

OPTOELECTRONICS ATTRIBUTES

10Gbps longhaul
Emerging module package standards (i.e., SFP, XFP, SNAP-12)
Pb-free incompatible (levels 1&2)
Sensitive materials (heat, handling, moisture and other environmental factors)
Light in-plane to substrate (fiber, flex)
Hybrid integrated optical & electronic systems
Little DFX
Out-of-plane bend issues: PCB fab, losses, coupling efficiency, reliability
Module heat @ 20W max
Component function/ λ stability strongly operating temperature dependent

DEPLOYED TECHNOLOGY

Semi-auto fiber alignment
Multi-step solder, weld, adhesive bond
MSAs define electrical I/O (only)
MEM/MOEMs

RESEARCH & DEVELOPMENT

Photonic band gap/optical crystals
New OE materials
Self/passive part alignment
Embedded waveguides
90° light bend with substrate
1550 nm VCSEL
Fiberless Level 2 assembly

2005

Drivers

Low Cost
Higher volumes
Bandwidth
Robust
Size reduction

OPTOELECTRONICS ATTRIBUTES

40 Gbps longhaul
Standard package types, pluggable (no fiber pigtailed)
Pb-free compatible
More robust OE materials
Out-of-plane light within substrate, optical via
Monolithic O-E integration
Some DFM & DFT
OE/thermal design tools
Bend radius within substrate thickness
Temperature tolerant devices

DEPLOYED TECHNOLOGY

Auto fiber alignment
Self/passive part alignment
Single step bonding
Waveguides couple to connectors
Standards for packages, assembly, datacom rel, etc

RESEARCH & DEVELOPMENT

Low cost SS OE devices, SOA, tuneable
Fiberless Level 2 assembly
All optical network
Optical self test modules
Nanostructures, nano-OEMs

2007

Drivers

Low cost
Higher volumes
Bandwidth
Robust
Size reduction

OPTOELECTRONICS ATTRIBUTES

40 Gbps longhaul
Integrated O-E organic substrates
Tunable, parallel sources/receivers
Monolithic O-E integration
Integrated design tools, for DFX
Transverse coupled waveguides
No active cooling requirement

DEPLOYED TECHNOLOGY

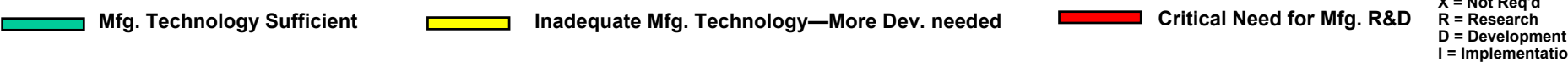
Fiberless Level 2 assembly
Self/passive part alignment
Waveguides coupling to devices
All adhesive bonding
Molded components
Many standards
System interoperability, protocol independent
Configurable optical network

RESEARCH & DEVELOPMENT

Photonic transistor & memory
Optical bit switching
Integrated OE modules based on PBG
Soliton transmission

2009/2011

	2005	2007	2009	2011	Need
Level-1: Device Technology					
VCSEL array yield & reliability, 1550 nm					D, I
Non-cooled, thermally tolerant devices					R, D
O-E integration, based on Si CMOS					R, D
Emerging SS devices, SOA, switches, OBG...					R
Level-2: Packaged component					
Design for manufacturing, test, cost (DFx)					D, I
Passive/self alignment					D, I
Hybrid O-E integration					D
Adhesives for attach & optical coupling					D, I
Pb-free compatibility					I
Waveguide-device coupling					D
Levels 3 & 4: module, sub-system					
Compatible electrical & optical assembly					D, I
Low temp, Pb-free solder attach					I
Fiber assembly (connector, fiber handling)					D, I
Embedded waveguides					D, I
Waveguide-connector coupling (in-plane)					D, I
Optical via (out-of-plane coupling)					D, I
Standards					
Packaging, assembly & test, e.g. IPC 0040					I
Interoperability at system/network level					D, I
Reliability for datacom/last mile applications					D, I
Test: critical parameters/reduced capex					I
Industry stnd optical interconnects					D, I

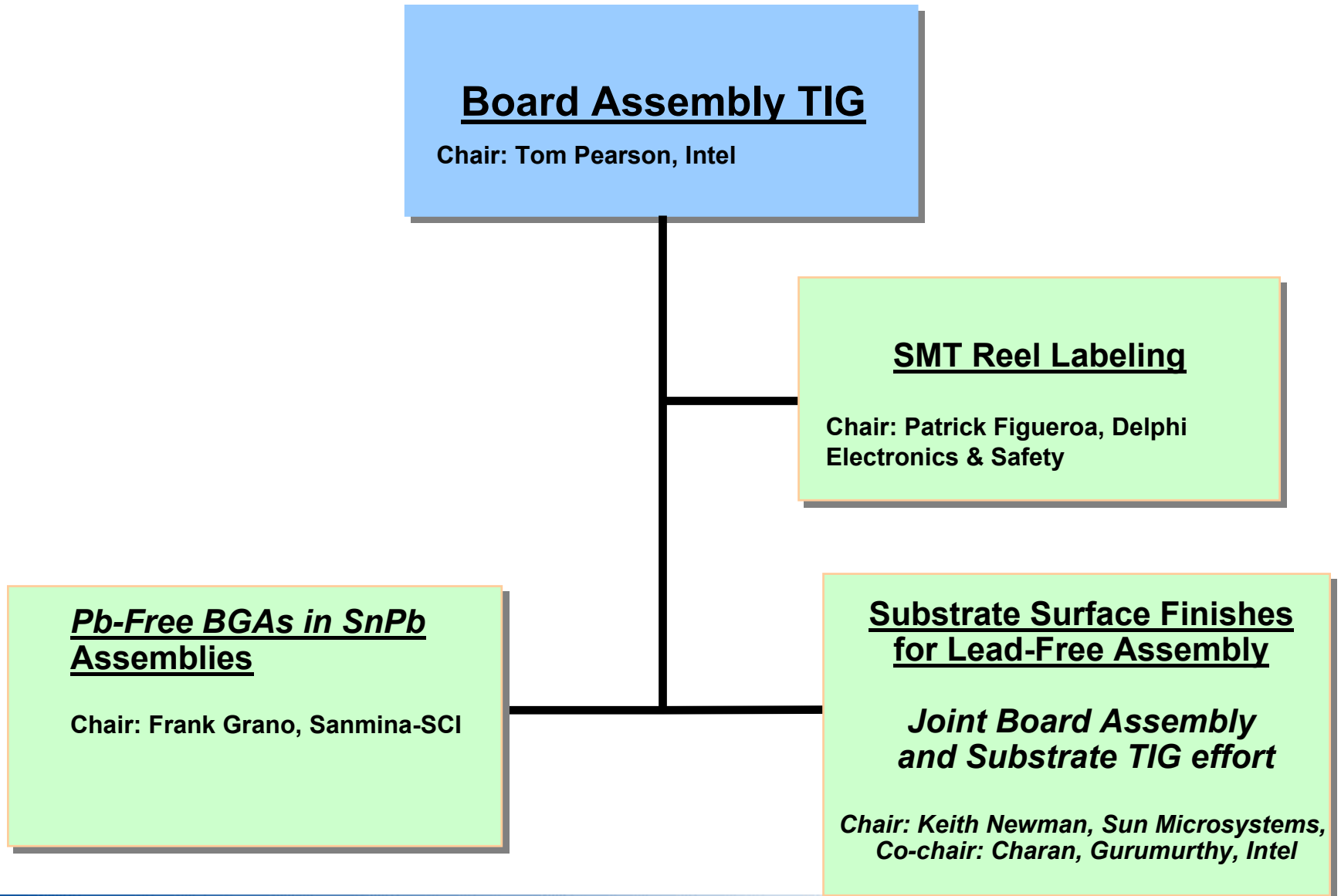


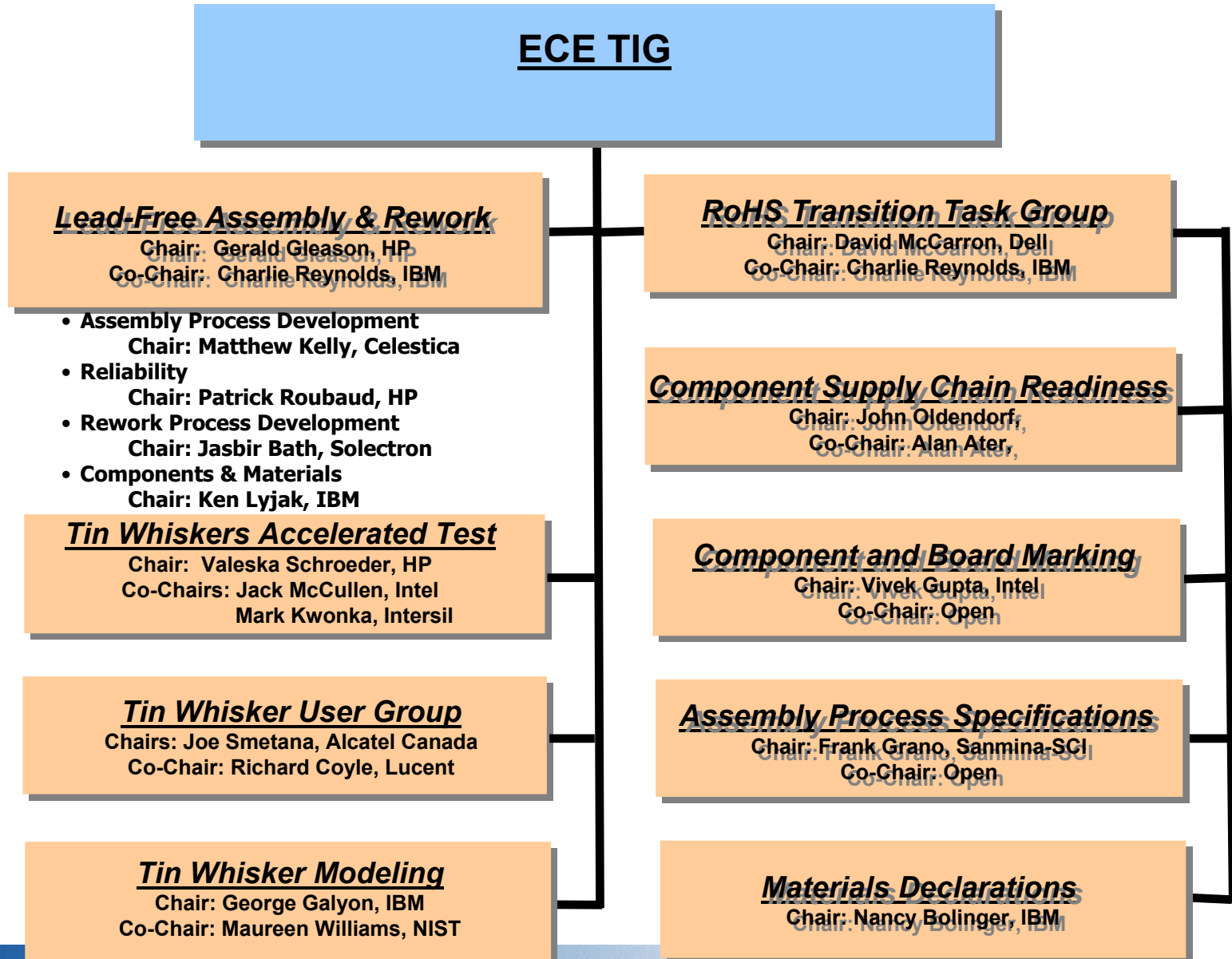
iNEMI Project Review

David Godlewski, iNEMI

New Projects:

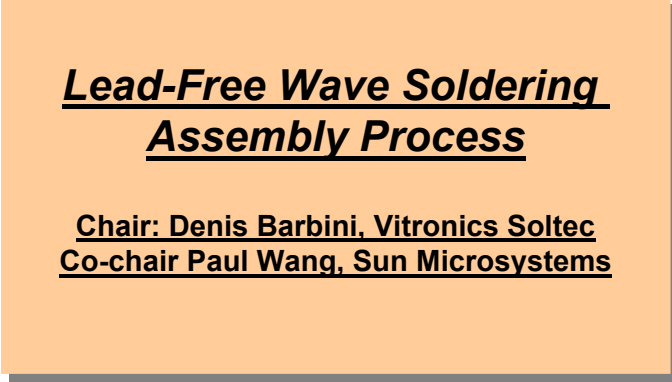
- **Board Assembly TIG:**
 - **SMT Reel Labeling Project**
 - **Pb-free BGAs in SnPb Assemblies Project**
- **ECE TIG**
 - **Pb-free Wave Soldering Assembly Process Project**
- **PLIM & ECE TIG:**
 - **Materials Composition Data Exchange Project**
- **Optoelectronic TIG:**
 - **Fiber Optic Splice Loss Measurement Project**
 - **Fiber Connector End-Face Inspection Project**
- **Substrates TIG:**
 - **Evaluation of Substrate Surface Finishes for Pb-free Assembly Project**
 - **Optoelectronics for Substrates Project**
- **Five projects completed in 2004:**
 - **Defects Per Million Opportunities**
 - **Fiber Optic Splice Improvement**
 - **Fiber Optic Signal Performance**
 - **Lead-Free Hybrid Assembly and Rework Project**
 - **High-Frequency Material Effects on HDI Formation Project**





A light blue rectangular box with a dark blue border, containing the text 'ECE TIG' in bold black font, underlined.

ECE TIG

An orange rectangular box with a dark orange border, containing the text 'Lead-Free Wave Soldering Assembly Process' in bold black font, underlined, and the names of the chair and co-chair below it.

**Lead-Free Wave Soldering
Assembly Process**

Chair: Denis Barbini, Vitronics Soltec
Co-chair Paul Wang, Sun Microsystems

Substrates TIG

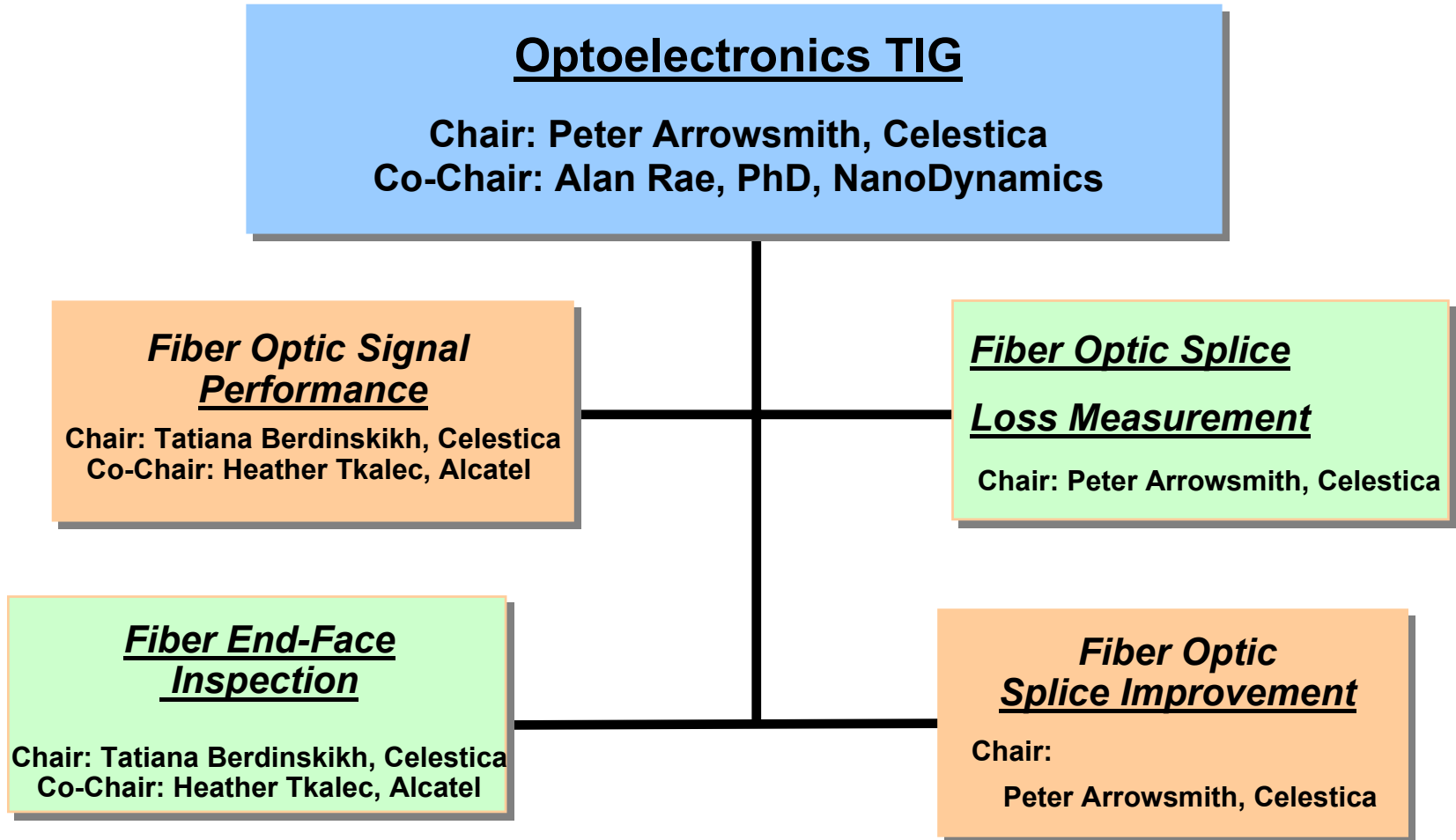
Chair: Hamid Azimi, PhD, Intel

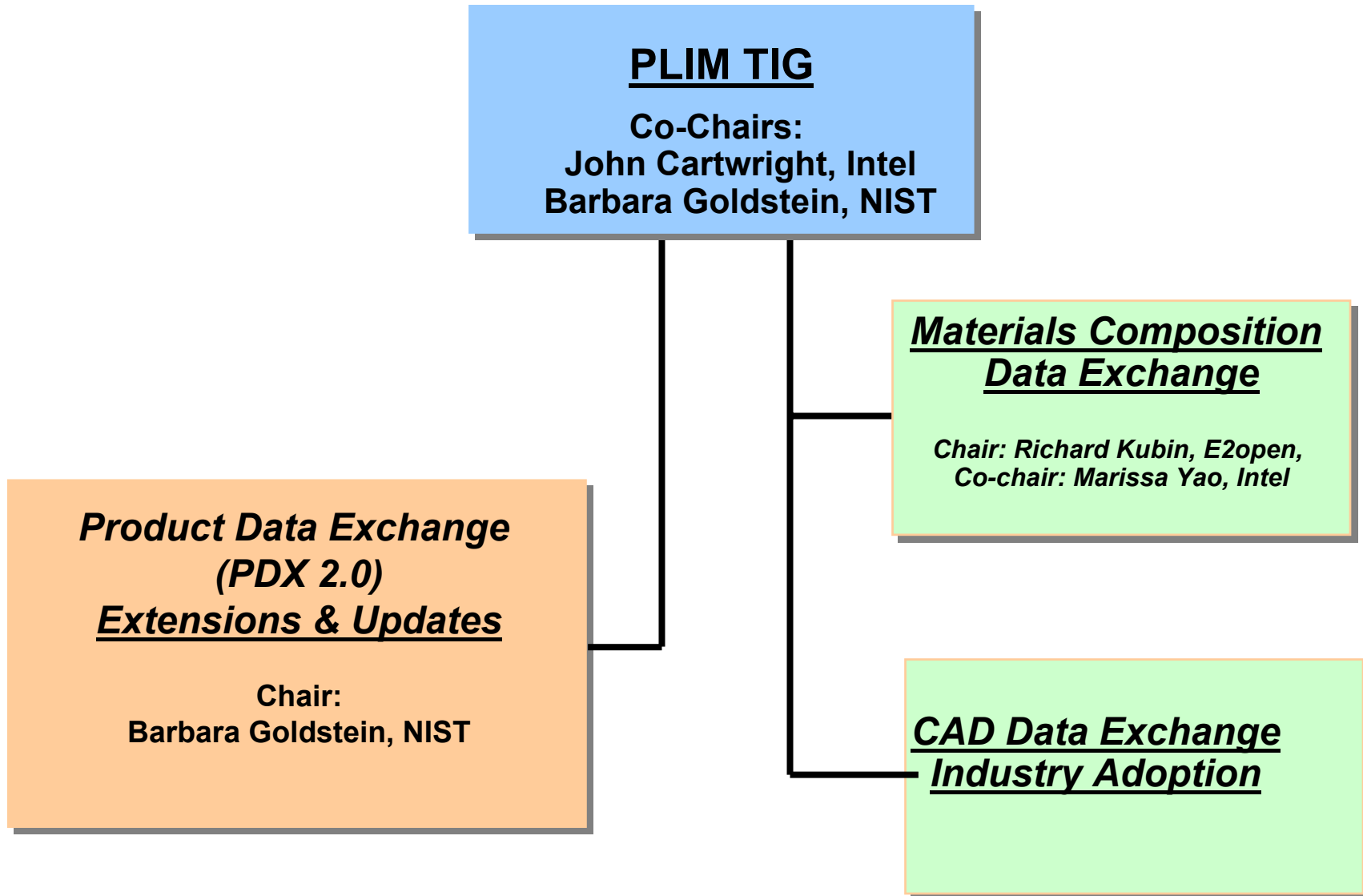
High Frequency Material Effects on HDI

Chair: Hamid Azimi, PhD, Intel
Co-Chair: Jack Fisher, IPC

Optoelectronics for Substrates

Chair: Jack Fisher, iNEMI/IPC







International Electronics Manufacturing Initiative

SMT Reel Labeling Project Overview



Patrick Figueroa, Delphi
April 27, 2005
Texas Instruments Alliance Product
Distribution Center
Fort Worth, Texas

- **Electronic Component package labeling is critical to enable verification and/or tracking of the following :**
 - **Correct SMT machine set-up**
 - **Moisture sensitive device exposure time**
 - **Component traceability**
 - **Real-time Inventory**
- **Some OEMs and EMS providers tend to develop their own company specific labeling specifications**
- **Leading to higher component costs and sometimes error prone due to re-labeling**

- **Develop an industry guideline for labeling automatically placed electronic component packages (e.g. Tape & Reel, Ammo Pack, Matrix Trays, etc) that meets the needs of electronics industry OEM/EMS companies.**

- **The group's efforts will initially focus on defining the following:**
 - **Minimum label content required**
 - **Example: Unique Trace Identifier (Could include supplier DUNS # and unique sequence number)**
 - **Data identifiers to be used for each piece of information**
 - **Acceptable bar code symbologies and/or RFID**
 - **2D symbologies, define field separators**
 - **Label location on each different package type**
 - **Acceptable bar code quality requirements**
 - **Polarity markings on label for capacitors, diodes, etc.**

- **Lead free (JEDEC Standard JESD97) and moisture sensitivity labeling requirements included in labeling guideline**
- **Guideline should also specify to what piece(s) of packaging this label should be applied**
- **The project group will not propose EDI requirement definition**

- **Collect data**
 - **Collect all applicable Industry Standards**
 - JEDEC Standard, JESD97
 - EIA 624 – Electronics Industries Association – Product Package Bar Code Label Standard for Non-Retail Applications
 - EIA 621 – Electronics Industries Association – Consumer Electronics Group Product and Packaging Bar Code Standard
 - Current activity being led by NEDA defining guideline for labeling product packages in the Distribution Environment
 - EPC (Extended Product Code) Global (epcglobalinc.org)
 - IEC 62090 – Product Package Labels for Electronic Components Using Bar Code and Two Dimensional Symbologies
 - ANSI MH10.8.6 – Packaging – Linear bar code and two-dimensional symbols for product packaging
 - ANSI MH10.8.7 – Labeling and Direct Product Marking with Linear Bar Code and Two-Dimensional
 - Data Content Standards
 - ANSI MH10.8.2 – Data Application Identifier Standard
 - ISO 15424 – Data Carrier / Symbology Identifiers
 - ISO 15459-2 – Automatic Identification and Data Capture Techniques – International Specification – Unique Identifier for Transport Units
 - ISO 15963 – Unique ID of RF Tag (Technical Report)
 - ANSI MH 10.8.3 / ISO 15434 – Transfer Data Syntax for High Capacity ADC Media

- **Conformance Standards Optically – Readable Media**
 - ISO 15415 – Bar Code Print Quality Test Specification – 2D Symbols
 - ISO 15416 – Bar Code Print Quality Test Specification – Linear Symbols
 - ISO 15426-1 – Verifier Conformance Spec – Linear
 - ISO 15426-2 – Verifier Conformance Spec – 2D
 - ISO 15423-1 – Scanner & Decoder Performance Testing – Linear
 - ISO 15423-2 – Scanner & Decoder Performance Testing – 2D
 - ISO 15419 – Digital Imaging, Printer Performance Testing & Bar Code Printing Software
 - ISO 15421 – Master Test Specification
- **Bar Code Symbology Specifications**
 - ISO 16388 – Code 39
 - ISO 15417 – Code 128
 - ISO 16022 – Data Matrix
 - ISO 15438 – PDF417
- **Team to define guidelines based on narrowing scope and better defining requirements specified in current industry standards – May 31, 2005**
- **Document and summarize – July 31, 2005**
- **Project completion – August 31, 2005**