SMT Reel Labeling Project Workshop
iNEMI Process

David Godlewski, iNEMI
April 27, 2005
Texas Instruments Alliance Product Distribution Center
Fort Worth, Texas
Mission

Assure Leadership of the Global Electronics Manufacturing Supply Chain for the benefit of members and the industry

iNEMI Scope

Supply Chain Management
Information Technology
Logistics
Communications
Business Practices

Materials Transformation
Equipment
Build to Order
Life Cycle Solutions
Software Solutions
Components
Materials
Collaborative Design

Marketing ➔ Design ➔ Manufacturing ➔ Order Fulfillment ➔ Customer

CONNECT WITH AND STRENGTHEN YOUR SUPPLY CHAIN
What Does iNEMI Do?

Leverage the combined power of member companies to provide industry leadership

- iNEMI roadmaps the global needs of the electronics industry
  - Evolution of existing technologies
  - Prediction of emerging/innovative technologies
- iNEMI identifies gaps (both business & technical) in the electronics infrastructure
- iNEMI stimulates research/innovation to fill gaps
- iNEMI establishes implementation projects to eliminate gaps
- iNEMI stimulates worldwide standards to speed the introduction of new technology & business practices
- iNEMI works with other organizations to ensure that government policy recommendations are aligned with our mission.
2005 Technical Plan Schedule

- Distribute Schedule and Template to TIG Chairs / TC 2/1/05
- TIG Chairs Hold Gap Analysis Meetings as Follows:
  - iNEMI Board Assembly and Substrates TIG Meeting @ APEX 2/22/05
  - iNEMI SIP TIG Meeting - NEW @ APEX 2/23/05
  - iNEMI Environmental TIG Meeting @ APEX 2/24/05, @ ISEE 5/16-19/05
  - iNEMI PLIM TIG Meeting @ Intel 3/1-3/05
  - iNEMI OPTO TIG Meeting @ OFC 3/6-10/05
- TIG Chairs / TC Discuss Gaps / Technical Plan at APEX 2/25/05
- Research Committee Telecons 3/3/05, 4/7/05
- Drafts from TIGs and RC due 6/17/05
- T.C. Face to Face on Technical Plan / Research Priorities in Herndon 6/23-24/05
- Release 2005 Research Priorities @ BOD/El Meetings in Herndon 9/14-15/05
- Release 2005 Technical Plan to Members @ SMTAI 9/25-29/05
Technical Plan Template

• Outline for each TIG’s Technical Plan input
  – Introduction
  – Gap Analysis and Five-year plan
  – What has changed
  – TIG Plan
    • Projects/programs to focus on short term -prioritize
    • Identify areas where research is needed -prioritize
  – Summary
### 2005

**Drivers**
- Low volumes
- Low cost
- Bandwidth
- Part # red’n

**Optoelectronics Attributes**
- 10Gbps longhaul
- Emerging module package standards (i.e., SFP, XFP, SNAP-12)
- Pb-free incompatible (levels 1&2)
- Sensitive materials (heat, handling, moisture and other environmental factors)
- Light in-plane to substrate (fiber, flex)
- Hybrid integrated optical & electronic systems
- Little DFX
- Out-of-plane bend issues: PCB fab, losses, coupling efficiency, reliability
- Module heat @ 20W max
- Component function/λ, stability strongly operating temperature dependent

**Deployed Technology**
- Semi-auto fiber alignment
- Multi-step solder, weld, adhesive bond
- MSAs define electrical I/O (only)
- MEM/MOEMs

**Research & Development**
- Photonic band gap/optical crystals
- New OE materials
- Self/passive part alignment
- Embedded waveguides
- 90° light bend with substrate
- 1550 nm VCSEL
- Fiberless Level 2 assembly

### 2007

**Drivers**
- Low cost
- Higher volumes
- Bandwidth
- Robust
- Size reduction

**Optoelectronics Attributes**
- 40 Gbps longhaul
- Standard package types, pluggable (no fiber pigtails)
- Pb-free compatible
- More robust OE materials
- Out-of-plane light within substrate, optical via
- Monolithic O-E integration
- Some DFM & DFT
- OE/thermal design tools
- Bend radius within substrate thickness
- Temperature tolerant devices

**Deployed Technology**
- Auto fiber alignment
- Self/passive part alignment
- Single step bonding
- Waveguides couple to connectors
- Standards for packages, assembly, datacom rel, etc

**Research & Development**
- Photonic transistor & memory
- Optical bit switching
- Integrated OE modules based on PBG
- Soliton transmission

### 2009/2011

**Drivers**
- Low cost
- Higher volumes
- Bandwidth
- Robust
- Size reduction

**Optoelectronics Attributes**
- 40 Gbps longhaul
- Integrated O-E organic substrates
- Tunable, parallel sources/receivers
- Monolithic O-E integration
- Integrated design tools, for DFX
- Transverse coupled waveguides
- No active cooling requirement

**Deployed Technology**
- Fiberless Level 2 assembly
- Self/passive part alignment
- Waveguides coupling to devices
- All adhesive bonding
- Molded components
- Many standards
- System interoperability, protocol independent
- Configurable optical network

**Research & Development**
- Photonic transistor & memory
- Optical bit switching
- Integrated OE modules based on PBG
- Soliton transmission

**Connect With and Strengthen Your Supply Chain**
### Optoelectronics – Prioritized Gap Analysis

#### Level-1: Device Technology

<table>
<thead>
<tr>
<th></th>
<th>2005</th>
<th>2007</th>
<th>2009</th>
<th>2011</th>
<th>Need</th>
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<tbody>
<tr>
<td>VCSEL array yield &amp; reliability, 1550 nm</td>
<td></td>
<td></td>
<td></td>
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<td>D, I</td>
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<tr>
<td>Non-cooled, thermally tolerant devices</td>
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<td>R, D</td>
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<tr>
<td>O-E integration, based on Si CMOS</td>
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<td>R, D</td>
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<tr>
<td>Emerging SS devices, SOA, switches, OBG...</td>
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#### Level-2: Packaged component

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<tbody>
<tr>
<td>Design for manufacturing, test, cost (DFx)</td>
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<td>D, I</td>
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<tr>
<td>Passive/self alignment</td>
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<td></td>
<td>D, I</td>
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<tr>
<td>Hybrid O-E integration</td>
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<td>D, I</td>
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<tr>
<td>Adhesives for attach &amp; optical coupling</td>
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<td>D, I</td>
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<tr>
<td>Pb-free compatibility</td>
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<td>I</td>
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<tr>
<td>Waveguide-device coupling</td>
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<td></td>
<td></td>
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#### Levels 3 & 4: module, sub-system

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<tr>
<td>Compatible electrical &amp; optical assembly</td>
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<tr>
<td>Low temp, Pb-free solder attach</td>
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<td>I</td>
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<tr>
<td>Fiber assembly (connector, fiber handling)</td>
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<td>D, I</td>
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<tr>
<td>Embedded waveguides</td>
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<td>D, I</td>
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<tr>
<td>Waveguide-connector coupling (in-plane)</td>
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<tr>
<td>Optical via (out-of-plane coupling)</td>
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#### Standards

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<th>2011</th>
<th>Need</th>
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<tbody>
<tr>
<td>Packaging, assembly &amp; test, e.g. IPC 0040</td>
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<td></td>
<td></td>
<td></td>
<td>I</td>
</tr>
<tr>
<td>Interoperability at system/network level</td>
<td></td>
<td></td>
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<td>D, I</td>
</tr>
<tr>
<td>Reliability for datacom/last mile applications</td>
<td></td>
<td></td>
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<td>D, I</td>
</tr>
<tr>
<td>Test: critical parameters/reduced capex</td>
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<td></td>
<td>I</td>
</tr>
<tr>
<td>Industry stnd optical interconnects</td>
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<td>D, I</td>
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</tbody>
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**Legend:**
- **Mfg. Technology Sufficient**
- **Inadequate Mfg. Technology—More Dev. needed**
- **Critical Need for Mfg. R&D**

**Codes:**
- X = Not Req’d
- R = Research
- D = Development
- I = Implementation
iNEMI Project Review

David Godlewski, iNEMI
New Projects:
• Board Assembly TIG:
  – SMT Reel Labeling Project
  – Pb-free BGAs in SnPb Assemblies Project
• ECE TIG
  – Pb-free Wave Soldering Assembly Process Project
• PLIM & ECE TIG:
  – Materials Composition Data Exchange Project
• Optoelectronic TIG:
  – Fiber Optic Splice Loss Measurement Project
  – Fiber Connector End-Face Inspection Project
• Substrates TIG:
  – Evaluation of Substrate Surface Finishes for Pb-free Assembly Project
  – Optoelectronics for Substrates Project
• Five projects completed in 2004:
  – Defects Per Million Opportunities
  – Fiber Optic Splice Improvement
  – Fiber Optic Signal Performance
  – Lead-Free Hybrid Assembly and Rework Project
  – High-Frequency Material Effects on HDI Formation Project
Board Assembly Projects

Board Assembly TIG
Chair: Tom Pearson, Intel

- SMT Reel Labeling
  Chair: Patrick Figueroa, Delphi Electronics & Safety

- Pb-Free BGAs in SnPb Assemblies
  Chair: Frank Grano, Sanmina-SCI

- Substrate Surface Finishes for Lead-Free Assembly
 Joint Board Assembly and Substrate TIG effort
  Chair: Keith Newman, Sun Microsystems, Co-chair: Charan, Gurumurthy, Intel
Environmentally Conscious Electronics (ECE) Projects

**ECE TIG**

- **Lead-Free Assembly & Rework**
  - Chair: Gerald Gleason, HP
  - Co-Chair: Charlie Reynolds, IBM
  - Assembly Process Development
    - Chair: Matthew Kelly, Celestica
  - Reliability
    - Chair: Patrick Roubaud, HP
  - Rework Process Development
    - Chair: Jasbir Bath, Socoltron
  - Components & Materials
    - Chair: Ken Lyjak, IBM

- **Tin Whiskers Accelerated Test**
  - Chair: Valeska Schroeder, HP
  - Co-Chairs: Jack McCullen, Intel
  - Mark Kwonka, Intersil

- **Tin Whisker User Group**
  - Chairs: Joe Smetana, Alcatel Canada
  - Co-Chair: Richard Coyle, Lucent

- **Tin Whisker Modeling**
  - Chair: George Galyon, IBM
  - Co-Chair: Maureen Williams, NIST

- **RoHS Transition Task Group**
  - Chair: David McCarren, Dell
  - Co-Chair: Charlie Reynolds, IBM

- **Component Supply Chain Readiness**
  - Chair: John Oldendorf
  - Co-Chair: Alan Ater

- **Component and Board Marking**
  - Chair: Vivek Gupta, Intel
  - Co-Chair: Open

- **Assembly Process Specifications**
  - Chair: Frank Grano, Sanmina-SCI
  - Co-Chair: Open

- **Materials Declarations**
  - Chair: Nancy Bolinger, IBM
Environmentally Conscious Electronics (ECE) Projects

**Lead-Free Wave Soldering Assembly Process**

Chair: Denis Barbini, Vitronics Soltec
Co-chair Paul Wang, Sun Microsystems
Substrates TIG Projects

Substrates TIG
Chair: Hamid Azimi, PhD, Intel

High Frequency Material Effects on HDI
Chair: Hamid Azimi, PhD, Intel
Co-Chair: Jack Fisher, IPC

Optoelectronics for Substrates
Chair: Jack Fisher, iNEMI/IPC
Optoelectronics TIG
Chair: Peter Arrowsmith, Celestica
Co-Chair: Alan Rae, PhD, NanoDynamics

Fiber Optic Signal Performance
Chair: Tatiana Berdinskikh, Celestica
Co-Chair: Heather Tkalec, Alcatel

Fiber Optic Splice Loss Measurement
Chair: Peter Arrowsmith, Celestica

Fiber End-Face Inspection
Chair: Tatiana Berdinskikh, Celestica
Co-Chair: Heather Tkalec, Alcatel

Fiber Optic Splice Improvement
Chair: Peter Arrowsmith, Celestica
Product Life Cycle Information Management (PLIM) Projects

PLIM TIG
Co-Chairs:
John Cartwright, Intel
Barbara Goldstein, NIST

Materials Composition Data Exchange
Chair: Richard Kubin, E2open,
Co-chair: Marissa Yao, Intel

Product Data Exchange (PDX 2.0) Extensions & Updates
Chair: Barbara Goldstein, NIST

CAD Data Exchange Industry Adoption
SMT Reel Labeling
Project Overview

Patrick Figueroa, Delphi
April 27, 2005
Texas Instruments Alliance Product Distribution Center
Fort Worth, Texas
Background

• Electronic Component package labeling is critical to enable verification and/or tracking of the following:
  – Correct SMT machine set-up
  – Moisture sensitive device exposure time
  – Component traceability
  – Real-time Inventory
• Some OEMs and EMS providers tend to develop their own company specific labeling specifications
• Leading to higher component costs and sometimes error prone due to re-labeling
Objective

• Develop an industry guideline for labeling automatically placed electronic component packages (e.g. Tape & Reel, Ammo Pack, Matrix Trays, etc) that meets the needs of electronics industry OEM/EMS companies.
The group’s efforts will initially focus on defining the following:

- Minimum label content required
  - Example: Unique Trace Identifier (Could include supplier DUNS # and unique sequence number)
- Data identifiers to be used for each piece of information
- Acceptable bar code symbologies and/or RFID
- 2D symbologies, define field separators
- Label location on each different package type
- Acceptable bar code quality requirements
- Polarity markings on label for capacitors, diodes, etc.
• Lead free (JEDEC Standard JESD97) and moisture sensitivity labeling requirements included in labeling guideline
• Guideline should also specify to what piece(s) of packaging this label should be applied
• The project group will not propose EDI requirement definition
Schedule

• Collect data
  – Collect all applicable Industry Standards
    • JEDEC Standard, JESD97
    • EIA 624 – Electronics Industries Association – Product Package Bar Code Label Standard for Non-Retail Applications
    • EIA 621 – Electronics Industries Association – Consumer Electronics Group Product and Packaging Bar Code Standard
    • Current activity being led by NEDA defining guideline for labeling product packages in the Distribution Environment
    • EPC (Extended Product Code) Global (epcglobalinc.org)
    • IEC 62090 – Product Package Labels for Electronic Components Using Bar Code and Two Dimensional Symbologies
    • ANSI MH10.8.6 – Packaging – Linear bar code and two-dimensional symbols for product packaging
    • ANSI MH10.8.7 – Labeling and Direct Product Marking with Linear Bar Code and Two-Dimensional
    • Data Content Standards
      – ANSI MH10.8.2 – Data Application Identifier Standard
      – ISO 15424 – Data Carrier / Symbology Identifiers
      – ISO 15963 – Unique ID of RF Tag (Technical Report)
      – ANSI MH 10.8.3 / ISO 15434 – Transfer Data Syntax for High Capacity ADC Media
• Conformance Standards Optically – Readable Media
  – ISO 15415 – Bar Code Print Quality Test Specification – 2D Symbols
  – ISO 15416 – Bar Code Print Quality Test Specification – Linear Symbols
  – ISO 15426-1 – Verifier Conformance Spec – Linear
  – ISO 15426-2 – Verifier Conformance Spec – 2D
  – ISO 15423-1 – Scanner & Decoder Performance Testing – Linear
  – ISO 15423-2 – Scanner & Decoder Performance Testing – 2D
  – ISO 15421 – Master Test Specification
• Bar Code Symbology Specifications
  – ISO 16388 – Code 39
  – ISO 15417 – Code 128
  – ISO 16022 – Data Matrix
  – ISO 15438 – PDF417

  – Team to define guidelines based on narrowing scope and better defining requirements specified in current industry standards – May 31, 2005
• Document and summarize – July 31, 2005
• Project completion – August 31, 2005