ITRS
Assembly and Packaging
2007 Roadmap
Progress is exceeding Roadmap Forecast

- 3D packaging
  - Techniques for 3D packaging are proliferating
- Flexible/wearable electronics
- Wafer thinning
- Wafer level packaging
- System level integration in Package
Major Challenges

- Handling for ultrathin die
- Cost targets for new package types
- Co-Design tools for SiP, 3D packaging, TSV, etc.
- Handling increasing thermal density (particularly for 3D packaging)
- Incorporation of new materials
- Signal integrity for complex SiP
Packaging is now a limiting factor but it is enabling for More than Moore

- Packaging has become the limiting element in system cost and performance.
- The Assembly and packaging role is expanding to include system level integration functions.
- As traditional Moore’s law scaling become more difficult innovation in assembly and packaging can take up the slack.
Moore’s Law Scaling can not maintain the Pace of Progress

Beyond CMOS

Information Processing
Digital content
System-on-Chip (SOC)

Combining SOC & SiP: Higher Value System

More Moore: Scaling

Baseline CMOS: CPU, Memory, Logic

130nm
22nm
32nm
45nm
65nm
90nm

More than Moore: Functional Diversification

Interacting with people and environment
Non-digital content
System-in-Package (SiP)

Baseline CMOS: CPU, Memory, Logic
System Integration

Cost / function vs. Time to market vs. System complexity

- System on Chip
- SiP and 3D Packaging
- Bio-Interface
- Power supply

Source: Fraunhofer IZM
Assembly and Packaging Technical working Group 2007 Focus

We are giving special focus to preparation of a white paper titled:

“The next step in Assembly and Packaging: Systems Level Integration”

Objectives of this white paper
- Catalyze a new SiP chapter ITRS
- Identify needs and gaps
- Identify new technology trends for future SiP
System-in Package (SiP) is a combination of multiple active electronic components of different functionality, assembled into a single unit, that provides multiple functions associated with a system or sub-system. An SiP may optionally contain passives, MEMS, optical components and other packages and devices.
SiP - Situation Analysis

• **Market:** In 2004, 1.89 Billion SiPs were assembled. By 2008, this number is expected to reach 3.25 Billion, growing at an average rate of about 12% per year.

• **Technology:** SiP applications have become the technology driver for small components, packaging, assembly processes and for high density substrates.

• **Growth:** System in Package (SiP) has emerged as the fastest growing packaging technology segment although still representing a relatively small percentage of the unit volume.
# Categories of SiP

<table>
<thead>
<tr>
<th>Horizontal Placement</th>
<th>Wire Bonding Type</th>
<th>Flip Chip Type</th>
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</thead>
<tbody>
<tr>
<td><strong>Stacked Structure</strong></td>
<td></td>
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<tr>
<td>Interposer Type</td>
<td>Wire Bonding Type</td>
<td>Wire Bonding + Flip Chip Type</td>
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<tr>
<td>Interposer-less Type</td>
<td></td>
<td>Flip Chip Type</td>
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<tr>
<td><strong>Embedded Structure</strong></td>
<td>Chip(WLP) Embedded + Chip on Surface Type</td>
<td>3D Chip Embedded Type</td>
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SiP: Multi-level System Integration

SiP may include SoC and other traditional packages

- Sub-system packages
- Stacked thin packages containing passives and active chips
- Mechanical, optical and other non electrical functions
- Complete systems or sub-systems with embedded components
- Bare die
- SoC

Source: Fraunhofer IZM
Wafer Level SiP - Vision

Energy source
ASIC + memories
Embedded passives
MEMS
Cooling

Source: LETI
3D Stacked Die Package

Substrate Base SiP (up to 7/8 die)

- Die thickness: 60 um
- Substrate (BT) thickness: 130 um
- Solder ball Stand-off: 50 um
# ITRS projection for stacked die SiP packages

2014 through 2020

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</thead>
<tbody>
<tr>
<td>Low cost/handheld (# die / stack)</td>
<td>14</td>
<td>14</td>
<td>15</td>
<td>15</td>
<td>16</td>
<td>16</td>
<td>17</td>
</tr>
<tr>
<td>High performance (# die / stack)</td>
<td>5</td>
<td>5</td>
<td>6</td>
<td>6</td>
<td>7</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>Low cost/handheld (# die / SiP)</td>
<td>15</td>
<td>15</td>
<td>16</td>
<td>16</td>
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<td>17</td>
<td>18</td>
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</tbody>
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Limited by thermal density
SiP presents new Design Challenges for signal integrity, power integrity and shielding

- Signal integrity for high density interconnect
  - Cross talk
  - Impedance discontinuities (reflections)
  - Timing skew
  - Parasitic capacitance, resistance and inductance in long traces (inductance change for each layer for wire bonded stacked die)

- Power integrity
  - Voltage drop for high speed signals (lead and trace inductance limits power delivery)
  - Ground noise due to high frequency current variations

- Shielding
  - Radiated noise within the package at high frequency
  - External electromagnetic noise sources
Evolutionary and revolutionary interconnect technologies are needed to enable the migration of microsystems from conventional state-of-art to 3D SiP.
Potential Solutions for Interconnect Challenges
Many variations of SiP package interconnect are in use or in development today.

- POP (WB Type)
- POP (Film Type)
- POP (FC Type + Interposer)
- PIP - Molded
- POP (only for Memory)
- PIP - Spacer
Interconnect Requirements may be satisfied by Wave Guide Optical Solutions

Examples of guided wave optical interconnects for chip-to-chip interconnection.
Low k ILD may Require Improved Underfill or Compliant I/O connections

The use of compliant electrical I/O can potentially eliminate the need for underfill, reducing cost and processing complexity as I/O density rises.
SiP presents new challenges for Thermal management

- High performance generates high thermal density
- Heat removal requires much greater volume than the semiconductor
  - Increased volume means increased wiring length causing higher interconnect latency, higher power dissipation, lower bandwidth, and higher interconnect losses
  - These consequences of increased volume generates more heat to restore the same performance
- ITRS projection for 14nm node
  - Power density >100W/cm²
  - Junction to ambient thermal resistance <0.2 degrees C/W
Thermofluidic Heat Sinks may be the Solution

Examples of thermofluidic heat-sink integration with CMOS technology.
Test Challenges of SiP

- Test cost
- BIST and other Embedded test approaches
- Thermal management
- Test access
- Contactor/Connection issues
- Single chip testing in SiP configurations
- Time to market
<table>
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<tr>
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<th>Impact Area</th>
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<tr>
<td>Test program development</td>
<td>(time to market)</td>
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<tr>
<td>Load board design</td>
<td>(time to market and cost)</td>
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<tr>
<td>BIST and other DFT</td>
<td>(time to market and cost)</td>
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<tr>
<td>ATE configuration</td>
<td>(cost)</td>
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<tr>
<td>Power requirements</td>
<td>(cost/performance)</td>
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<tr>
<td>Thermal management</td>
<td>(cost/performance)</td>
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<tr>
<td>Contactor/ Connection</td>
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<tr>
<td>Round trip delay</td>
<td>(cost/performance)</td>
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<tr>
<td>High frequency</td>
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There are several regulatory activities resulting from environmental considerations that will impact the future SiP technology as well as all other parts of the electronics industry.

These include:

ELV: Directive on end-of-life vehicles
RoHS: Directive on the restriction of the use of certain hazardous substances in electrical and electric equipment
WEEE: Directive on waste electrical and electronic equipment
EuP: Directive on the eco-design of Energy-using Products
REACH: Registration, Evaluation and Authorization of Chemicals
Thank You