iNEMI SOLDER PASTE DEPOSITION PROJECT - FIRST STAGE REVIEW
OPTIMIZING SOLDER PASTE PRINTING FOR LARGE AND SMALL COMPONENTS

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ABSTRACT
The widely recognized industry standard IPC-7525 has been used as the starting point for an experimental program that explores the effect of varying the keep out distance for 0201 and 0402 chip components, CSP and SOP with pitches down to 0.4mm, and larger components represented by CCGA. Other variables that were included in the experimental program to determine if they had an effect on the sensitivity of paste transfer to keep-out distance included stencil type, step height and solder type.

In the first stage of the project the printing to each pad was measured with automated 3D SPI systems and optimum combinations of parameters identified by statistical analysis. In this paper the authors will explain the methodology chosen to achieve the project objectives and indicate the direction of likely future work. Early results indicate that a key objective of the project, to provide evidence to support the case for a reduction in the keep out distances below the current industry standard, might be achievable.
Key words: Miniature and fine pitch components, keep-out distance, transfer efficiency, consistency

INTRODUCTION
The widening range of component sizes on many printed board assemblies is creating a dilemma for the paste application process. The trend towards smaller chip components and finer pitches on IC packages means that smaller volumes of solder paste are required on each pad if problems of tombstoning, mid-chip balling and bridging are to be avoided. However, in most of these assemblies there are also large components that require substantial volumes of solder to form joints with the required electrical and mechanical properties. For some components and finishes, extra solder paste is needed to compensate for potential coplanarity issues. Given the constraints on the area ratio, if an adequate transfer efficiency is to be achieved the extent to which the solder paste volume can be controlled by varying the aperture dimensions is limited. While there is hope that alternative application methods will make it possible to optimize solder paste volume for each pad, for the time being the most cost effective solution is to use a step stencil in which stencil thickness is varied to fine tune the paste volume to the requirements of the component terminations. This solution imposes a constraint on the layout to the extent that components with similar requirements for solder paste volume have to be grouped. However, a greater concern in assemblies in which space is at a premium is the "keep-out" distance required on either side of the step. Large "keep-out" distances used to accommodate various stencil thicknesses represents a significant loss of area available for component mounting. In this first project of iNEMI Asia, the objective is to determine for a representative range of components what the minimum distance on each side of the step can be without compromising the quality of the reflowed solder joint.

TEST BOARD DESIGN
General Specification

Board size	360.0mm x 340.0mm x 2.5mm
Board layer	4 layers
Surface finish	OSP
Board material	FR-4

Table 1. Test Board Specification

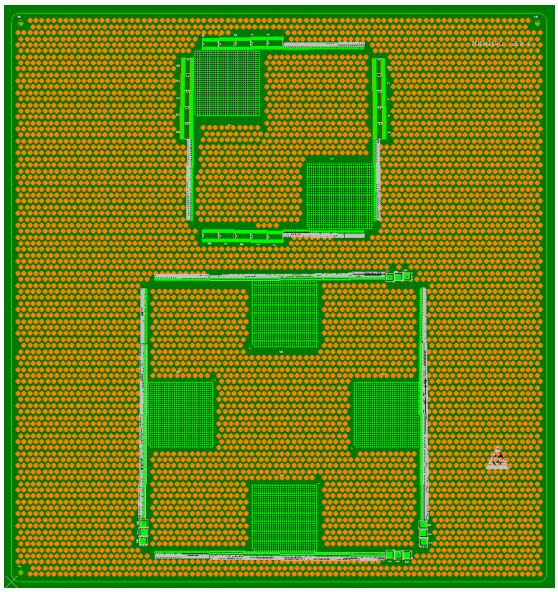

Figure 1. Test Board Layout

Layout
The keep-out distance for step stencils has been described in IPC-7525. For the purpose of this project boards were designed to provide a range of keep-out distances for 0201, 0402 and 0.4mm pitch SOP and CSP components (Table 2). To assess the effect of printing direction components were arranged around all four sides of the stepped area.

EXPERIMENT MATRIX DESIGN
Given the project objective of determining the minimum keep-out distance that can be used in practical application

the experimental program covers a range of process variables typically encountered in commercial production (Table 3).

Component Type	Keep-out Distance (mil)	KD Levels	Component Layout
0201	24，32，40，43，48，51，56，59，67，75	10	around step/ outside
0402	24，32，40，48，56，56’，64，72，80，88	10	around step/ outside
0.4mm pitch SOP	24，32，40，48，56，252，260，268，276，284	10	around step/ outside
0.4mm pitch CSP	closest is 24，furthest is 184，interval is 8	21	around step outside
1.27mm pitch CCGA	/	/	around step /inside

Table 2. Test board layout

Notes:
1. Keep-out distance: The space between the pads of the miniature and fine pitch components and the component requiring more solder
2. KD (Keep-out distance) levels: The number of levels of keep-out distance for each component;
3. Component layout: The direction and location of each component in relation to the stencil step.

Factor	Level 1	Level 2
Solder type	Tin-lead (Sn63Pb37) Indium NC-SMQ92H ROL0	Lead-free (SAC305) Indium 8.9 ROL1
Solder particle size	Type 3	Type 4
Stencil fabrication	Laser-cut	Electroformed
Stencil type	Step-up	Step-down
Step height（the original stencil thickness is 0.12mm）	0.06mm	0.03mm

Table 3. Experiment Factors and Levels

The experiment matrix is as Table 4:

EXPERIMENTAL PROCEDURE

OSP Thickness Measurement

The solderability of an OSP finish is known to be affected by the roughness of the copper and its ability to survive a reflow profile. It is known that OSP thickness may vary due to the Cu roughness. FIB was used to measure OSP thickness since this method can accurately reveal the relationship between the OSP thickness and copper roughness.

Figure 2 shows the result of OSP thickness measurement on CCGA and CSP initially and after the first and second reflow. The greater initial thickness of the OSP on the CSP pads is thought to be due to their smaller size. After the first reflow, there is not sufficient loss of coating thickness to compromise solderability even on the copper peaks where the coating is thinner. After the second reflow there is significant loss of coating thickness but there is still sufficient coating on the peaks to protect the overall solderability of the pads so that it is not expected that solderability will be a factor influencing results in the later assembly stage of the project.

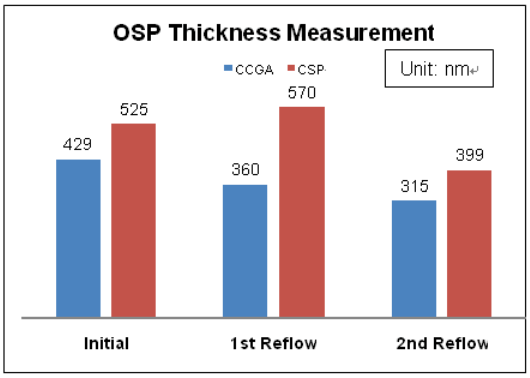

Figure 2. OSP Thickness Measurement

GR&R

GR&R was performed to determine the repeatability of the solder paste inspection equipment before starting the experiment. It was considered that results should be consistent within 10%.of the measured value A single board was printed and then inspected 9 times, the deposit height and volume results for BGA pads are summarized in Table 5. The repeatability was calculated as follow:

Repeatability = 6 *σ/ (0.8 * average value)

Where σ＝standard deviation of 9 samples

Average value = the average value of 9 samples

0.8 presents ± 40% process window

The repeatability was found to satisfy the set criterion (Table 5)

Printing Parameter Settings

Initial settings for print speed, squeegee pressure and separation speeds on the Speedline Technologies Inc “Accela” printer were those recommended in the solder paste data sheet. Adjustments were then made on the

basis of transfer efficiency, deposit shape and cleaning of the stencil surface with the final settings being as listed in Table 6. To avoid any variation due to squeegee stroke direction, only the front to rear direction was used.

	Average Repeatability	
BGA Location	**Height**	**Volume**
U21	3.23%	1.80%
U22	2.21%	1.76%
U23	2.03%	1.41%
U24	2.33%	1.37%
U25	1.74%	1.19%
U26	2.07%	1.33%
Overall average	2.27%	1.48%

Table 5. 3D-SPI Repeatabilty Results

For run 1～4：

Print speed	75 mm/sec
Squeegee pressure	8 kg
Separation speed	5.5 mm/sec
Separation mode	Continuous

For run 5～16：

Print speed	35 mm/sec
Squeegee pressure	8 kg
Separation speed	5.5 mm/sec
Separation mode	Continuous

Table 6. Printer Settings

These settings were kept constant for all the remaining run orders (stencils) with careful checking of the print quality after each stencil change. To enhance statistical significance there were three repeats of each run order so that a total of 48 boards were printed with every pad being inspected by the 3D SPI. Solder paste transfer efficiency and consistency were also recorded for analysis.

DATA ANALYSIS

DoE Run

The DoE analysis was performed on each component surrounding the steps. These components are 0402, SOP, CSP, and 0201. The DoE analysis of 0402 is presented here as an example.

0402 component had 10 levels of KD. The closest, KD1, was 24mil. The furthest, KD10, was 88mil. Trial plots of 0402 data at each KD, grouped by DoE run order, orientation, and side indicate that ORT has a significant effect on TE (transfer efficiency) and deposit height, while the side does not have such a significant effect where:

RO: Run Order;
ORT: Orientation of the component direction in relation to the step. ORT1 means the left and right side of the step while ORT2 means the top and bottom side.
Side: The side of the step. For example, ORT1 Side1 means the left side of the step.

Figures 3 and 4 are examples of such trial plots which represent the two extremes of KD. It can be seen that the TEs are almost the same for Side 1 and Side 2 for each run, but that there is a significant difference between ORT1 and ORT2 for most runs. This means ORT should be a separate factor, but the data of both sides may be able to be combined to simplify the DoE analysis.

Among the five main DoE factors and the ten possible two-factor interactions, step appears to be the most significant factor in determining TE for both ORT1 (Fig 5) and ORT2 (Fig 6). The next most significant factors appear to be step height for ORT1 (Fig 5) and then solder paste and solder type combinations (Fig 6).

KD Trend Analysis

The line plot, which directly presents the trend for each run and differences between runs, was also used in the analysis of the results. Transfer efficiency and consistency will be particularly considered here and results for 0402 are again used as examples (Figures 7 and 8).

Figure 7 shows the line plot of TE for 0402:

- KD is not the significant factor in a single run, which means TE varies little with increasing KD;
- TEs differ between some runs, especially Runs 13 and 14 which have TE values higher than other runs.

Figure 8 shows the line plot of transfer consistency for 0402:

- KD is not the significant factor in a single run, which means TC varies little with increasing KD;
- TC differs little between runs, but Run 10 is an exception;
- There is a large variation in TC for all 16 runs on the left of the step at 56mil KD. The cause has been the subject of discussion by the project team and attributed to differences in the stencil fabrication.

0201, 0.4mm pitch CSP and SOP have also been analysed using this method and the results are summarized in Table 7.

Summary of the First stage

Based on the analysis above the following conclusions have been drawn:

- While it might be expected on the basis of common sense that the farthest KD should yield a better TE

and deposit height than the closest KD, the trend analysis shows the KD has little or no effect on TE and height for 0402 and SOP type pads. Variations between DoE runs are greater than variation with the KD over the range studied.

- For all keep-out distances and run orders orientation has a significant effect. ORT1 (aperture at the side of step) always gives higher TE than ORT2 (aperture at the front/rear of the step). But with the same orientation Side has little or no effect.

- From the overall DoE analysis, the project team saw the following factors as important:
  - Solder paste type,
  - Stencil type,
  - Step down/up and
  - Step thickness.

  That was expected and confirmed that the team had chosen the right factors and/or level setting.

- An unexpected result was that some DoE runs yielded TEs significantly different from others. The cause of this excessive swing in the response variable is unknown at this point and more investigation by the team is needed to understand and explain the cause.

Next stage plan

Based on the results of the first stage printing experiments, assembly verification will be undertaken in China during August 2009 and the printing result and the assembly result compared. Finally the optimum keep-out distances for each component type in various applications will be obtained so accomplishing the objective of this project.

Acknowledgement

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Run order	Solder type	Solder particle size	Stencil fabrication	Stencil type	Step thickness/mm
1	Lead-Free	Type 4	Laser-cut	Step-down	0.03
2	SnPb	Type 3	Laser-cut	Step-down	0.03
3	SnPb	Type 4	Electroformed	Step-up	0.06
4	Lead-Free	Type 3	Electroformed	Step-up	0.06
5	Lead-Free	Type 4	Laser-cut	Step-up	0.06
6	SnPb	Type 3	Laser-cut	Step-up	0.06
7	SnPb	Type 4	Electroformed	Step-down	0.03
8	Lead-Free	Type 3	Electroformed	Step-down	0.03
9	Lead-Free	Type 3	Laser-cut	Step-up	0.03
10	SnPb	Type 4	Laser-cut	Step-up	0.03
11	SnPb	Type 3	Electroformed	Step-down	0.06
12	Lead-Free	Type 4	Electroformed	Step-down	0.06
13	Lead-Free	Type 3	Laser-cut	Step-down	0.06
14	SnPb	Type 4	Laser-cut	Step-down	0.06
15	Lead-Free	Type 4	Electroformed	Step-up	0.03
16	SnPb	Type 3	Electroformed	Step-up	0.03

Table 4. Experiment Matrix

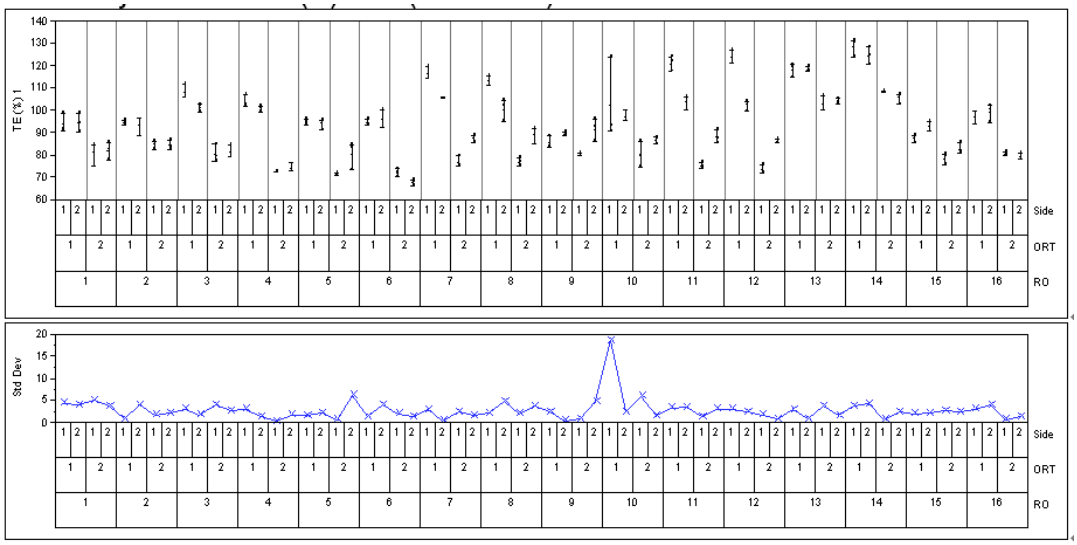

Figure 3. Trial plot of 0402 TE and Std Dev for KD at 24mil (closest KD)

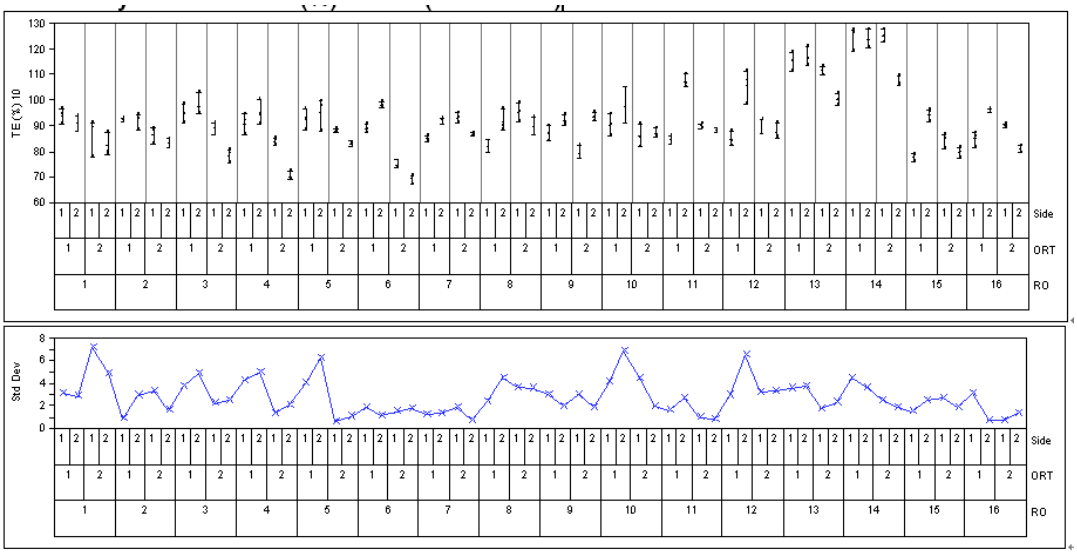

Figure 4. Trial plot of 0402 TE and Std Dev for KD at 88mil (furthest KD)

Term	t Ratio
Step[up]	-2.027166
Step thick	1.937066
Solder paste[SnPb]*Solder type[T4]	1.406759
Stencil type[Efab]	-1.022193
Stencil type[Efab]*Step[up]	1.011305
Step[up]*(Step thick-0.045)	-0.980517
Stencil type[Efab]*(Step thick-0.045)	-0.893559
Solder paste[SnPb]	0.666667
Solder type[T4]*Stencil type[Efab]	-0.436008
Solder type[T4]	0.331564
Solder type[T4]*(Step thick-0.045)	0.229221
Solder paste[SnPb]*Stencil type[Efab]	-0.189535
Solder type[T4]*Step[up]	-0.184329
Solder paste[SnPb]*Step[up]	0.091837
Solder paste[SnPb]*(Step thick-0.045)	-0.060730

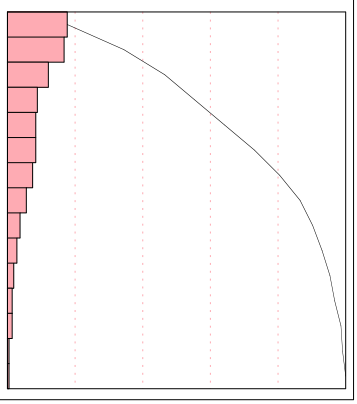

Figure 5. Pareto for ORT 1, TE

Term	t Ratio
Step[up]	-2.928274
Solder paste[SnPb]*Solder type[T4]	2.563033
Step[up]*(Step thick-0.045)	-2.090952
Stencil type[Efab]*Step[up]	1.564716
Stencil type[Efab]*(Step thick-0.045)	-1.440878
Stencil type[Efab]	-1.334927
Solder type[T4]*(Step thick-0.045)	0.923296
Step thick	0.770655
Solder type[T4]	0.562679
Solder paste[SnPb]*Step[up]	-0.414873
Solder paste[SnPb]	0.377273
Solder type[T4]*Stencil type[Efab]	-0.363636
Solder type[T4]*Step[up]	0.283745
Solder paste[SnPb]*Stencil type[Efab]	0.122658
Solder paste[SnPb]*(Step thick-0.045)	0.004263

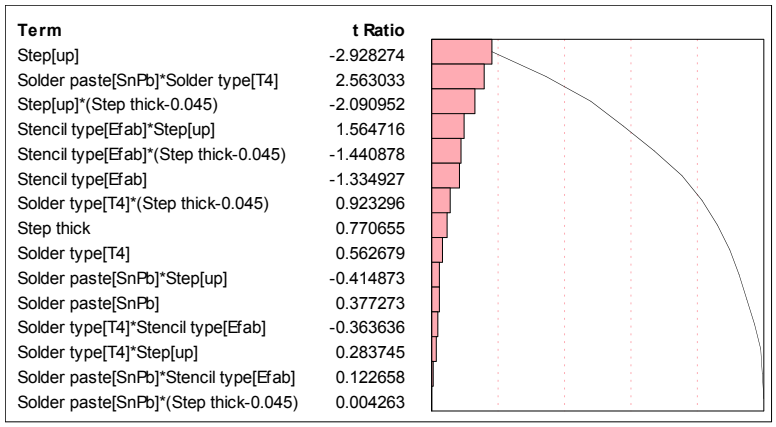

Figure 6. Pareto for ORT 2, TE

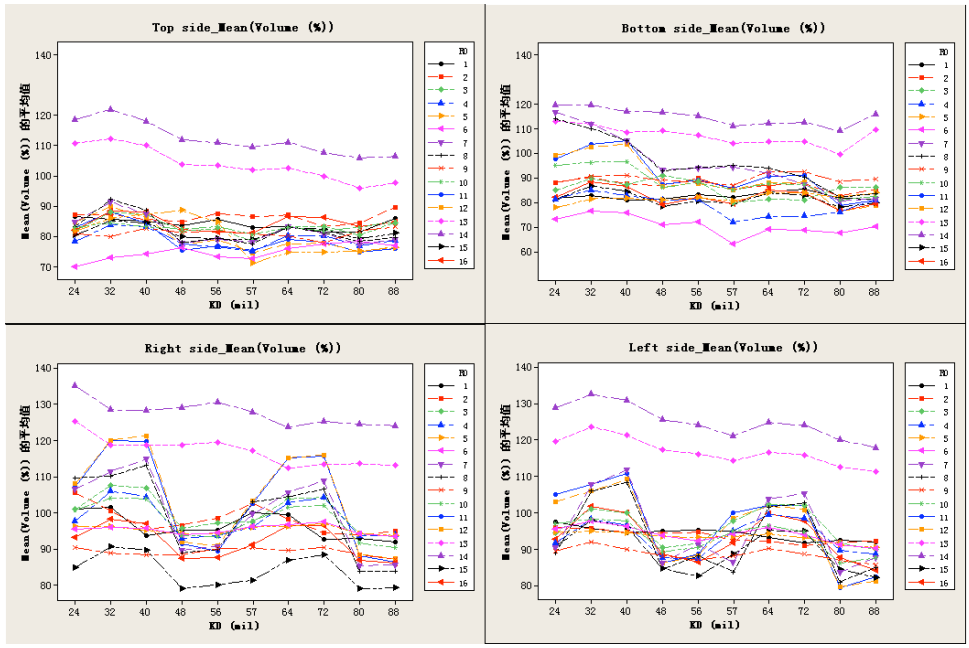

Figure 7. TE of 0402

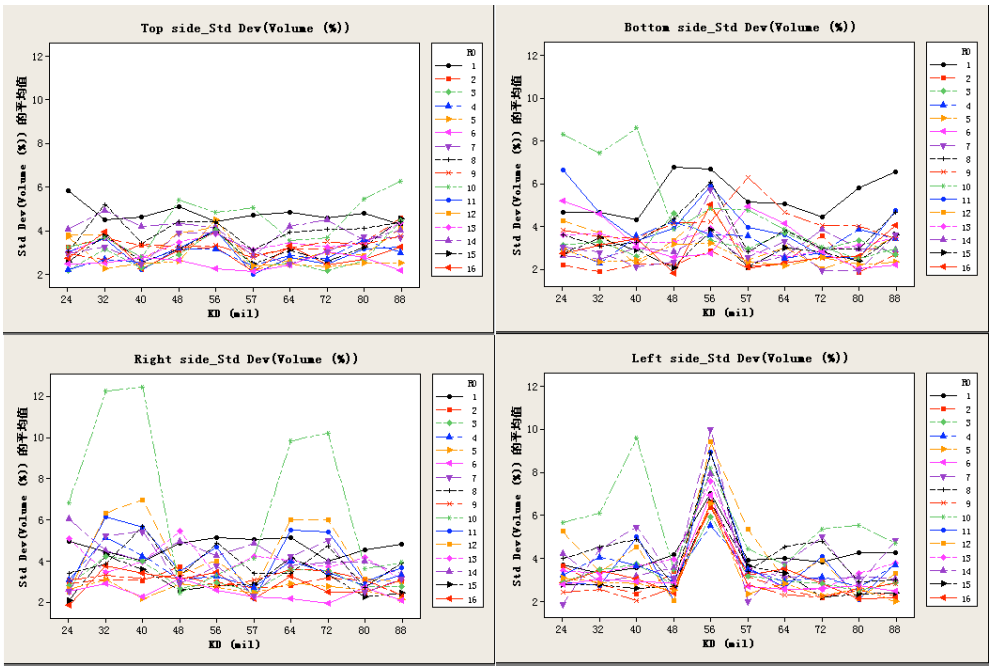

Figure 8. TC of 0402

Component Type	Transfer Efficiency	Transfer Consistency
0201	No clear trend in a single run; Notable differences between runs.	No clear trend in a single run; Notable differences between runs
0.4mm pitch SOP	In a single run TE clearly reduces with increasing KD; Notable difference between runs.	No clear trend in a single run; Not much difference between runs
0.4mm pitch CSP	Considerable variation in TE with increasing KD in some runs; The trend is more consistent between runs, that is, the trend of TE with increasing KD although there are still large differences in the absolute values.	No clear trend in a single run; Not much difference between runs

Table 7. Transfer Efficiency and Consistency for 0201、0.4mm Pitch CSP and SOP