



iNEMI

International Electronics Manufacturing Initiative

**iNEMI
Solder Paste
Deposition Project**

*Presented by:
Runsheng Mao,
Indium Corporation of America
Clinton, NY, USA
On behalf of Team Leader:
Shoukai Zhang
Huawei Technology
ShenZhen, China
October 6, 2009*

Advancing manufacturing technology

Authors

- **Shoukai Zhang, Huawei Technology, Shenzhen, China**
- **Rita Mohanty, Ph.D., Speedline, Franklin, MA, USA**
- **Xiaodong Jiang, Alcatel-Lucent Shanghai Bell Shanghai, China**
- **Runsheng Mao, Ph.D. Indium Corporation, Clinton, NY, USA**
- **Chiko Yu, Integrated Service Technology, Hsinchu, Taiwan**
- **Chuan Xia, Cisco Systems, Hong Kong, China**
- **Keith Sweatman, Nihon Superior Co., Ltd. Queensland, Australia**
- **Desmond Teoh, Celestica, Suzhou, China**
- **Haley Fu, Ph.D., iNEMI, Shanghai, China**
- **Jim Arnold, Ph.D., iNEMI, Mesa, AZ, USA**

Outline

- ➔ **Introduction**
 - **DOE**
 - **Experimental**
 - **Data Analysis**
 - **Stage Summery**
 - **Future Plan**

Introduction

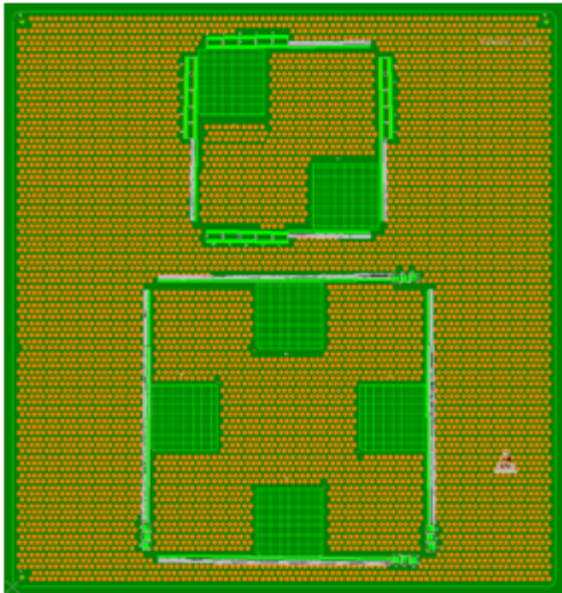
- **The widely recognized industry standard IPC-7525 has been used as the starting point for this project that explores the effect of varying the keep out distance (KD) for small components 0201 and 0402 chips, 0.4mm CSP and 0.4mm SOP. Large component is represented by CCGA.**
- **Other DOE factors which may have effect on the paste transfer included stencil type, step type, step thickness and solder paste type.**

Outline

- **Introduction**
- ➔ **DOE**
- **Experimental**
- **Data Analysis**
- **Stage Summery**
- **Future Plan**

Test Board Spec

Size	360.0mm×340.0mm×2.5mm
Layer	4
Surface finish	OSP
Material	FR-4



Board Layout

Component	KD/mil	KD level	Layout
0201	24 , 32 , 40 , 43 , 48 , 51 , 56 , 59 , 67 , 75	10	Outside
0402	24 , 32 , 40 , 48 , 56 , 64 , 72 , 80 , 88	9	Outside
0.4mm pitch SOP	24 , 32 , 40 , 48 , 56 , 252 , 260 , 268 , 276 , 284	10	Outside
0.4mm pitch CSP	Min 24 , Max 184 , Step 8	21	Outside
1.27mm pitch CCGA	/	/	Inside

DOE

Factor

Solder paste

Powder size

Stencil fabrication

Step type

Step thickness
(none-step area thickness is 0.12mm)

Level

Tin-lead

Lead-free

Type 3

Type 4

Laser-cut

Electroformed

Step-up

Step-down


0.03mm

0.06mm

DOE

Run order	Solder type	Solder particle size	Stencil fabrication	Stencil type	Step thickness/mm
1	Lead-Free	Type 4	Laser-cut	Step-down	0.03
2	SnPb	Type 3	Laser-cut	Step-down	0.03
3	SnPb	Type 4	Electroformed	Step-up	0.06
4	Lead-Free	Type 3	Electroformed	Step-up	0.06
5	Lead-Free	Type 4	Laser-cut	Step-up	0.06
6	SnPb	Type 3	Laser-cut	Step-up	0.06
7	SnPb	Type 4	Electroformed	Step-down	0.03
8	Lead-Free	Type 3	Electroformed	Step-down	0.03
9	Lead-Free	Type 3	Laser-cut	Step-up	0.03
10	SnPb	Type 4	Laser-cut	Step-up	0.03
11	SnPb	Type 3	Electroformed	Step-down	0.06
12	Lead-Free	Type 4	Electroformed	Step-down	0.06
13	Lead-Free	Type 3	Laser-cut	Step-down	0.06
14	SnPb	Type 4	Laser-cut	Step-down	0.06
15	Lead-Free	Type 4	Electroformed	Step-up	0.03
16	SnPb	Type 3	Electroformed	Step-up	0.03

Outline

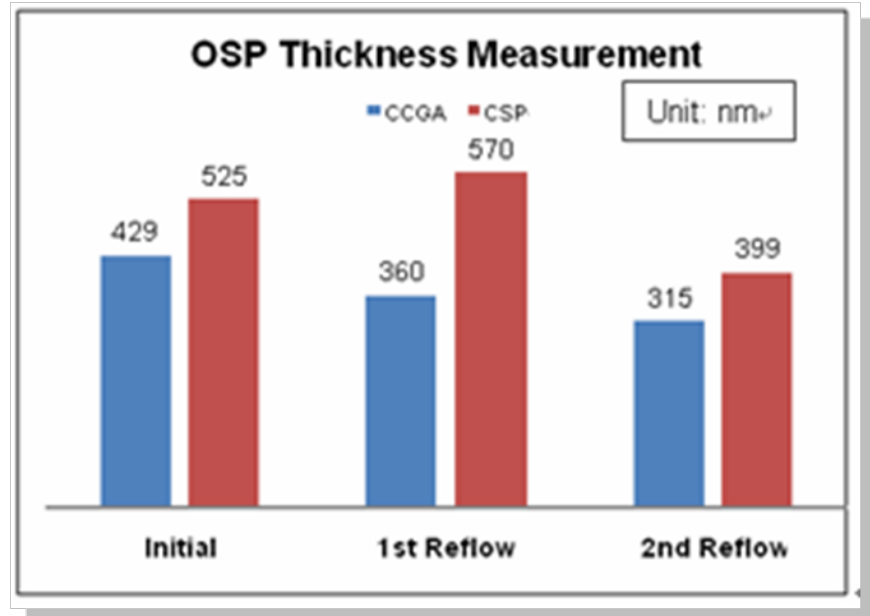
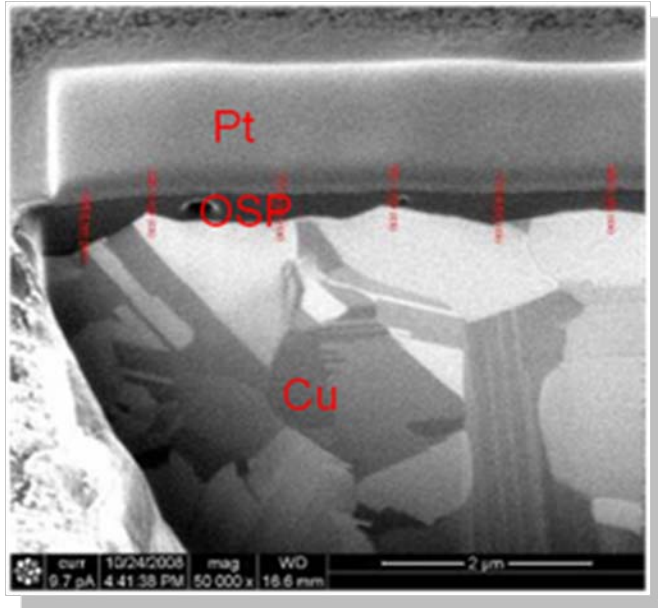
- **Introduction**
- **DOE**
-  **Experimental**
- **Data Analysis**
- **Stage Summery**
- **Future Plan**

Experimental

- **Solder pastes**
 - **SnPb: NC-SMQ92H (ROL0) with Sn63 (Indium Corporation)**
 - **Lead-free: Indium8.9 (ROL1) with SAC305 (Indium Corporation)**
- **Printer**
 - **Accela (Speedline)**
- **3D SPIs**
 - **Koh Young KY-3030**
 - **Cyber Optics SE-300**

Experimental

OSP Thickness Measurement



- Method: FIB
- The difference of pad thickness $< 0.5 \mu$, no effects on printing ;
- After double reflow, the OSP can still satisfy the solder ability.

Experimental

GR&R

BGA Location	Average Repeatability	
	Height	Volume
U21	3.23%	1.80%
U22	2.21%	1.76%
U23	2.03%	1.41%
U24	2.33%	1.37%
U25	1.74%	1.19%
U26	2.07%	1.33%
Overall average	2.27%	1.48%

Repeatability = $6 \times \sigma / (0.8 \times \text{average value})$


Where σ = standard deviation of 9 samples
Average value = the average value of 9 samples

0.8 represents $\pm 40\%$ process window

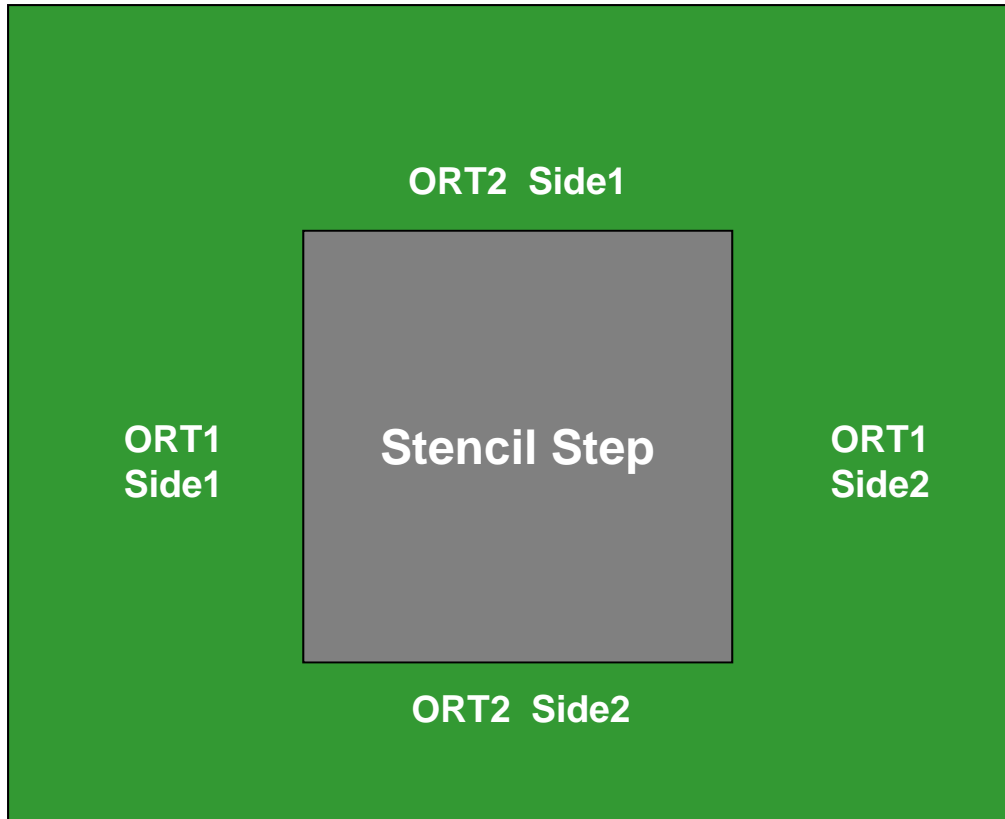
The repeatability was found to satisfy the set criterion

- Number of samples in each DOE run : 3
- Total PCBs printed : $16 \times 3 = 48$
- Each pad was inspected with 3D SPI. The paste volume, transfer efficiency (V%), paste height, and bridge information were recorded for later analysis

Outline

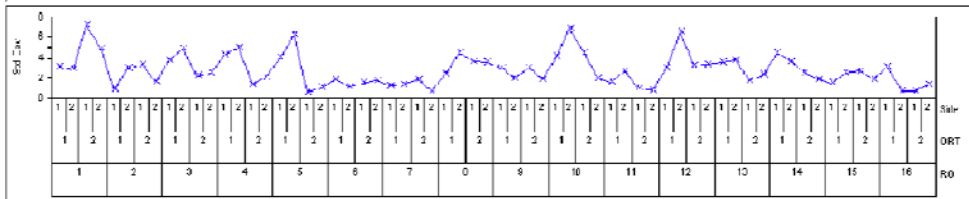
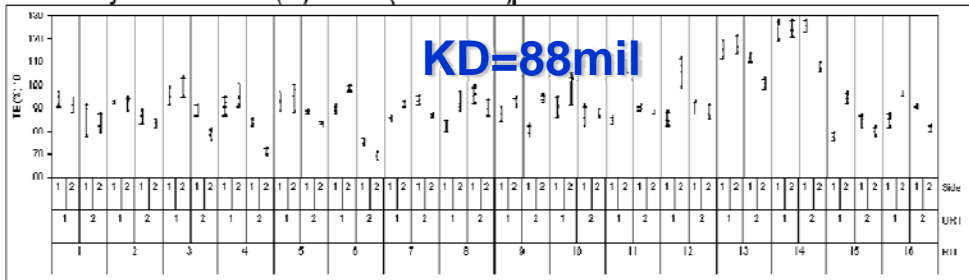
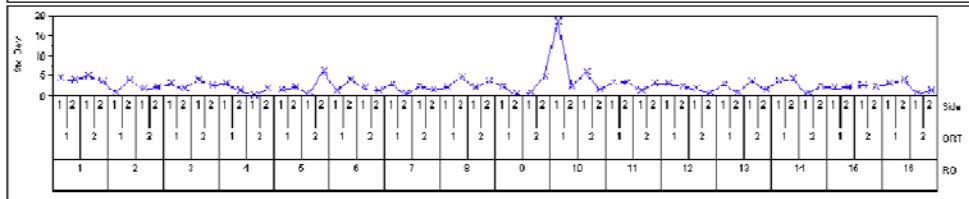
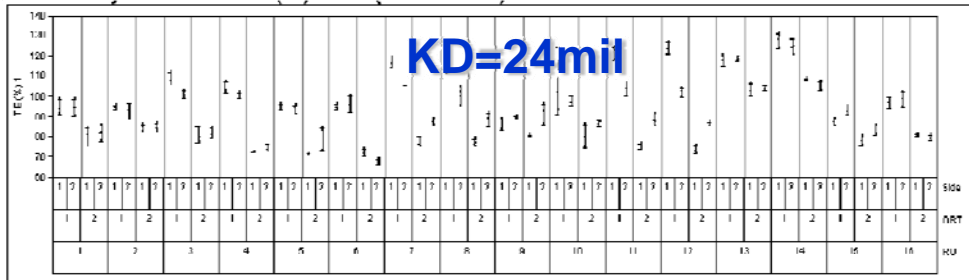
- **Introduction**
- **DOE**
- **Experimental**
-  **Data Analysis**
- **Stage Summery**
- **Future Plan**

Data Analysis



- **ORT** — Orientation
ORT1 – left and right
ORT2 – top and bottom
- **Side** — left (1) or right (2) for ORT1, top (1) or bottom (2) for ORT2

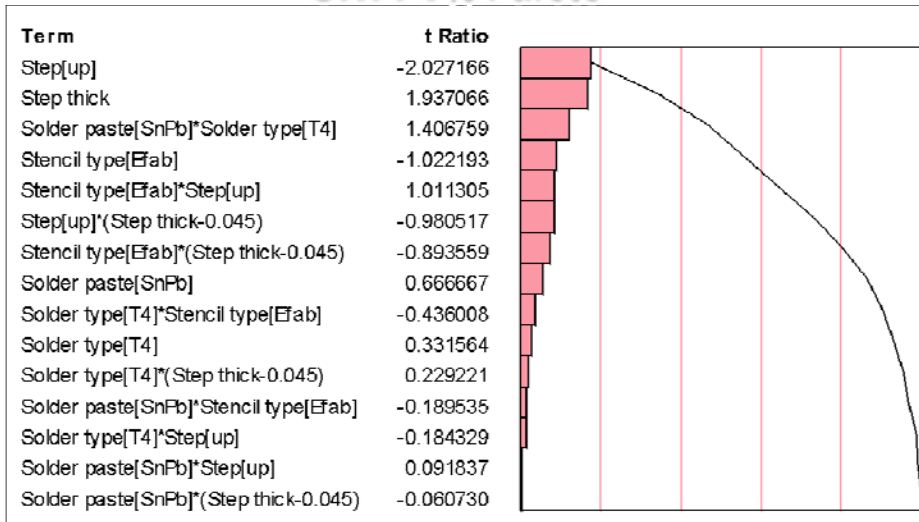
Data Analysis



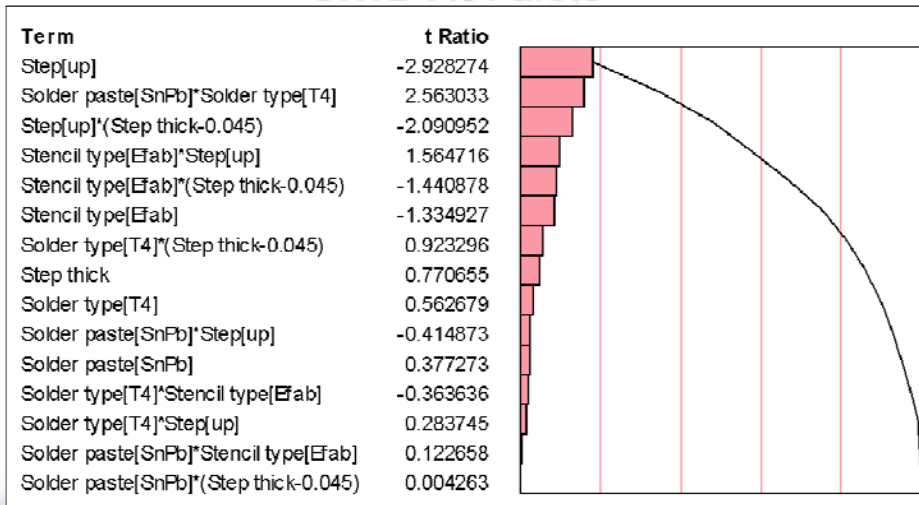
- The DOE analysis was performed on each component surrounding the steps, i.e. 0402, SOP, CSP, and 0201.
- 0402 is presented here as an example.
- 0402 Average TEs :
 - TEs between side 1 and side 2 have almost no difference, so the 2 side data can be combined
 - TEs between ORT1 and ORT2 have significant difference, so the ORT1, ORT2 data need to be analyzed separately.
- 0402 Std Dev of TEs :
 - Usually < 10%.

Data Analysis

ORT1 V% Pareto



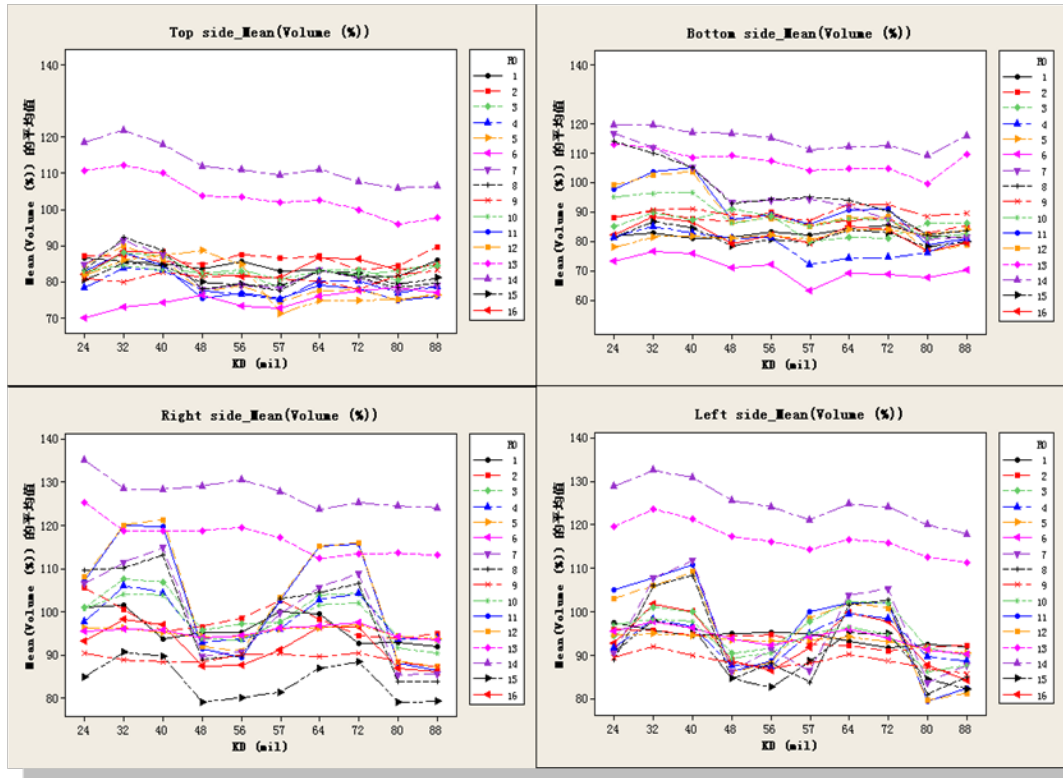
ORT2 V% Pareto



- Among the five main DOE factors (solder paste, powder size, stencil fabrication, step type, and step thickness) and the ten possible two-factor interactions, most significant factor on ORT1 V% is step type (up and down), followed by step thickness
- For ORT2 V%, the most significant factor is step type, followed by the interaction of solder paste and powder size
- In summery, step type is a significant factor

Data Analysis

KD trend analysis of 0402 Average TEs

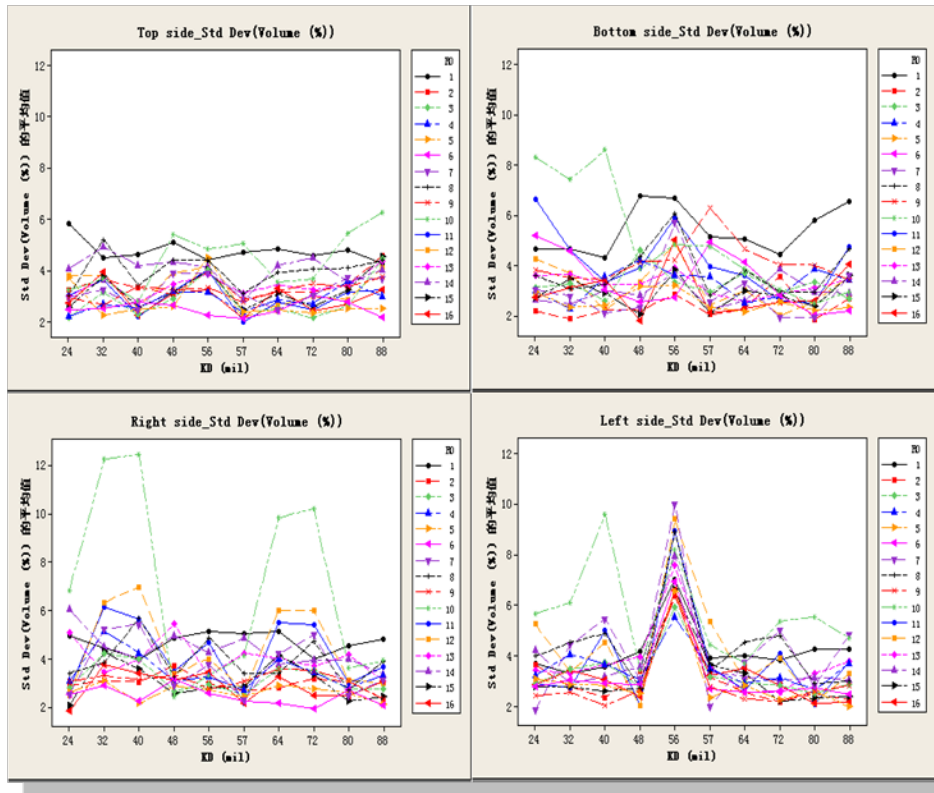


0402 TE vs. KD

- KD may not be the most significant factor in a single run, because TE varies little with increasing KD;
- TEs differ between some runs, especially Runs 13 and 14 which have TE values higher than other runs.

Data Analysis

KD trend analysis of 0402 transfer consistency (std dev of TEs)




0402 TC vs. KD

- KD may not be the most significant factor in a single run, which means TC varies little with increasing KD;
- TC differs little between runs, but Run 10 is an exception – high std dev;
- There is a large variation in TC for all 16 runs on the left of the step at 56mil KD. The cause has been the subject of discussion by the project team and attributed to differences in the stencil fabrication.

Data Analysis

Component	Transfer Efficiency	Transfer Consistency
0201	No clear trend in a single run; Notable differences between runs.	No clear trend in a single run; Notable differences between runs
0.4mm pitch SOP	In a single run TE clearly reduces with increasing KD; Notable difference between runs.	No clear trend in a single run; Not much difference between runs
0.4mm pitch CSP	Considerable variation in TE with increasing KD in some runs; The trend is more consistent between runs, that is, the trend of TE with increasing KD although there are still large differences in the absolute values.	No clear trend in a single run; Not much difference between runs

Outline

- **Introduction**
- **DOE**
- **Experimental**
- **Data Analysis**
-  **Stage Summery**
- **Future Plan**

Stage Summary (1)

- In theory, the larger the KD, the more stable TE and TC should be obtained
- Initial trend analysis shows the KD has little effect on TE and TC for 0402 and SOP type pads within the chosen KDs. Variations between DOE runs are greater than variation with the KD over the range studied
- The TE of some runs (run 13 and 14) are much higher than other runs, and the TE decreases significantly with the increase of KD
- Variations between DOE runs are greater than variation with the KD

Stage Summary (2)

- **Orientation (ORT) is a significant factor**
- **The TEs in the left and right sides (ORT1) are always higher than the top and bottom sides (ORT2)**
- **The difference of TEs between left side and right side is small, and so is the difference between top and bottom side**

Stage Summary (3)

- **Based on DOE analysis, the project team considers following factors are significant**
 - **Step type (up or down)**
 - **Step thickness**
 - **The interaction of solder paste type (SnPb or lead-free) and the particle size (type 3 or type 4)**

Outline

- **Introduction**
- **DOE**
- **Experimental**
- **Data Analysis**
- **Stage Summery**
- ➔ **Future Plan**

Future Plan

- **Assembly verification was completed in September 2009 and data analysis is underway**
- **The results from assembly will be analyzed and compared to earlier printing results**
- **Finally, the optimum keep-out distances for each component will be obtained so that the KD in high density PCBs may be reduced**

Acknowledgements

The authors appreciate the close cooperation between Huawei, Alcatel-Lucent, Speedline, Indium Corporation, IST, Cisco, Rohm & Haas, Nihon Superior, Celestica and iNEMI in this project and extend their thanks to Photo Stencil and all the engineers involved for their great support.



www.inemi.org

Email contacts:

Shoukai Zhang

skzhang@huawei.com, Huawei Technology

Dr. Haley Fu

haley.fu@inemi.org, iNEMI



iNEMI[®]
Advancing manufacturing technology