Packaging Substrate Workshop Wrap Up

Bob Pfahl, iNEMI
Breakout Session (ends 10:30 am)

• **Introduction & your expectation**
  – Issues & Root cause (material properties) of warpage & solutions
    • 1st level chip joint yield (from assembly) due to strip warpage vs reflow, warpage level at substrate level (core warpage)
    • 2nd level SMT assembly
  – Substrate characteristics (Tg, curve temp vs reflow temp & reflow response)
  – Core material properties
  – PoP & CSP (fine pitch) assembly process
  – Board level SMT assembly yield (room temp vs reflow)
  – Warpage measurement metrology (substrate/packaging) & specification

• **Identity gaps, brainstorm options & priorities**
  – Strip vs single substrate
  – PoP (JEDEC spec only @ RT, top/bottom warpage) & CSP (fine pitch) assembly process

• **Recommendation of iNEMI projects (9:55am)**
  – Qualification criteria (acceptance, measurement method) including substrate, pkg, board levels
  – Identify key material properties (core, core/SM thickness, substrate, design (Cu trace/via), pkg assembly) and key contributors (die size, thickness) which impacts 1st level and 2nd level for different applications
    • Factor: process parameters (UF, MC etc), reflow profile, pkg pitch, PCB warpage improvement

• **Define project scope draft proposal (10:25am)**
Project 1

• Qualification criteria (acceptance, measurement method) including substrate, pkg, board levels
  – Problem statements:
    • The current standard is not adequate to predict good yield results at 1st and 2nd level assembly
    • Measurement methods (dimensional and test) not common
  – Objectives
    • Define the qualification method and criteria e.g. sample size, precondition, variations of material and processes (1st and 2nd level).
    • Establish measurement methods
  – Expected Outputs
    • Procedure and criteria reference for OEM and suppliers
Project 2

• Identify key material properties (core, core/SM thickness, substrate, design (Cu trace/via), pkg assembly) and key contributors (die size, thickness) which impacts 1st level and 2nd level for different applications
  • Factor: process parameters (UF, MC etc), reflow profile, pkg pitch, PCB, environmental factors (shipping and storage; moisture effect).

– Problem statements:
  • No clear understanding of the key contributors to the 1st and 2nd level assembly

– Objectives
  • Understand the key contributors
  • Establish understanding to modulate the key contributors

– Expected Outputs
  • A set of primary parameters (materials, design and processes) and the working window to control the warpage through supply chain
  • Recommendation/guidelines for shipping and storage.
Miniaturization

Facilitator: Hamid Azimi, Intel
Presenter: Claudia Beckering, Epcos
Who participated?

- Hamid Azimi, Intel (Facilitator)
- Charan Gurumurthy, Intel (Facilitator)
- Claudia Beckering, Epcos (Presenter)
- Kenya Misu, DuPont
- JY Kim, Amkor
- Steve Yang, NanYa
- Takada-san, Ibiden
- Nakamura-san, Ajinomoto
- Tsuriya-san, Freescale
- Philippe Bourgeon, TI
- Luis Rivera, TI
- YG Ko, SEMCO
Brainstorm

• BP < 130 micron; First level interconnect enabling
• L/S < 10/10 micron; tolerances, Layer count
• L/S finer on laminate vs. Build up
• Electrical Performance Requirements
• Package on Package (POP) – generic via and land diameter; via density
• Embedding active and passives
• Materials
• FC – CSP – fine L/S Challenge
• Wafer level packaging – backend Si technology for wiring substrate
• TSV (through Si via)
• Litho alignment/SR registration
• Metrology and manufacturing equipment
• Testing and Inspection
• PTH diameter
• Placement accuracy for component on mother board
• Z- height (Thinner substrate / Coreless )
• Surface finish / Solder joint reliability
• SR defined or pad defined
• Warpage (other team) – rigidity of substrate
• **Miniaturization = Wiring density**
  • BP < 130 micron; First level interconnect enabling
  • L/S < 10/10 micron; tolerances, Layer count
  • L/S finer on laminate vs. Build up
  • Electrical Performance Requirements
  • Package on Package (POP) – generic via and land diameter; via density
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  • Wafer level packaging – backend Si technology for wiring substrate
  • TSV (through Si via)
  • Litho alignment/SR registration
  • Metrology and manufacturing equipment
  • Testing and Inspection
  • PTH diameter

• Assembly interaction challenges (holistic approach team – Mario)
  • Placement accuracy for component on mother board
  • Z- height (Thinner substrate / Coreless )

• Reliability (holistic approach team – Mario):
  • Surface finish / Solder joint reliability
  • SR defined or pad defined

• Warpage (other team) – rigidity of substrate
Wiring Density Program – Project Selection

These priorities consider Semi-additive Processing (SAP), Build Up (BU) and Laminate options. They all consider cost and reliability.

Top priority:
1. Material set (better dimensional stability, better adhesion, smoother profile)
2. Low cost litho/laser equipment for insitu shrinkage correction
3. New generation plating with better tolerances
4. Next generation of inspection and test of fine traces

Next priority:
1. Embedding active and passive infrastructure
Holistic Approach

Facilitator: Mario Bolanos, TI
Presenter: Bernd Appelt, ASE
Team Members

- Mario Bolanos – TI
- Bill Bader – iNEMI
- Bernd Appelt – ASE
- Akira Matsunami – Ti
- Isao Yamada – Intel
- Koichi Nonomura – Kyocera SLC
Brainstorming

- Pick a single package and utilize it as a pilot vehicle to create a holistic modeling approach and outline
  - Model would be a design tool that defines critical materials properties and proposed specifications for a specific package type.
  - Team would initially determine which package.
  - Data depth/accuracy in critical materials properties will be required for model effectiveness.
  - Will require data experts from materials, packaging, and substrate suppliers
  - Package selected needs to be one which is defined as a market need say 2-4 years out in the future.
  - Application details and specs need to be provided from the OEM(s) side. – coverage of multiple applications in desirable
Brainstorm

• Create a model and flow chart for new packages that covers entire supply chain from raw materials through system implementation.
• Create a 2010 plus analytical assessment of optimizing Time to Yield covering design, materials, packaging.
• Methodology to bring end customer requirements forward in meaningful way to the substrate and packaging suppliers.
• Reliability Methodology for substrates that supports comprehensive usage models and end product reliability requirements.
  – Pick a market segment and/or product line as a pilot vehicle
  – Good potential research cooperative project with universities
**Priority Projects**

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Priority Projects

• Create a 2010 plus analytical assessment of optimizing Time to Yield covering design, materials, packaging
  – Need to build in a methodology for low volume learning from substrate supplier, through packaging, then into system level yields
  • Covers data assessments including Cpk, FA. Etc
  – Financial contracts need to specify ramp quantities and time frame – Developing a commitment from both sides
  – Cooperative design team from substrate through system that leverages off existing BKM’s and proven specifications where possible
  – Define and use standards on areas such as surface finishes
  – May require brand new predictive tools that enable identification of key technology challenges, equipment or tool investments
Project Priorities

• Reliability Methodology for substrates that supports comprehensive usage models and end product reliability requirements.
  – Pick a market segment and/or product line as a pilot vehicle
    • Cover details of rel specs – life cycle, thermal cycles, shock test, etc.
  – Good potential research cooperative project with universities
  – OEM’s to provide detailed specifications/requirements – mechanical and electrical
  – Substrate suppliers to provide material properties early to support OEM simulations
  – May require that new metrology be developed to support the reliability model
  – New acceleration methods are highly desirable to shrink TTM
  – Define interfacial & chemical properties – define metrology requirements and methods
Proposed Initiatives

- Warpage
  - Qualification Criteria including Substrates, Pkg, board levels
  - Identify primary factors of warpage
- Miniaturization
  - Wiring Density Program
    - Material Set
    - Low Cost Litho/Laser
    - Plating
    - Inspection and Test
- Holistic Approach
  - Develop Holistic Modeling Approach (Using One Package)
  - Optimizing time to yield covering design, materials, packaging
  - Reliability Methodology for Substrates
Next Steps

• Identify Champions and interested Individuals and Firms for each proposal

• Post List of Proposals on Web Site

• Notify iNEMI (Jim Arnold) of which Initiatives you want to pursue: jim.arnold@inemi.org

• Jim Arnold from iNEMI Staff will work with each Champion to Establish Scheduled WebEx meetings to further develop each initiative.
Availability of Presentations

Presentations will be available for download at:

http://www.inemi.org/cms/newsroom/Presentations/Packaging_Substrates_Nov09.html
Packaging Substrate Workshop
Focusing on Technology for Miniaturization

Meeting Scope: Industry workshop to identify gaps in organic substrate technology that need to be addressed to facilitate miniaturization of electronics packaging.

The workshop will:
- Review organic substrate technology roadmaps and compare vs. industry requirements – Identify Gaps
- Establish action groups to address specific issues raised in meeting
- Brainstorm options and priorities
- Propose initiatives

We achieved our objectives!
www.inemi.org

Email contacts:
Bill Bader
Bill.Bader@inemi.org

Bob Pfahl
bob.pfahl@inemi.org

Haley Fu-Asia
haley.fu@inemi.org