Organic Substrate Roadmap Challenges
iNEMI Conference Nov 17-18, 2009

Prepared by Unimicron
Presented by Richard Sheridan
November, 2009
~ Introduction ~
WIN WITH

Unimicron

Carrier Business Unit
# Brief Introduction

<table>
<thead>
<tr>
<th>Category</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Established</td>
<td>1970</td>
</tr>
<tr>
<td>Incorporated</td>
<td>Jan. 25, 1990</td>
</tr>
<tr>
<td>Registered Capital</td>
<td>USD 325M</td>
</tr>
<tr>
<td>Chairman of Board</td>
<td>T. J. Tseng</td>
</tr>
<tr>
<td>IC Carrier President</td>
<td>Steve Chiang</td>
</tr>
<tr>
<td>Total Employees</td>
<td>5,414 (Taiwan); 9,313 (China)</td>
</tr>
</tbody>
</table>

**Business Units:**

- **Carrier**
- **PCB**
- **Testing / Burn In**
### Worldwide Top 10 Circuit Board Makers

<table>
<thead>
<tr>
<th>Rank</th>
<th>2007 Company</th>
<th>Revenue (US$M)</th>
<th>Rank</th>
<th>2008 Company</th>
<th>Revenue (US$M)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ibiden (J)</td>
<td>1,820</td>
<td>1</td>
<td>Nippon Mektron (J)*</td>
<td>1,790</td>
</tr>
<tr>
<td>2</td>
<td>Unimicron (T)</td>
<td>1,550</td>
<td>2</td>
<td>Ibiden (J)</td>
<td>1,750</td>
</tr>
<tr>
<td>3</td>
<td>Nippon Mektron (J)*</td>
<td>1,530</td>
<td>3</td>
<td>Unimicron (T)</td>
<td>1,550</td>
</tr>
<tr>
<td>4</td>
<td>Samsung E-M (K)</td>
<td>1,270</td>
<td>4</td>
<td>Samsung E-M (K)</td>
<td>1,235</td>
</tr>
<tr>
<td>5</td>
<td>Nanya PCB (T)</td>
<td>1,240</td>
<td>5</td>
<td>CMK (J)</td>
<td>1,205</td>
</tr>
<tr>
<td>6</td>
<td>CMK (J)</td>
<td>1,165</td>
<td>6</td>
<td>Nanya PCB (T)</td>
<td>1,190</td>
</tr>
<tr>
<td>7</td>
<td>King Board (HK)</td>
<td>900</td>
<td>7</td>
<td>Tripod (T)</td>
<td>965</td>
</tr>
<tr>
<td>8</td>
<td>Tripod (T)</td>
<td>830</td>
<td>8</td>
<td>King Board (HK)</td>
<td>950</td>
</tr>
<tr>
<td>9</td>
<td>Fujikura (J)</td>
<td>825</td>
<td>9</td>
<td>Fujikura (J)</td>
<td>850</td>
</tr>
<tr>
<td>10</td>
<td>Shinko (J)</td>
<td>795</td>
<td>10</td>
<td>Young Poong (K)</td>
<td>845</td>
</tr>
</tbody>
</table>

* Nippon Mektron’s sales included 20%+ assembly value.

**Unimicron Ranking**

- 2007: 3rd
- 2008:不变

**2008 Actual (US$M)**

\[
\text{Unimicron} + \frac{\text{PPt}}{412} = \text{Total}
\]

\[
1,550 + \frac{412}{1,962} = \frac{1,962}{1,962}
\]

**Source:** 2008 Prismark estimate (March 2009)
Unimicron Group Profile

Unimicron Suzhou
- FMC, BOC, CSP

Unimicron FC
- CSP, BOC, SIP, FMC, PoP, FCCSP

Unimicron CSP
- IC Burn-in, IC Testing

Unimicron Shanghai
- HDI, Fine-Line, Thin Board MLB

Unimicron Kunshan
- BVH, MLB, HDI

Unimicron Shenzhen
- HDI, Hi-End PCB

Unimicron Taoyuan
- HDI, BVH

Uniflex Kunshan
- Flex PCB

Unimicron Shanhong
- HDI, Hi-End PCB

Chung Yuan Plant
- IC Burn-in, IC Testing

Taiwan

China

World Class Quality
Carrier SBU Organization Chart

Carrier SBU President
Steve Chiang

President office
Marketing & NPI Sr. VP Eric Lao
TQM Committee Sr. Mgr Gordon Peng

Unimicron Suzhou
President David Cheng

Sales & Marketing Div.
VP Joseph Wu

Quality Management Div.
Sr. Manager Gordon Peng

Taiwan Region
COO Chia Pin Lee

Research and Design Div.
Sr. Manager Dr. TY Chen
Product Classification

Unimicron Products

Carrier 30%
Others 1%
PCB 69%

Carrier Product Type

CSP 44%
Flip Chip 34%
BOC 7%
FMC 8%
SIP Module 7%

Carrier Application

Wireless & Mobile 56%
PC & Networking 36%
Storage Media 8%
~ Roadmaps ~
# FCBGA Roadmap

<table>
<thead>
<tr>
<th>Feature</th>
<th>Time Frame</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Production</td>
<td>Sample</td>
<td></td>
</tr>
<tr>
<td>Min Core Thickness (mm)</td>
<td></td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
</tr>
<tr>
<td>Structure</td>
<td></td>
<td>4-2-4</td>
<td>6-2-6</td>
<td>7-X-7</td>
</tr>
<tr>
<td>Max Body Size (mm)</td>
<td></td>
<td>42.5x42.5</td>
<td>45x45</td>
<td>50x50</td>
</tr>
<tr>
<td>Core Layer</td>
<td>Min Core L/S</td>
<td>50/50</td>
<td>45/45</td>
<td>25/25</td>
</tr>
<tr>
<td></td>
<td>Min PTH/Pad for 800um core</td>
<td>150/300</td>
<td>150/300</td>
<td>150/300</td>
</tr>
<tr>
<td></td>
<td>Min PTH/Pad for 400um core</td>
<td>150/300</td>
<td>125/275</td>
<td>125/275</td>
</tr>
<tr>
<td>Build Up Layer</td>
<td>Min Build Up L/S (um)</td>
<td>18/18</td>
<td>14/14</td>
<td>10/10</td>
</tr>
<tr>
<td></td>
<td>Min Laser Via/Pad (um)</td>
<td>70/100</td>
<td>65/95</td>
<td>60/90</td>
</tr>
<tr>
<td></td>
<td>Max Stack Laser Via</td>
<td>3 stacked</td>
<td>3 stacked</td>
<td>3 stacked</td>
</tr>
<tr>
<td>Flip Chip Area</td>
<td>Min Bump Pitch (um)</td>
<td>170</td>
<td>150</td>
<td>135</td>
</tr>
<tr>
<td></td>
<td>Min Bump Pad Size (um)</td>
<td>120</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>Min Bump Pad Opening (um)</td>
<td>85</td>
<td>75</td>
<td>75</td>
</tr>
<tr>
<td>Ball Pitch (mm)</td>
<td></td>
<td>0.8</td>
<td>0.6</td>
<td>0.6</td>
</tr>
<tr>
<td>Process Innovation</td>
<td>SAP</td>
<td>PCF</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>New Product Technology</td>
<td>-</td>
<td>PCF Core</td>
<td>Embedded Pattern, Coreless</td>
<td>-</td>
</tr>
</tbody>
</table>
# CSP Roadmap

<table>
<thead>
<tr>
<th>Frame Feature</th>
<th>Time</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Production</td>
<td>Sample</td>
<td></td>
</tr>
<tr>
<td><strong>Material</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Laminate</td>
<td></td>
<td>BT-NXA, E679FGB AMC</td>
<td>ELC-4785GS, BT-NS, E679GT</td>
<td>Low CTE material (&lt;10 ppm)</td>
</tr>
<tr>
<td>Solder resist</td>
<td></td>
<td>AUS-303 / 308; AUS-320; AUS-410 (DF)</td>
<td>Thin DFSR, Thermal-cured SR</td>
<td></td>
</tr>
<tr>
<td><strong>Structure</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2L thickness, um</td>
<td></td>
<td>150</td>
<td>130</td>
<td>100</td>
</tr>
<tr>
<td>4L thickness, um</td>
<td></td>
<td>210</td>
<td>180</td>
<td>160</td>
</tr>
<tr>
<td><strong>Capability</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L/S - um</td>
<td></td>
<td>25/25 (Semi-additive)</td>
<td>20/20 (Semi-additive) 35/35 (Subtractive)</td>
<td>15/15</td>
</tr>
<tr>
<td>Finger pitch - um</td>
<td></td>
<td>85</td>
<td>80</td>
<td>70</td>
</tr>
<tr>
<td><strong>Interconnect</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Through via / pad, um</td>
<td></td>
<td>100 / 190</td>
<td>75 / 170</td>
<td>75 / 150</td>
</tr>
<tr>
<td>Micro via / pad, um</td>
<td></td>
<td>65 / 130</td>
<td>65 / 110</td>
<td>60 / 100</td>
</tr>
<tr>
<td>FC bump pitch, um</td>
<td></td>
<td>150 (array)</td>
<td>150 (array)</td>
<td>135 (array),</td>
</tr>
<tr>
<td><strong>Surface Finish – Wire bond</strong></td>
<td></td>
<td>NiAu, AFOP, EPP</td>
<td>ENEPIG</td>
<td>ENEPIG</td>
</tr>
<tr>
<td><strong>Surface Finish – Flip chip</strong></td>
<td></td>
<td>OSP, SOP + Ni/Au SOP+OSP, SOP+IT</td>
<td>ENEPIG, Sn plating</td>
<td>ENEPIG, Sn plating</td>
</tr>
<tr>
<td>Solder resist registration, um</td>
<td></td>
<td>20</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>Ball Pitch (mm)</td>
<td></td>
<td>0.4</td>
<td>0.4</td>
<td>0.3</td>
</tr>
<tr>
<td>New Product Technology</td>
<td></td>
<td>Coreless for POP_TMV, Cavity POP (w/ EDC option), Fan out WLP, TSV 3D, Embedded: Active, Passive, Circuits</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
~ Challenges ~
Alignment

- Via in FC Bump Pads
  - Requirement: 65/135 → 65/110 → 60/100
  - Alignment methodology
  - Lower CTE materials
    - A must for thin CSP structures
  - Coreless
  - DLD
  - Exposure technology
    - Multiple division exposure
    - Auto scaling

CpK's for 60/100:
  - FCBGA: >3
  - FCCSP: 1-1.4
Alignment

- Solder Resist Alignment
  - Requirement: 20um → 15um → 10um
    - Dry Film Solder resist
      - Thickness uniformity
      - Finer filler size
    - Lower CTE materials
    - Multiple division exposure
    - Multiple division exposure + auto scaling
  - Laser ablated SR?
Test Machine

<table>
<thead>
<tr>
<th>Exposure method</th>
<th>Machine</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A</td>
</tr>
<tr>
<td>DI</td>
<td>DI</td>
</tr>
</tbody>
</table>

S/M material

For New Machine: AUS 308, AUS 320, AUS 410
For Property: SR-1, Thermal
Measurement Plan

- Sample size

SRR = pad center to opening center

1. For SRR: 20 points/panel, total: 1 panel
2. For Opening shape: 5 points/panel, total: 1 panel
Result

Note: CpK is calculated for positional tolerance of SR opening only and does not incorporate conductor pad size tolerance or SR opening tolerance.
S/M Thickness control

AUS 320

Spec: 16 +/- 6  Cpk: 1.53

AUS 410

Spec: 15 +/- 5  Cpk: 1.81

DFSR is better than LPSR in thickness control

Sample size: 9 point/PNL, total 5 panel
Laser Ablated SRO

SRO_{\text{Top}} : 92.34 \text{ um}
SRO_{\text{Bottom}} : 81.17 \text{ um}
Foot : 5.59 \text{ um}

There is big foot and rough side-wall
Warpage

- Dimensional stability → Low CTE materials
- Complex mix of factors → Modeling and DOE study
- Metrology → What is ‘good’? Strip vs Unit
- PoP vs non-PoP vs overmolded PoP
- Design Symmetry

Result:
- Core thickness: 80 μm
- At reflow time 220sec and temp 220 °C
- The package max. temperature = 198.88 °C
- Max deformation (Z Axis) = 0.17935 mm

 Dummy Cu added
Conductor Pitch

- Requirement: 50 → 40 → 30um
  - Process change: MESA (mSAP) → PSAP (SAP)
  - Resist Adhesion
  - Enhanced/expanded cleanrooms
  - ‘Contact-free’ processes
  - Cu plating technologies

High CapEx Required
HF and Low CTE materials

- Filler sizes and types
  - Hydrophilic vs Hydrophobic
  - Organic vs inorganic
- Drill compatibility
- Plating activation
- Material management
  - Hitachi, MGC, Sumitomo, Doosan, others?
- Cost
Fine Pitch Pre-soldering (SOP) <150um

<table>
<thead>
<tr>
<th>Metal Stencil Printing</th>
<th>DF Stencil Printing</th>
<th>Micro-ball Placement</th>
<th>SPOP</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Diagram" /></td>
<td><img src="image2.png" alt="Diagram" /></td>
<td><img src="image3.png" alt="Diagram" /></td>
<td><img src="image4.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>

Pitch:  
- Metal Stencil Printing: >140um
- DF Stencil Printing: 100-140um
- Micro-ball Placement: >125um

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# Fine Pitch Pre-soldering (SOP) <150um

<table>
<thead>
<tr>
<th></th>
<th>Metal Stencil</th>
<th>DFStencil</th>
<th>uBall</th>
<th>SPOP</th>
</tr>
</thead>
</table>
| **Pros** | • Lowest Cost  
• Mature infrastructure  
• Ternary metallurgy available | • Low Cost  
• Scalable  
• Low cap ex  
• Ternary metallurgy available | • Demonstrated capability on FCBGA  
• Ternary metallurgy available | • Low cost  
• Scalable  
• Planarity  
• Die standoff  
• Uses existing infrastructure  
• Void free |
| **Cons** | • Limited to >140um pitch  
• Process not mature  
• Material selection | • Process not mature  
• Material selection | • Alignment on FCCSP  
• Cost  
• High cap ex | • Rel performance for Cu pillar bumped die unknown (ELK)  
• Ternary metallurgy not available  
• Not available w/OSP |

- Solder voiding
- Varied specs
- Metrology
SPOP® Technology

SPOP-CT²™ : (Solder Plated on Pad - Cu + Thick Tin)

SPOP® Applications

- FCBGA
- FCCSP
- Hybrid(FC+WB)

Top view

Structure

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SPOP® Technology Advantage

Enhance FC interconnection reliability and increase yield for fine bump pitch:

SPOP® offers 1). Void free solution for L.F assembly

2). High Yield for LF or Eutectic Wafer Bump

- Higher stand off -- Easy for underfill filling
- Good solder volume control – Less bridge issue

Wafer Bump: LF & Eutectic

SPOP or Micro ball

Bridge caused by rich solder

Best solution – SPOP®

SPOP

- No bridge issue
- Higher gap for easier underfill filling
Customization

- Bump technologies
  - Au stud
  - Solder
  - Cu pillar

- Final finish
  - ImSn
  - E’lytic Ni/Au
  - SOP over Ni/Au, OSP, Sn
  - OSP
  - ENEPIG
  - Others

- Material selection
- Layer and dielectric stack-ups
Electrical Test

- Fixture Costs
  - Finer pitches are driving up costs
  - Custom strip designs are forcing redundancy in ET fixture expenditures by OEM/IDM’s
- When is 100% test required?
Electrical Performance

- Lower Inductance
- Decoupling
  - Frequencies of AP’s on the rise
  - No room for SMT solution…especially PoP
  - Embedded passives?
- Signal loss
  - Conductor roughness
- Electrical simulation capabilities
  - Tools
  - Experience
  - Customer alignment
Unimicron’s Embedded Technologies

Year 2004
CFP Capacitors
~ 16.8 pF/mm²
Stopped, PWB

Year 2006
Ceramic Capacitors
~ 1.5 nF/mm²
Stopped, IC substrates

Year 2008
Embedded Discrete Components
Pilot / Qualification, IC substrates
- 0402, 0603, 1005 passives
- IC components

Year 2009  ➔  Adopt PPT’s Emb. Tech. after merger

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Embedded Substrate Technology Approaches

- **3C-SiP™** (Chip-Copper-Connection)
- **EC-FCBGA™** (Embedded-Capacitor)
- **3C-CSP™** (Chip-Copper-Connection)
- **EC-FCCSP™** (Embedded-Capacitor)

### Customer Structure Application PKG Size (mm²) SBT Thk. (um) Qualification Status

<table>
<thead>
<tr>
<th>Customer</th>
<th>Structure</th>
<th>Application</th>
<th>PKG Size (mm²)</th>
<th>SBT Thk. (um)</th>
<th>Qualification Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>3C-SiP</td>
<td>Handheld</td>
<td>5 x 5</td>
<td>370</td>
<td>Passed</td>
</tr>
<tr>
<td>B</td>
<td>3C-SiP</td>
<td>Cell Phone</td>
<td>12 x 12</td>
<td>400</td>
<td>Passed</td>
</tr>
<tr>
<td></td>
<td>EC-FCBGA</td>
<td>GPU</td>
<td>35 x 35</td>
<td>960</td>
<td>Passed</td>
</tr>
<tr>
<td>C</td>
<td>3C-CSP</td>
<td>Memory Module</td>
<td>13.5 x 8</td>
<td>750</td>
<td>Passed</td>
</tr>
<tr>
<td>D</td>
<td>EC-FCBGA</td>
<td>GPU</td>
<td>35 x 35</td>
<td>960</td>
<td>Passed</td>
</tr>
<tr>
<td>E</td>
<td>EC-FCBGA</td>
<td>FPGA</td>
<td>35 x 35</td>
<td>1050</td>
<td>Passed</td>
</tr>
<tr>
<td>F</td>
<td>EC-FCCSP</td>
<td>Cell Phone</td>
<td>15 x 15</td>
<td>280</td>
<td>On-going</td>
</tr>
</tbody>
</table>

※ **3C-SiP™** is working on scale up test with 1 customer.
※ **4 customers co-work to qualify 3C-SiP™.**
※ **2 customers are qualifying EC-FCCSP right now.**
Cross Section Illustration

[Image of cross section illustration with labeled layers: SM, PP&GF, MLCC, and dimensions 1, 2, 3, 4, 5.]
Electrical Performance

✓ Fly-probe method to measure the capacitor value.
✓ Average capacitor value is 92.6nF with +/- 20% variation.
Reliability Performance

Reliability tests

<table>
<thead>
<tr>
<th>Substrate Level Reliability</th>
<th>Solder Dip 288°C</th>
<th>Reflow 260°C</th>
<th>Precon. L3 +PCT (121°C/100%RH)</th>
<th>Precon. L3 +TCT (-55~125°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>5x</td>
<td>35x</td>
<td>96hr</td>
<td>168hr</td>
</tr>
<tr>
<td>Lot 1</td>
<td>0/54</td>
<td>0/54</td>
<td>0/54</td>
<td>0/54</td>
</tr>
<tr>
<td>Lot 2</td>
<td>0/54</td>
<td>0/54</td>
<td>0/54</td>
<td>0/54</td>
</tr>
</tbody>
</table>

*SAM Inspection*

- Passed reliability requirements and ready for sample qualification.

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Fine L/S (20/20, 15/15)

- Trace roughness for mSAP vs. SAP

<table>
<thead>
<tr>
<th>Laminate roughness (After Cu etching)</th>
<th>mSAP</th>
<th>PSAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEM</td>
<td><img src="image" alt="mSAP SEM" /></td>
<td><img src="image" alt="PSAP SEM" /></td>
</tr>
<tr>
<td>X-section</td>
<td><img src="image" alt="mSAP X-section" /></td>
<td><img src="image" alt="PSAP X-section" /></td>
</tr>
</tbody>
</table>

The interface between Cu trace & laminate in MSAP method is rougher than PSAP.
Fine L/S (20/20, 15/15)

- Trace roughness for mSAP vs. SAP

**Trace roughness**
(After CZ etching)

**mSAP**

Ra: 0.48 um, Rz: 4.51 um

**PSAP**

Ra: 0.56 um, Rz: 4.77 um

Wyco

The surface roughness is more rougher in PSAP process.
X-out Economics

- Unit yield vs Shipping yield
- Substrate costs vs Assembly material/throughput costs
- Adding layers and finishes

Shipping Yield as a function of Unit Yield

20% X-out Threshold

Shipping Yield (%) vs Unit Yield (%)
Substrate Roadmap Challenges: Summary

- **Alignment**
  - Drill AR <25um
  - SR registration <15um

- **Coreless**
  - CF processing
  - Dimensionally stable carrier

- **SR thickness and tolerance**
  - Nominal <20um
  - Tolerance <6um

- **Warpage / Planarity**
  - Improved predictive models
  - Establish metrology for substrate

- **HF and low CTE materials**

- **Finer conductor lines**
  - FCBGA line pitch: 28 → 24 → 20
  - FCCSP line pitch: 50 → 40 → 30

- **Fine pitch pre-soldering**
  - Print vs uBall vs Plated

- **Customization**
  - Varied materials and stack-ups

- **Electrical test: High fixture costs**

- **Electrical performance**
  - Inductance
  - Decoupling
  - Signal Loss

- **X-out economics**
Possible Consortia Activities

- Warpage
  - Build effective models
  - Define metrology and specs
- Decoupling for PoP
  - Work collaboratively on embedded solution
- Conductor roughness
  - Evaluate roughness needed for FCCSP devices
  - Establish specs and metrology
- Solder voiding specs
- SOP, bump metallurgy, die standoff, and ELK dielectric combinations
Coreless Platform

- Coreless substrate
  - A substrate with all build-up layers
  - Microvia for interconnection
  - Flexible layer counts
Coreless Benefits

- Reduce Substrate Thickness
- Higher Via Density
- High Structure Flexibility with Simplified Design Rules
- Compatible with Cu Pillar Process for FC Joining

Carrier core for easy processing

2 Coreless substrates made at one time
4L Coreless FC POP Sample

Structure

- Cu pillar for FC connection, NSMD design
- Stacked up POP pad for top POP package, SMD design
- PSAP fine line @ 20/20um
- 4L coreless + Cu pillar + stacked POP, total thk. : 0.28 +/- 0.04 mm

Top View

PoP Pad : SMD
275um SRO/325um Pad

C4 : NSMD

Green : SR Covered
Red : Cu Pad

Open solder mask design in I/O area.
4L Coreless FC POP Sample

- 4L w/ Cu pillar
- 20um L/S
- 4L PSAP processing compatible with std. FCBGA production line

World Class Quality

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