PBGA and strip format CSP

Steve Yang
WB R&D Director
Nan Ya PCB Corp
November 17th, 2009
Outline

1. Introduction
   - Packaging Trend
   - Substrate approach to meet packaging trend
   - The growth of packaging substrate
   - The changes and forecast of packaging substrate
   - Mobile Phone Handset Sales

2. Packaging Substrate Technology
   - PBGA roadmap and design rule
   - CSP roadmap and design rule
   - FCCSP roadmap and design rule
   - Key substrate technology to approach packaging trend

3. Packaging substrate reliability test

4. Summary
Introduction
Packaging Trend

- Standard Lead-frame Package
- Performance Limited by Package
- Horizontal Structure
- Stack Structure
- Embedded Structure

**IC Minimization Trend**
- 0.7um
- 0.3um
- 0.13um
- 90nm
- 65nm
- 45nm
- 32nm
- 28nm
- 22nm

**Die Size**
- 110mm²
- 96mm²
- 81mm²
- 64mm²
- 50mm²
- 40mm²

**Package Option**
- BGA
- CSP
- MCM (FC)
- MCM (WB)
- WB Die Stack
- PoP

Nanya PCB Corporation
Substrate approach to meet packaging trend

IC Minimization Trend

<table>
<thead>
<tr>
<th>Year</th>
<th>1985</th>
<th>1995</th>
<th>2005</th>
<th>2015</th>
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<tr>
<td>IC Technology</td>
<td>0.7um</td>
<td>0.3um</td>
<td>0.13um</td>
<td>90nm</td>
</tr>
<tr>
<td>Die Size</td>
<td>110mm²</td>
<td>96mm²</td>
<td>81mm²</td>
<td>64mm²</td>
</tr>
</tbody>
</table>

1st Evolution

Lead Frame

WB Substrate

FC-BGA Substrate

2nd Evolution

FC-CSP Substrate

3rd Evolution

Embedded Chip

Embedded Passive

FC-POP
The Growth of Packaging Substrate

<table>
<thead>
<tr>
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<tr>
<td>PCB Market ($M)</td>
<td>33,100</td>
<td>36,368</td>
<td>40,920</td>
<td>32,694</td>
<td>30,841</td>
<td>33,311</td>
<td>38,421</td>
<td>40,638</td>
<td>45,144</td>
<td>47,684</td>
<td>48,228</td>
<td>40,314</td>
<td>42,128</td>
<td>46,593</td>
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<td>57,679</td>
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<tr>
<td>Packaging Substrates ($M)</td>
<td>1,442</td>
<td>2,143</td>
<td>3,505</td>
<td>2,603</td>
<td>2,638</td>
<td>3,025</td>
<td>3,565</td>
<td>4,977</td>
<td>6,467</td>
<td>7,058</td>
<td>6,959</td>
<td>5,803</td>
<td>6,085</td>
<td>6,825</td>
<td>7,885</td>
<td>8,592</td>
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<tr>
<td>Packaging Substrates Ratio</td>
<td>4.4%</td>
<td>5.9%</td>
<td>8.6%</td>
<td>8.0%</td>
<td>8.6%</td>
<td>9.1%</td>
<td>9.3%</td>
<td>12.2%</td>
<td>14.3%</td>
<td>14.8%</td>
<td>14.4%</td>
<td>14.4%</td>
<td>14.4%</td>
<td>14.6%</td>
<td>14.8%</td>
<td>14.9%</td>
</tr>
</tbody>
</table>

Source: Prismark, Aug, 2009
The Changes and Forecast of Packaging Substrate

### 2000
- **Commodity Boards**: 23.6%
- **Multilayer Boards**: 54.3%
- **Flexible Circuits**: 8.4%
- **Microvia Boards**: 5.1%
- **Packaging Substrates**: 8.6%

**Total**: $40,920M

### 2008
- **Commodity Boards**: 15.5%
- **Multilayer Boards**: 41.5%
- **Flexible Circuits**: 15.3%
- **Microvia Boards**: 13.3%
- **Packaging Substrates**: 14.4%

**Total**: $48,230M

### 2013
- **Commodity Boards**: 13.7%
- **Multilayer Boards**: 41.6%
- **Flexible Circuits**: 15.7%
- **Microvia Boards**: 14.1%
- **Packaging Substrates**: 14.9%

**Total**: $57,679M

### Value ($M)

<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Commodity Boards</td>
<td>$9,674</td>
<td>$7,492</td>
<td>-22.6%</td>
<td>$7,902</td>
<td>1.1%</td>
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<tr>
<td>Multilayer Boards</td>
<td>$22,217</td>
<td>$19,934</td>
<td>-10.0%</td>
<td>$24,004</td>
<td>3.7%</td>
</tr>
<tr>
<td>Microvia Boards</td>
<td>$2,074</td>
<td>$6,425</td>
<td>209.8%</td>
<td>$8,105</td>
<td>4.8%</td>
</tr>
<tr>
<td>Packaging Substrates</td>
<td>$3,505</td>
<td>$6,359</td>
<td>88.5%</td>
<td>$8,592</td>
<td>4.3%</td>
</tr>
<tr>
<td>Flexible Circuits</td>
<td>$3,450</td>
<td>$7,359</td>
<td>113.3%</td>
<td>$9,075</td>
<td>4.3%</td>
</tr>
<tr>
<td>Total</td>
<td>$40,920</td>
<td>$48,230</td>
<td>17.9%</td>
<td>$57,679</td>
<td>3.6%</td>
</tr>
</tbody>
</table>

Source: Prismark, Aug, 2009
Mobile Phone Handset Sales

- Subscriber Growth Leveling Off
- CAAGR '90-00: 46%
- CAAGR '00-07: 23%
- 47% World Penetration End-2007
- Expect CAAGR '07-12: 7%
- Expect 82% World Penetration End-2012
- ~100M New Subscribers Annually After 2012

- Mobile Phone Sales Leveling Off
- CAAGR '90-00: 56%
- CAAGR '00-07: 16%
- 1.14Bn Phones Sold in 2007
- Increasing cyclicity with GDP growth
- Expect CAAGR '07-12: 5%

- Source: Prismark

- Global recession results in below-trend phone growth
- Source: Prismark, Aug, 2009
"Smaller" & "Thinner" package size which needs the alignment of package and substrate technology.
Packaging Substrate Technology
(PBGA/CSP/FCCSP)
### PBGA Substrate Roadmap

<table>
<thead>
<tr>
<th>Substrate Tech.</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
</tr>
</thead>
<tbody>
<tr>
<td>Structure</td>
<td>2L/4L/6L</td>
<td>1-2-1/1-4-1</td>
<td>2-2-2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Min. BF pitch</td>
<td>125um</td>
<td>110 um</td>
<td>100um</td>
<td>90 um</td>
<td>80 um</td>
</tr>
<tr>
<td>Min. line pitch</td>
<td>100um</td>
<td>80 um</td>
<td>70um</td>
<td>60 um</td>
<td></td>
</tr>
<tr>
<td>Via Diameter</td>
<td>200um</td>
<td>150 um</td>
<td>100um</td>
<td>75 um</td>
<td></td>
</tr>
<tr>
<td>Via Land</td>
<td>350um</td>
<td>300 um</td>
<td>230um</td>
<td>200 um</td>
<td></td>
</tr>
<tr>
<td>Wafer Tech.</td>
<td>180/130 nm</td>
<td>90 nm</td>
<td>65 nm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## PBGA Substrate Design Rule

<table>
<thead>
<tr>
<th></th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire bond pitch/</td>
<td>125/60</td>
<td>110/55</td>
<td>100/50</td>
<td>90/45</td>
<td>80/40</td>
</tr>
<tr>
<td>Min. top width (um)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Line pitch/</td>
<td>100/35</td>
<td>80/30</td>
<td>70/25</td>
<td>70/25</td>
<td>60/20</td>
</tr>
<tr>
<td>Min. width (um)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Laser Via size/</td>
<td>100/250</td>
<td>100/230</td>
<td>80/200</td>
<td>75/180</td>
<td>75/180</td>
</tr>
<tr>
<td>Laser via land size (um)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mechanical via size/</td>
<td>200/350</td>
<td>150/300</td>
<td>100/230</td>
<td>100/200</td>
<td>100/200</td>
</tr>
<tr>
<td>Mechanical via land size (um)</td>
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</table>
# CSP Substrate Roadmap

<table>
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<th>Substrate Tech.</th>
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<th>2010</th>
<th>2011</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Structure</strong></td>
<td>2L/4L/1-2-1</td>
<td>1-4-1/2-2-2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Min. BF pitch</strong></td>
<td>105 um</td>
<td>90 um</td>
<td>80 um</td>
<td>70 um</td>
<td>60 um</td>
</tr>
<tr>
<td><strong>Min. line pitch</strong></td>
<td>70um</td>
<td>60um</td>
<td>50 um</td>
<td>40 um</td>
<td>34 um</td>
</tr>
<tr>
<td><strong>Via Diameter</strong></td>
<td>80um</td>
<td>75 um</td>
<td>70um</td>
<td>65 um</td>
<td></td>
</tr>
<tr>
<td><strong>Via Land</strong></td>
<td>200um</td>
<td>180 um</td>
<td>150um</td>
<td>130 um</td>
<td></td>
</tr>
<tr>
<td><strong>Min. Ball pad pitch</strong></td>
<td>500um</td>
<td>400um</td>
<td>350um</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Wafer Tech.</strong></td>
<td>90 nm</td>
<td>65 nm</td>
<td>45 nm</td>
<td>32 nm</td>
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</tr>
</tbody>
</table>
## CSP Substrate Design Rule

<table>
<thead>
<tr>
<th></th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire bond pitch/ Min. top width (um)</td>
<td>105/55</td>
<td>90/45</td>
<td>80/40</td>
<td>70/35</td>
<td>70/35</td>
</tr>
<tr>
<td>Line pitch/ Min. width (um)</td>
<td>70/25</td>
<td>60/20</td>
<td>50/15</td>
<td>40/14</td>
<td>34/12</td>
</tr>
<tr>
<td>Laser Via size/ Laser via land size (um)</td>
<td>80/200</td>
<td>75/180</td>
<td>70/150</td>
<td>65/130</td>
<td>60/120</td>
</tr>
<tr>
<td>Mechanical via size/ Mechanical via land size (um)</td>
<td>100/230</td>
<td>100/200</td>
<td>75/175</td>
<td>75/150</td>
<td>60/135</td>
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<tr>
<td>Ball pitch/SRO (um)</td>
<td>500/275</td>
<td>400/250</td>
<td>400/230</td>
<td>350/220</td>
<td>300/200</td>
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</table>
FCCSP Substrate Roadmap

**Substrate Tech.**

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<tbody>
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<td><strong>C4 Bump Pitch</strong></td>
<td>180 um</td>
<td>150 um</td>
<td>130/120 um</td>
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<tr>
<td><strong>SR Opening</strong></td>
<td>90 um</td>
<td>85 um</td>
<td>80 um</td>
<td>75 um</td>
<td>70 um</td>
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<tr>
<td><strong>C4 Pad Size</strong></td>
<td>140 um</td>
<td>135 um</td>
<td>120 um</td>
<td>105 um</td>
<td>95 um</td>
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<tr>
<td><strong>SM Type</strong></td>
<td>Liquid Type</td>
<td>Dry Film Type</td>
<td></td>
<td></td>
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<tr>
<td><strong>Process</strong></td>
<td>MSAP</td>
<td>SAP</td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

**Wafer Tech.**

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<th>2011</th>
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<tbody>
<tr>
<td>90 nm</td>
<td>65 nm</td>
<td>45 nm</td>
<td>32/28 nm</td>
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## FCCSP Substrate Design Rule

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<th>2011</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line pitch/ Min. width (um)</td>
<td>70/25</td>
<td>60/20</td>
<td>50/15</td>
<td>40/14</td>
<td>30/12</td>
</tr>
<tr>
<td>C4 Pitch/ SRO (um)</td>
<td>180/90</td>
<td>150/85</td>
<td>150/80</td>
<td>130/75</td>
<td>120/70</td>
</tr>
<tr>
<td>C4 Pad registration (um)</td>
<td>+/-25</td>
<td>+/-25</td>
<td>+/-20</td>
<td>+/-15</td>
<td>+/-12.5</td>
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<tr>
<td>Laser Via size/ Laser via land size (um)</td>
<td>80/200</td>
<td>75/180</td>
<td>70/150</td>
<td>65/130</td>
<td>60/110</td>
</tr>
<tr>
<td>Mechanical via size/ Mechanical via land size (um)</td>
<td>100/230</td>
<td>100/200</td>
<td>75/175</td>
<td>75/150</td>
<td>60/135</td>
</tr>
</tbody>
</table>
Key Substrate Technology to Approach Packaging Trend

Packaging Trend

- High speed/ performance
  - Wire bond connection
- High density/ small form factor
  - Fine L/S
  - Higher density structure
- Thinner package
  - Thin substrate
  - Flat substrate surface

Key Substrate Technology

- Flip chip connection
- Compatible surface finish
Key Substrate Technology to Approach Packaging Trend

Packaging Trend

Key Substrate Technology

High speed/ performance
- Wire bond connection
- Flip chip connection

High density/ small form factor
- Finer line
- Higher density structure
- Compatible surface finish

Thinner package
- Thin substrate
- Flat substrate surface
FCCSP driver

**Performance**
- High electrical performance
- High frequency

**Density**
- High I/O
- Fine bump pitch
- Via on pad design

**Cost**
- Non-Au wire package
- Lower Au thk./area of surface finish (IT/OSP/ENEPIG)

- Per high performance, density, cost, WB → FC package is the trend.
Key Substrate Technology to Approach Packaging Trend

Packaging Trend

- High speed/ performance
- Wire bond connection
- Flip chip connection

Key Substrate Technology

- High density/ small form factor
  - Fine L/S
  - Higher density structure
  - Compatible surface finish

- Thinner package
  - Thin substrate
  - Flat substrate surface
### Key technology / Fine L/S - SAP with PCF

**Modified Semi-additive (MSAP)**
- Electro Cu
- E’less Cu
- Low profile Cu foil (UTC)

**Semi-additive (SAP)**
- Electro Cu
- E’less Cu
- Primer

<table>
<thead>
<tr>
<th>Process</th>
<th>MSAP</th>
<th>SAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Material</td>
<td>Core with UTC</td>
<td>Core with PCF</td>
</tr>
<tr>
<td>Base Cu</td>
<td>UTC (2~5um)</td>
<td>E’less Cu (0.5~1.0 um)</td>
</tr>
<tr>
<td>Roughness</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Exposure</td>
<td>Plastic film</td>
<td>Glass mask</td>
</tr>
<tr>
<td>Etching</td>
<td>Quick etch</td>
<td>Quick Etch</td>
</tr>
<tr>
<td>L/S capability</td>
<td>25/25</td>
<td>20/20 ↓</td>
</tr>
</tbody>
</table>

- **L/S Pitch**
  - 50 um
  - 40 um
  - 30 um

- **BF Pitch**
  - 80 um
  - 60 um
  - 45 um

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Nanya PCB Corporation

iNEMI Packaging Substrates Workshop, Nov, 2009
Key technology / Fine L/S - SAP with PCF

Non-desmear type PCF

- Material issue (Core or Dielectric with primer)
- Desmear/PTH(E'less Cu)
- D/F Lam./Glass mask exposure/Develop/Electro Cu plating
- Mechanical drill

Desmear type PCF

- Material issue (Core or Dielectric with primer)
- Desmear/PTH(E'less Cu)
- D/F Lam./Glass mask exposure/Develop/Electro Cu plating
- Mechanical drill

Non-desmear type PCF will be ruined by desmear.

Non-desmear type PCF will lead to some reliability issues if we use desmear process.

Non-desmear type PCF

Q3  Q4

Q1  Q2

2008  2009

Nanya PCB Corporation
Key Technology / Higher density structure - VOP and Via on PTH Technology

- **Strength**
  - High density interconnection
  - BGA Ball pad pitch reduction

- **Key Technologies**
  - Cu filling technology in “Via” and “PTH”

**VOP (Via-on-Pad)**

**Via on PTH**

- 1+2+1
**Key technology / Compatible surface finish-ENEPiG**

- **What is “ENEPiG”?**
  - Electroless Nickel Electroless Palladium Immersion Gold.
  - Good SJR by Lead Free Condition → Using Pd as a barrier so that the Ni oxidation can be prevented and we can get good solder joint results.

- **Why is “ENEPiG” a surface finish option for WB Substrates??**
  - To increase Density for Circuit Design
  - To decrease the Substrate Size
  - To decrease Plating Stub (Bus Bar) to help High Frequency Products Development
  - Wire-Bond is Workable

Assembly Area smaller than 1/2 if using Busless Design!!
### Comparison for Busless Design Substrate between E’lytic Ni/Au Plating & ENEPIG

<table>
<thead>
<tr>
<th>Compared List</th>
<th>Busless Design w/ Electrolytic Ni/Au Plating</th>
<th>Busless Design w/ ENEPIG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plating Method</td>
<td>Electrolytic Plating</td>
<td>Electroless Plating</td>
</tr>
<tr>
<td>High Density Circuitry w/ Busless Design</td>
<td>All substrate makers need extra processes for busless design</td>
<td>One step plating, no need extra processes</td>
</tr>
<tr>
<td>Process Controllability</td>
<td>OK</td>
<td>OK</td>
</tr>
</tbody>
</table>
| Plating Thickness | Ni: 5~15um  
Au: 0.5~1.0um | Ni: 5~10um  
Pd: 0.03~0.08um  
Au: 0.10~0.15um |
| Process Cycle Time | High (Multi-Steps) | Low (One Step) |
| Wire Bondability | OK                                          | OK                        |
| Cold Ball Pull Reliability | IR (260°C) 1X – 564g~707g  
IR (260°C) 3X – 519g~676g | IR (260°C) 1X – 634g~721g  
IR (260°C) 3X – 643g~769g |
| Ball Shear Reliability | IR (260°C) 1X – 687g~856g  
IR (260°C) 3X – 762g~903g | IR (260°C) 1X – 528g~672g  
IR (260°C) 3X – 572g~672g |
| Total Cost | High | Low |

- Lower cost and short cycle time is the driving force to use ENEPIG on busless design.
Wire Bondability Comparison between E’lytic Ni/Au & ENEPIG

- **Input Parameters**
  - **Ni/Pd/Au Thickness:**
    1. Ni: 5 ~ 10 µm
    2. Pd: 0.06 ~ 0.14 µm
    3. Au: 0.10 ~ 0.15 µm
  - **Pull Strength**
    1. Sampling Size: 20 Wires
    2. Au Wire Width: 25 µm
    3. Pull Strength Criterion: 3.5 g min.
  - **Thermal Aging Test:**
    1. Prebake Time: 24 hr (@ 125°C)
    2. Thermal Aging Time: 96 hrs (@ 175°C)

- **Break Mode Analysis**

- **W/B Pull Strength Data Analysis**
  - **Before Thermal Aging Test**
  - **After Thermal Aging Test**

  ![](chart)

  *Mode B, C & D are acceptable*

<table>
<thead>
<tr>
<th>SF Type</th>
<th>Break Mode</th>
<th>Judgement</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENEPIG</td>
<td>7%  6%  87%</td>
<td>Pass</td>
</tr>
<tr>
<td>E’lytic Ni/Au</td>
<td>28% 69%  3%</td>
<td>Pass</td>
</tr>
</tbody>
</table>

Base on the break mode and W/B pull strength data, ENEPIG is suitable for wire bonding !!!
Application of ENEPIG- Hybrid CSP (FC+WB) – Compatible Surface Finish for FC & WB

<table>
<thead>
<tr>
<th>Hybrid CSP with SOP</th>
<th>Surface Finish Option 1</th>
<th>Surface Finish Option 2</th>
<th>Surface Finish Option 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>C4 Pad</strong></td>
<td>OSP</td>
<td>OSP</td>
<td>ENEPIG</td>
</tr>
<tr>
<td><strong>Bond Finger</strong></td>
<td>Soft Ni/Au</td>
<td>Soft Ni/Au</td>
<td>ENEPIG</td>
</tr>
<tr>
<td><strong>Ball Pad</strong></td>
<td>Soft Ni/Au</td>
<td>OSP</td>
<td>ENEPIG</td>
</tr>
<tr>
<td><strong>Process Cycle Time</strong></td>
<td>Worse (Multi-Steps)</td>
<td>Worse (Multi-Steps)</td>
<td>Best (One Step)</td>
</tr>
<tr>
<td><strong>Quality</strong></td>
<td>Good</td>
<td>Worse (discolor issue on bottom OSP pad)</td>
<td>Best</td>
</tr>
<tr>
<td><strong>Reliability</strong></td>
<td>Good</td>
<td>Good</td>
<td>Best</td>
</tr>
</tbody>
</table>

**ENEPIG is preferred for Hybrid CSP base on Cycle Time, Quality and Reliability !!!**
Key Substrate Technology to Approach Packaging Trend

Packaging Trend
- High speed/performance
  - Wire bond connection
- High density/small form factor
  - Finer line
  - Higher density structure
  - Compatible surface finish

Key Substrate Technology

Thinner package
- Thin substrate
- Flat substrate surface
Key technology / Thin substrate - Thinner core

Standard structure

Thin structure with thinner core

<table>
<thead>
<tr>
<th>Component</th>
<th>Standard</th>
<th>Thin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core</td>
<td>60um</td>
<td>40um</td>
</tr>
<tr>
<td>Cu thickness</td>
<td>15um</td>
<td>15um</td>
</tr>
<tr>
<td>S/R</td>
<td>20um</td>
<td>15um</td>
</tr>
<tr>
<td>Board thickness</td>
<td>130um</td>
<td>100um</td>
</tr>
</tbody>
</table>

Substrate thickness from 130um to 100um!!!
Key technology / Flat substrate Surface - DF type SR

Minimize Z-height package

IC Technology (Wafer Thinning)

- 3 mils
- 2 mils
- 1.5 mils

Package Technology (Die Stack)

- >2/3 stacks
- 4 stacks
- 5 stacks

Challenge of thin die package

Uneven surface by liquid SR

Die crack

Solution

Flat surface by Dry film SR

Comparison of substrate surface by DF SR and liquid SR

Dry film SR

Uneven

liquid SR

Flat

Cross section on the hole area

Nanya PCB Corporation
Packaging Substrate Reliability Test
Purpose of substrate level reliability test

1. In order to realize the substrate reliability after package and product level in advance.

2. By applying some specific condition on the substrate, to simulate the actual condition after package or product level in a short term test, then define the risk level of the substrate quality.

Substrate can work \rightarrow Reliability test \rightarrow How long the substrate can work

Substrate Life time ??

Substrate workable condition ??
## Summary of the major reliability test item for WB/FC- CSP

<table>
<thead>
<tr>
<th>Test item</th>
<th>Test Purpose</th>
<th>Test Condition</th>
<th>Spec. reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Precon, IPC L3</td>
<td>Simulating the pre-condition for assembly</td>
<td>30C/60% RH, 192hrs</td>
<td>JESD22-A113-B</td>
</tr>
<tr>
<td>TSB (Thermal Shock B)</td>
<td>Evaluating the influence after severe temperature change</td>
<td>-55 deg. C (cold oil) ~ 125 deg. C (hot oil), 1000 cycles</td>
<td>JESD22-A106-A</td>
</tr>
<tr>
<td>TSC (Thermal Shock C)</td>
<td>Evaluating the influence after severe temperature change</td>
<td>-65 deg. C (cold oil) ~ 155 deg. C (hot oil), 1000 cycles</td>
<td>JESD22-A106-A</td>
</tr>
<tr>
<td>bHAST (Biased Highly Accelerated Stress Test)</td>
<td>Evaluating the ion migration situation under high temp./high humidity/high voltage surrounding</td>
<td>130 deg. C 85% RH 1.9V or 3.5V 168 hrs</td>
<td>JESD22-A110-B</td>
</tr>
<tr>
<td>Ball Shear Test</td>
<td>Bonding strength for solder joint reliability</td>
<td>Test speed: 300 um/s Test load: 820 g</td>
<td>XA-TW-313</td>
</tr>
<tr>
<td>Cold Ball Pull</td>
<td>Bonding strength for solder joint reliability</td>
<td>Test speed: 5000 um/s Test load: 25 g</td>
<td>XA-TW-329</td>
</tr>
<tr>
<td>Peel Strength</td>
<td>Bonding strength between copper &amp; dielectric</td>
<td>Cu thickness: 30um Peel speed: 50um/s</td>
<td>JESD22-A103-B</td>
</tr>
<tr>
<td>Wire-bond Pull Strength</td>
<td>Bonding strength between Au-wire &amp; bond finger</td>
<td>Wire diameter: 1.2 mil</td>
<td></td>
</tr>
</tbody>
</table>

### Most of the criteria of substrate reliability test follows the JEDEC spec, which is widely used in semiconductor industry.
Substrate level reliability test procedure

1. Substrate level reliability test items are divide into in line & end of line test. In line test data can be collected during the process, and end of line test data is collected before outgoing.

2. End of line test items divide into long term & short term test, the definition comes from the time used for the test.

3. All substrate reliability tests are done to ensure no issues after package and product level.
1. Electronic device is aiming for “Lighter”, “Smaller” and “Thinner” but remains the high performance & multi-function requirement and also low cost.

2. Packaging substrate needs to meet the trend of electronic devices. New material and process are developed to provide the solution for both technology & cost to meet this trend.

Nanya PCB Corporation
Q & A

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Thank you