LARGE BODY FCBGA SUBSTRATE

KOICHI NONOMURA

Department of Product Design Engineering
Organic Package Division #1, Yasu, Shiga, Japan

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2. Technology Roadmap
3. Product Experience
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KYOCERA SLC Technologies Corporation
FCBGA Substrate Overview

- **Core Layer**
  - Thickness: 0.4 ~ 0.8mm
  - Material: Glass Reinforce Epoxy Resin
  - CTE: < 16ppm/degC

- **Build up Layer**
  - Thickness: 0.03 ~ 0.035mm
  - Material: Epoxy Resin
  - CTE: < 50ppm/degC, Loss Tangent < 0.020

- **Solder Resist Layer**
  - Thickness: 0.015 ~ 0.025mm
  - Material: Resin
  - CTE: < 60ppm/degC

**System Level CTE View**

- **Silicon Chip**
  - CTE typical: 3.0ppm/degC

- **Organic Composite Substrate**
  - CTE typical: 16 ~ 18ppm/degC

- **Organic Mother Board**
  - CTE typical: 17ppm/degC
<table>
<thead>
<tr>
<th>Substrate Category</th>
<th>Substrate Size (mm)</th>
<th>Substrate IO Count</th>
<th>Application Products</th>
</tr>
</thead>
<tbody>
<tr>
<td>FCCSP</td>
<td>Below 15.0 x 15.0mm</td>
<td>Below 841 0.5mm pitch full matrix</td>
<td>Cell Phone Processor</td>
</tr>
<tr>
<td>FCBGA Small</td>
<td>15.0 x 15.0mm to 35.0 x 35.0mm</td>
<td>Below 1156 1mm pitch full matrix</td>
<td>DSP, ASIC</td>
</tr>
<tr>
<td>FCBGA Medium</td>
<td>35.0 x 35.0mm to 42.5 x 42.5mm</td>
<td>1156 to 1681 1mm pitch full matrix</td>
<td>MPU, ASIC</td>
</tr>
<tr>
<td>FCBGA Large</td>
<td>45.0 x 45.0mm to 55.0 x 55.0mm</td>
<td>1936 to 2916 1mm pitch full matrix</td>
<td>MPU, ASIC</td>
</tr>
</tbody>
</table>
FCBGA Technology Roadmap Overview

- **Substrate Size** → Higher IO Count
  - 4-4-4 Thick Core
  - 6-4-6 Thick Core
  - 8L Coreless 10L Coreless
  - 4-2-4 Thin Core

- **Density** → Finer FC Pitch
  - 6L Coreless
  - 8L Coreless
  - 10L Coreless

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# Large Body FCBGA Product Experience

<table>
<thead>
<tr>
<th>Application</th>
<th>MPU</th>
<th>ASIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stack up</td>
<td>6-4-6</td>
<td>4-2-4</td>
</tr>
<tr>
<td>Core Thickness</td>
<td>600um</td>
<td>400um</td>
</tr>
<tr>
<td>Minimum Via Pitch Build up / Core</td>
<td>125um / 600um</td>
<td>125um / 250um</td>
</tr>
<tr>
<td>Substrate Size</td>
<td>50.0 x 50.0mm</td>
<td>52.5 x 52.5mm</td>
</tr>
<tr>
<td>Chip IO Count / Pitch</td>
<td>7352+1598 / 200um</td>
<td>3390 / 225um</td>
</tr>
<tr>
<td>Chip Inter Connect</td>
<td>C4</td>
<td>C4</td>
</tr>
<tr>
<td>Substrate IO Count / Pitch</td>
<td>2295 / 1mm</td>
<td>2577 / 1mm</td>
</tr>
<tr>
<td>Board Inter Connect</td>
<td>LGA Socket</td>
<td>BGA</td>
</tr>
</tbody>
</table>
Large Body FCBGA Substrate Challenge

- Large Chip
- Large Substrate

### Chip Size Assessment for Large Body Substrate

<table>
<thead>
<tr>
<th>Substrate Size (mm)</th>
<th>Substrate IO Count 1mm pitch</th>
<th>FC Bump IO</th>
<th>Chip Size(mm)</th>
<th>Pad Pitch: 200um Opening: 130um</th>
<th>Pad Pitch: 150um Opening: 70um</th>
<th>Pad Pitch: 130um Opening: 60um</th>
<th>Pad Pitch: 120um Opening: 60um</th>
</tr>
</thead>
<tbody>
<tr>
<td>45x45</td>
<td>1681</td>
<td>6724</td>
<td>16.2</td>
<td>12.2</td>
<td>10.5</td>
<td>9.7</td>
<td></td>
</tr>
<tr>
<td>50x50</td>
<td>2401</td>
<td>9604</td>
<td>19.4</td>
<td>14.6</td>
<td>12.6</td>
<td>11.6</td>
<td></td>
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<tr>
<td>55x55</td>
<td>2809</td>
<td>11236</td>
<td>21.0</td>
<td>15.8</td>
<td>13.7</td>
<td>12.6</td>
<td></td>
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<tr>
<td>60x60</td>
<td>3481</td>
<td>13924</td>
<td>23.4</td>
<td>17.6</td>
<td>15.2</td>
<td>14.0</td>
<td></td>
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<tr>
<td>65x65</td>
<td>4096</td>
<td>16384</td>
<td>25.4</td>
<td>19.1</td>
<td>16.5</td>
<td>15.2</td>
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</tr>
</tbody>
</table>
Large Chip Challenge

Current Material Set Substrate Composite CTE Model

- 6-2-6: 6 Wiring Layer (60% Cu Ratio) Strip Line Structure
- 4-2-4: 4 Wiring Layer (60% Cu Ratio) Strip Line Structure

16.9 ppm/degC CTE Miss Match FC Pad Off Set Study

- Delta TEMP 160degC
- Delta TEMP 196degC
- Delta TEMP 140degC

Chip Size (mm) vs. Core Thickness (um)
## Large Substrate Challenge

### Wiring Length Study on Large Substrate

<table>
<thead>
<tr>
<th>Substrate IO Count</th>
<th>1.0mm BGA Pitch</th>
<th>0.8mm BGA Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Substrate Size (mm)</td>
<td>Wiring Length (mm)</td>
</tr>
<tr>
<td>1681</td>
<td>45x45</td>
<td>16.4</td>
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<td>2401</td>
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<td>4096</td>
<td>65x65</td>
<td>23.0</td>
</tr>
</tbody>
</table>

### Differential Pair Wiring Electrical Loss Model

- **2809 IO, 45x45mm, 0.8mm BGA, 14.6mm Length**
- **2809 IO, 55x55mm, 1.0mm BGA, 19.6mm Length**
- **4096 IO, 65x65mm, 1.0mm BGA, 23.0mm Length**
Large Body FCBGA Substrate Input and Challenge Summary

• Large Chip
  1. Input for Device and Assembly Customer
     ✔ CTE Miss-Match in Between Chip and Substrate
     ✔ Fine FC Pitch Pad Off Set for Large Chip with ASM TEMP
  2. Substrate Challenge
     ✔ Low Composite CTE Control for High Stack up and Thin Core
     ✔ Low CTE Dielectric Material Development

• Large Substrate
  1. Input for System Customer
     ✔ Electrical Loss with Longer Trace Wiring on Large Substrate
     ✔ Shorten Trace with 0.8mm Pitch BGA for Better Performance
  2. Substrate Challenge
     ✔ Low Electrical Loss Material Development