NEMI Cost Analysis: Optical Versus Copper Backplanes

Part I: Benchmarking Copper

NEMI project team
Adam Singer
APEX 2004
Overview

• An apology – no optical comparison yet
  – *But, if you leave your card, we’ll send you an update*

• NEMI team goal

• Background on copper and optical technology

• Cost modeling methodology background

• Copper backplane cost analysis

• “The Metric”

• Future work
Optical PCBs – Needed Yet?

• Copper still finding ways to improve
• Market demand for next-gen telecom systems slowed dramatically in 2001-3
• Cost crossover point not yet understood

Reason for NEMI project
- Develop cost models
- Compare Cu and optical costs
NEMI’s Goal

Crossover zone: changeover will not be immediate, but will range depending on issues including cost sensitivity, reliability, and design limitations.
**Optoelectronics Concepts**

**Photons**
- Zero Rest mass
- $FxD > 10^{14}$ Hz x 100km
- Boson $\Rightarrow$ Mult. Signals
- OE Conversion needed

*Best for long distance, high speed*

**Electrons**
- $9.11 \times 10^{-31}$ kg
- $FxD > 10^{10}$ Hz x 0.001km
- Fermion: One Signal
- No OE Conversion

*Best for very short distance (<5 meters) at moderate to high speed*
Value to Market
“Faster” Backplanes

- Making the copper thicker
- Making the dielectric layer thinner
- Using dielectrics with lower loss tangents
- Adding more signal layers
- Minimizing the signal length
- Maximizing distance between signals
- Making the board larger (wider and longer) to handle more signals per layer
# Copper Roadmap

## Generic Copper Backplane Bandwidth Technology Roadmap

<table>
<thead>
<tr>
<th>PCB Technology</th>
<th>Materials</th>
<th>Technology</th>
<th>Connector Launch Design</th>
<th>Via Design</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FR-4, Df = 0.020</td>
<td>PPO / CE, Df = 0.015-0.008</td>
<td>BT / APPE, Df = 0.010</td>
<td>PTFE, Df = 0.009 - 0.003</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PTFE / Ceramic, Df = 0.002 - 0.0008</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Processes</td>
<td></td>
<td>Single transmission line, Length management</td>
<td>Differential pair, length, type (Surface microstrip, embedded microstrip, stripline, edge coupled, broadside coupled), location in stack</td>
<td></td>
</tr>
<tr>
<td>Transmission Line Design</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Connector Technology</td>
<td>Teradyne connectors</td>
<td>ERmet</td>
<td>VHDM &amp; VHDM L-series</td>
<td>VHDM-HSD</td>
</tr>
<tr>
<td></td>
<td>ERmi</td>
<td>Ermet ZD</td>
<td>ERmetZD</td>
<td>Ermet Zero XT</td>
</tr>
<tr>
<td></td>
<td>Tyco connectors</td>
<td>HM-ZD</td>
<td>Z-Pack HM-ZD</td>
<td>Z-Pack HM-ZD</td>
</tr>
<tr>
<td></td>
<td>MultiGig RT-1</td>
<td>MultiGig RT-2</td>
<td>MultiGig RT-3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FCI</td>
<td>Metral 2000</td>
<td>AirMax VS</td>
<td>AirMax VS</td>
</tr>
<tr>
<td></td>
<td>Metral 4000</td>
<td>AirMax VS</td>
<td>AirMax</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fujitsu</td>
<td>FCN-261200x</td>
<td>FCN260D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Winchester</td>
<td>Xcell</td>
<td>SIP-1000 I platform</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Molex</td>
<td>Molex is a Teradyne licensee</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Receiver / Transmitter Signal Conditioning Chip Set</td>
<td>Taps required</td>
<td>None</td>
<td>Required</td>
<td>One</td>
</tr>
<tr>
<td>Velio</td>
<td>GigaCore</td>
<td>GigaCore2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bus Architecture</td>
<td>Shared Bus?</td>
<td>Point to Point?</td>
<td>Multi point?</td>
<td>Sub type?</td>
</tr>
</tbody>
</table>
• Telecom capex dropped in ’03
  – Internet bubble effects still present
• Recovery in the ’04-’05 timeframe
  – Despite bubble, internet usage doubles every year
Market Status

LONG HAUL BACKBONE NETWORK CAPACITY IN THE US

Capacity (Tbps)

2002 installed capacity is sufficient until 2004

Required Capacity

Source: RHK, FCC, KMI, Broadband Week, Goldman Sachs and McKinsey estimate

2000 2001 2002 2003 2004 2005

Installed Lit Capacity

Courtesy of Prismark, September 2002
Optical Backplanes

• Today: optical fibers / fiber mat on surface
  – Point-to-point limitation
  – Splice or connector required for each fiber end
  – **Costly**
• Future: planar optical waveguides
  – Patternable layer on or within PCB
  – Bus architecture
  – Laser/detector arrays “self-aligned” in assembly
Current Challenges for Future Optical Backplanes

• Optical connector technology
  – Through-hole or SMT?
• Turning 90º with acceptable loss
• Reliability
• Manufacturability
• Cost of components and assembly
# The Cost Model

## DESIGN ISSUES

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Cu backplane</th>
</tr>
</thead>
<tbody>
<tr>
<td>Annual Production Volume</td>
<td>117 (000) board per year</td>
</tr>
</tbody>
</table>

Other assumptions:
- 8 mil lines
- 8 mil spaces
- 20 mil minimum drill diameter
- [The inputs above do not yet affect the model]

<table>
<thead>
<tr>
<th>Panel Length</th>
<th>Panel Width</th>
<th>Finishing Board Length</th>
<th>Finishing Board Width</th>
<th>Drilled Through-Holes</th>
<th>Minimum Panel Edge Margin</th>
<th>Minimum Space Between Boards</th>
<th>Boards Per Panel</th>
</tr>
</thead>
<tbody>
<tr>
<td>24 inch</td>
<td>20 inch</td>
<td>20 inch</td>
<td>18 inch</td>
<td>5,000 per board</td>
<td>0.8 inch</td>
<td>0.1 inch</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Number of Innerlayer Pairs - FR-4</th>
<th>Wgt Price</th>
<th>Lam Price</th>
<th>Lam Pricewg</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>$2.17</td>
<td>$2.17</td>
<td></td>
</tr>
</tbody>
</table>

Yield of Innerlayer Pairs: 94.0% INNERYIELD

Yield of Boards, Post-Lamination: 99.2% * number of innerlayer pairs
Yield of Boards, Post-Lamination: 88.0% TOTYIELD

## PROCESSING ISSUES

Sequence of Operations:
- Product Description
- Facility Description
- Operation Database
- Cost Summary
- Go
Models in Manufacturing

• Cost models
  – “Bottoms-up” like activities based costing
  – Engineering relationships
  – Purchasing inventory for BOM optimization
  – Scope: the mfg facility
  – Output: cost per part by operation and by factor (materials, equipment, and so on)

• Pricing models
  – Rules of thumb based on reference parts
  – Accounting data dependency
  – Profit included
  – Scope: include all business costs
  – Output: price per part

• Business models
  – “Bottoms up”
  – Scope: all of the business
  – Output: ROI, time to breakeven, NPV, and others
Cost Modeling Method

• Based on Technical Cost Modeling, as developed by IBIS Associates / MIT
• Activities Based Costing, plus engineering relationships
  – Cycle time = f(design, machine speed)
Cost Model Context

- North American facility
- Equipment investment assumes max 24 inch width conveyors
- Yields reflective of 8 mil line / space
- Drilling reflects 20 mil minimum diameter
- Medium throughput (350Ksqft/yr topsurface)
Facilities Assumptions

<table>
<thead>
<tr>
<th>Assumption</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct Labor Wage</td>
<td>$15.00/hour</td>
</tr>
<tr>
<td>Indirect Labor Salary</td>
<td>$50,000/year</td>
</tr>
<tr>
<td>Indirect Laborers:Direct Laborer Ratio</td>
<td>0.07 ilab/dlab</td>
</tr>
<tr>
<td>Indirect Labor Shifts per Day</td>
<td>1.2 shift/day</td>
</tr>
<tr>
<td>Benefits on Wage/Salary</td>
<td>35.0%</td>
</tr>
<tr>
<td>Working Days per Year</td>
<td>360 d/yr</td>
</tr>
<tr>
<td>Working Hours per Day</td>
<td>24 h/d</td>
</tr>
<tr>
<td>Capital Recovery Rate</td>
<td>8% /yr</td>
</tr>
<tr>
<td>Working Capital Period</td>
<td>1 mo(s)</td>
</tr>
<tr>
<td>Equipment Depreciation Life</td>
<td>5 yrs</td>
</tr>
<tr>
<td>Building Recovery Life</td>
<td>20 yrs</td>
</tr>
<tr>
<td>Total Space:Work Space Ratio</td>
<td>1.25 : 1</td>
</tr>
<tr>
<td>Price of Electricity</td>
<td>$0.110/kWh</td>
</tr>
<tr>
<td>Dedicated Equipment?</td>
<td>0 [1=Y 0=N]</td>
</tr>
<tr>
<td>Equipment Investment Scaling Factor</td>
<td>100% of baseline</td>
</tr>
<tr>
<td>Non-Recurring Engineering</td>
<td>$1,000 per design</td>
</tr>
</tbody>
</table>
Product Assumptions

- 32 metal layers
- No buried vias
- FR-4
- 24x20 inch panel
- 20x18 inch finished board
- 5,000 drilled holes per board
- ~1-3 Gbps performance
### Process Flow

#### INNERLAYER
- **Rec1**: Receive Laminate
- **Cln1**: Clean - Chemical
- **Pat1**: Laminate Dry Film
- **Pat2**: Expose Dry Film
- **Pat3**: Photo Plotter
- **Pat4**: Develop Dry Film
- **Pat5**: Etch Cu - Strip Resist
- **Pat6**: Film Punch
- **Pat7**: Registration Punch
- **Ins1**: AOI
- **Prp1**: Oxide Coating System

#### OUTERLAYER
- **Lam1**: Receive Prepreg
- **Lam2**: Receive Foil
- **Lam3**: Kitting and Lay-up Area
- **Lam4**: Laminate Multilayer (Press)
- **Lam5**: Routing - Depin and Debook
- **Lam6**: Deflash & ID
- **Drl1**: Pin Stack - Before Drill
- **Drl2**: Drill Through Holes
- **Drl4**: Deburring
- **Drl5**: Auto Hole Check
- **Drl6**: Desmear & Etchback - PM
- **Plt1**: Plate E'tless Cu
- **Plt2**: E'tytic Strike Cu
- **Cln2**: Clean - Pumice Scrub
- **Pat1**: Laminate Dry Film
- **Pat2**: Expose Dry Film
- **Pat3**: Photo Plotter
- **Pat4**: Develop Dry Film
- **Plt3**: Plate E'tytic Cu & Sn
- **Pat6**: Strip Resist, Etch Cu, Strip Sn
- **Drl8**: Manual Hole Size Check
- **Ins1**: AOI
- **Rep1**: Repair Opens & Shorts
- **Cln1**: Clean - Chemical
- **Sma1**: Flood Coat Solder Mask (DS Scren)
- **Sma2**: Tack Cure
- **Sma3**: Expose Solder Mask
- **Sma4**: Develop Solder Mask
- **Sma5**: UV Cure
- **Sma6**: Cure
- **Hsl1**: HASL & Clean
- **Nmn1**: Nomenclature Print
- **Fin1**: Routing - Depaneling
- **Fin2**: Clean
- **Ins2**: Electrical Test
- **Ins3**: Flying Probe
- **Ins4**: Find, Analyze, Repair, Retest
- **Ins5**: Final Inspection & Audit
- **Fin2**: Clean
- **Fin4**: Final packaging & labeling
- **Wst1**: Waste Treatment
- **Nre1**: Non-recurring Engineering
Cost Summary

Cost Summary (per board)

<table>
<thead>
<tr>
<th></th>
<th>Innerlayer Cost</th>
<th>Outerlayer Cost</th>
<th>Total Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cost ($)</td>
<td>$416</td>
<td>$144</td>
<td>$560</td>
</tr>
<tr>
<td>%</td>
<td>74%</td>
<td>26%</td>
<td></td>
</tr>
</tbody>
</table>

Total Equipment Investment $44.0 MM
Total Building Space 23.0 K sqft

Total Building Investment $2.1 MM

Cost/Sqin (Top Surface, Board) $1.55
Cost/Sqin (Top Surface, Panel) $1.17
Cost/Sqin (Per Metal Layer) $0.036

Cost Factor Breakdown (per board)

<table>
<thead>
<tr>
<th></th>
<th>Dir Labor</th>
<th>Material</th>
<th>Utilities</th>
<th>Tooling</th>
<th>Equip</th>
<th>Bldg</th>
<th>Ind Labor</th>
<th>Maint</th>
<th>Capital</th>
</tr>
</thead>
<tbody>
<tr>
<td>Innerlayer Cost</td>
<td>$86</td>
<td>$258</td>
<td>$2</td>
<td>$10</td>
<td>$34</td>
<td>$0</td>
<td>$9</td>
<td>$7</td>
<td>$10</td>
</tr>
<tr>
<td>% of innerlayer</td>
<td>21%</td>
<td>62%</td>
<td>0%</td>
<td>2%</td>
<td>8%</td>
<td>0%</td>
<td>2%</td>
<td>2%</td>
<td>2%</td>
</tr>
<tr>
<td>Outerlayer Cost</td>
<td>$33</td>
<td>$49</td>
<td>$1</td>
<td>$18</td>
<td>$25</td>
<td>$0</td>
<td>$5</td>
<td>$5</td>
<td>$7</td>
</tr>
<tr>
<td>% of outerlayer</td>
<td>23%</td>
<td>34%</td>
<td>1%</td>
<td>13%</td>
<td>18%</td>
<td>0%</td>
<td>4%</td>
<td>4%</td>
<td>5%</td>
</tr>
<tr>
<td>Total Cost</td>
<td>$119</td>
<td>$307</td>
<td>$3</td>
<td>$28</td>
<td>$59</td>
<td>$1</td>
<td>$14</td>
<td>$12</td>
<td>$17</td>
</tr>
<tr>
<td>% of total</td>
<td>21%</td>
<td>55%</td>
<td>1%</td>
<td>5%</td>
<td>11%</td>
<td>0%</td>
<td>2%</td>
<td>2%</td>
<td>3%</td>
</tr>
</tbody>
</table>

Validated by two backplane fabricators:
+/- 10% of their costs

Cookson Electronics

shared intelligence™
## Cost Analysis

<table>
<thead>
<tr>
<th>Case</th>
<th>No. of Drilled Holes</th>
<th>No. of Metal Lam'n Layers</th>
<th>Post Yield</th>
<th>Total Board Cost</th>
<th>Cost per Metal Layer</th>
<th>Cost per Top Panel Surface Sqin</th>
<th>Cost per Metal Lyr sqin</th>
<th>Total Invest (MM)</th>
<th>Total Equipment Space (Ksqft)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline Case</td>
<td>5,000</td>
<td>32</td>
<td>88%</td>
<td>$560</td>
<td>$17.49</td>
<td>$1.17</td>
<td>$0.036</td>
<td>$44</td>
<td>23.0</td>
</tr>
<tr>
<td>Holes Lower</td>
<td>2,500</td>
<td>32</td>
<td>88%</td>
<td>$545</td>
<td>$17</td>
<td>$1.14</td>
<td>$0.036</td>
<td>$43</td>
<td>22.1</td>
</tr>
<tr>
<td>Holes Higher</td>
<td>7,500</td>
<td>32</td>
<td>88%</td>
<td>$574</td>
<td>$17.94</td>
<td>$1.20</td>
<td>$0.037</td>
<td>$45</td>
<td>24.2</td>
</tr>
<tr>
<td>Holes Highest</td>
<td>10,000</td>
<td>32</td>
<td>88%</td>
<td>$588</td>
<td>$18.39</td>
<td>$1.23</td>
<td>$0.038</td>
<td>$46</td>
<td>25.1</td>
</tr>
<tr>
<td>Layers Lower</td>
<td>5,000</td>
<td>24</td>
<td>91%</td>
<td>$423</td>
<td>$17.61</td>
<td>$0.88</td>
<td>$0.037</td>
<td>$38</td>
<td>20.0</td>
</tr>
<tr>
<td>Layers Higher</td>
<td>5,000</td>
<td>36</td>
<td>86%</td>
<td>$634</td>
<td>$17.61</td>
<td>$1.32</td>
<td>$0.037</td>
<td>$47</td>
<td>24.4</td>
</tr>
<tr>
<td>Holes &amp; Layers Lowest</td>
<td>2,500</td>
<td>24</td>
<td>91%</td>
<td>$411</td>
<td>$17.14</td>
<td>$0.86</td>
<td>$0.036</td>
<td>$37</td>
<td>19.1</td>
</tr>
<tr>
<td>Holes &amp; Layers Highest</td>
<td>10,000</td>
<td>36</td>
<td>86%</td>
<td>$668</td>
<td>$18.56</td>
<td>$1.39</td>
<td>$0.039</td>
<td>$49</td>
<td>26.5</td>
</tr>
</tbody>
</table>
"The Metric"

So far, cost has focused on board cost

But is that fair comparison for optical PCBs?
   – Performance will be at a different level
   – Connectors will be different
   – Assembly method probably different

So, what metric to use?
“The Metric”

- **Cost per Gbps per top surface square inch**: takes into account the number of metal layers (not including ground/power planes), maximum Gbps per channel, and maximum channels per inch (as determined by minimum line/space rules)
- **Cost per Gbps per channel per meter**: takes into account losses per unit length and maximum Gbps per channel
- **Cost per Gbps per board**: takes into account design-dependent maximum Gbps for all channels on the board at any one time
- **Cost per Gbps per board cross-section**: takes into account maximum Gbps per channel and the number of channels cut by a cross-section dividing the length of the board into equal parts

- Suggestions?
Future Work

- Next generation copper PCB for 10Gbps
- Assembly costs
- Optical PCB technology
  - Embedded, edge-coupled
  - Embedded, surface-coupled
    - Mirror/grating/in-via-coupling
    - Bent waveguide
Summary

- Copper backplane model in place & validated
- Your input on optical technology needed
- Your input on cost-performance metric needed