



International Electronics Manufacturing Initiative

**Optoelectronics TIG Gap
Analysis Meeting**

***Peter Arrowsmith, Celestica
Anaheim Marriott
March 7, 2005***

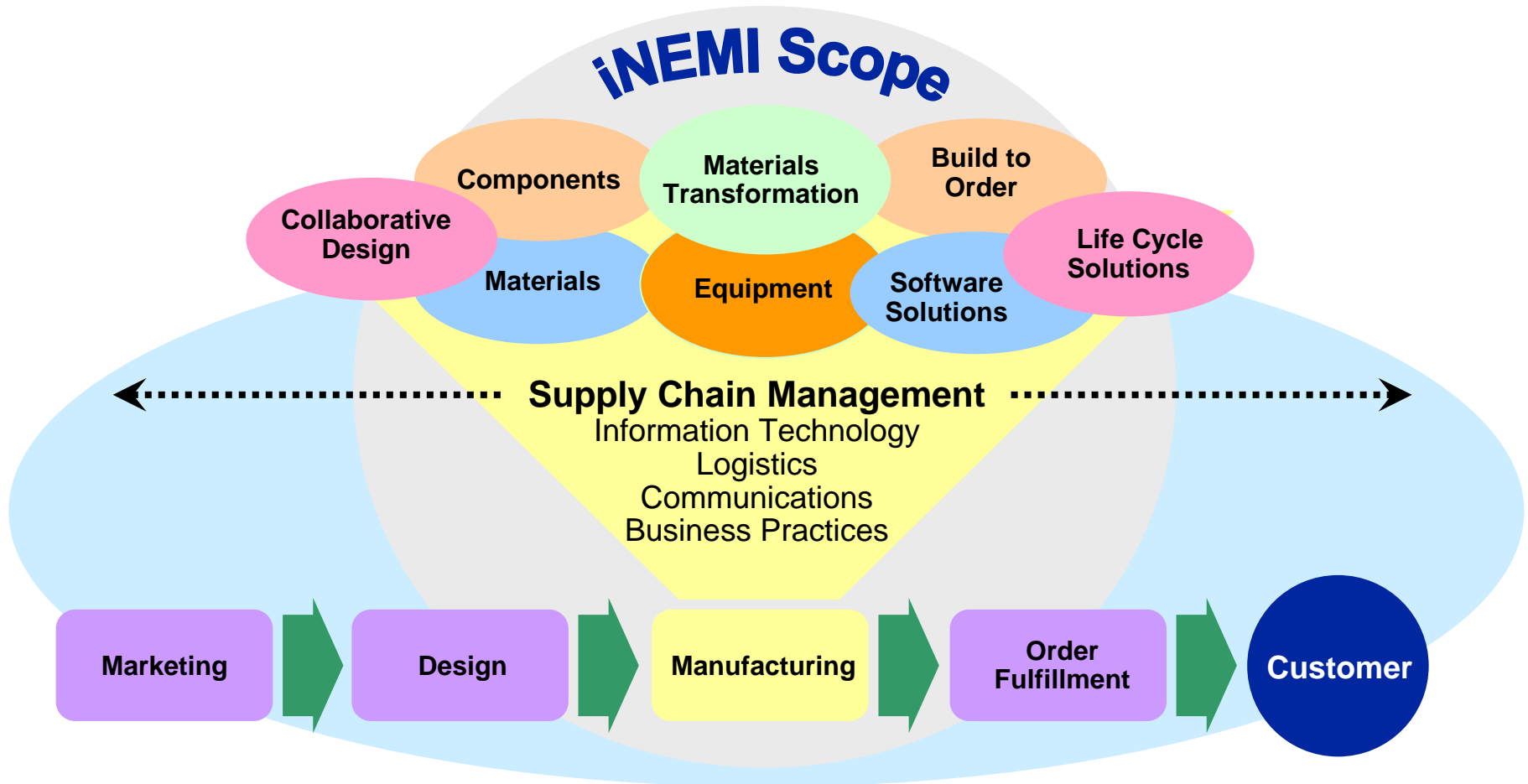
- **Introduction**
Goals of meeting **Peter Arrowsmith**
- **iNEMI Process** **Chuck Richardson, iNEMI**
- **iNEMI Project Review** **David Godlewski, iNEMI**
- **High Level conclusions/gaps iNEMI 2004 Roadmap**
- **Working session to develop iNEMI Strategy/Plan Outline - All**
 - **Review/prioritize gaps from roadmap**
 - **Identify other opportunities (based on industry needs)**
 - **Prioritize list**
 - **Develop outline of plan**
- **Identify next steps/closure of meeting - All**

- **Optoelectronics Chapters of the 2004 iNEMI Roadmap**
 - **Compares technology trends with anticipated product needs**
 - **Identifies “gaps” and “showstoppers” that potentially threaten product realization**
 - **In-depth discussions at this meeting will be used to develop action plans that address the needs, and help close the gaps with follow-up activities as the initiation of deployment projects**

iNEMI Process

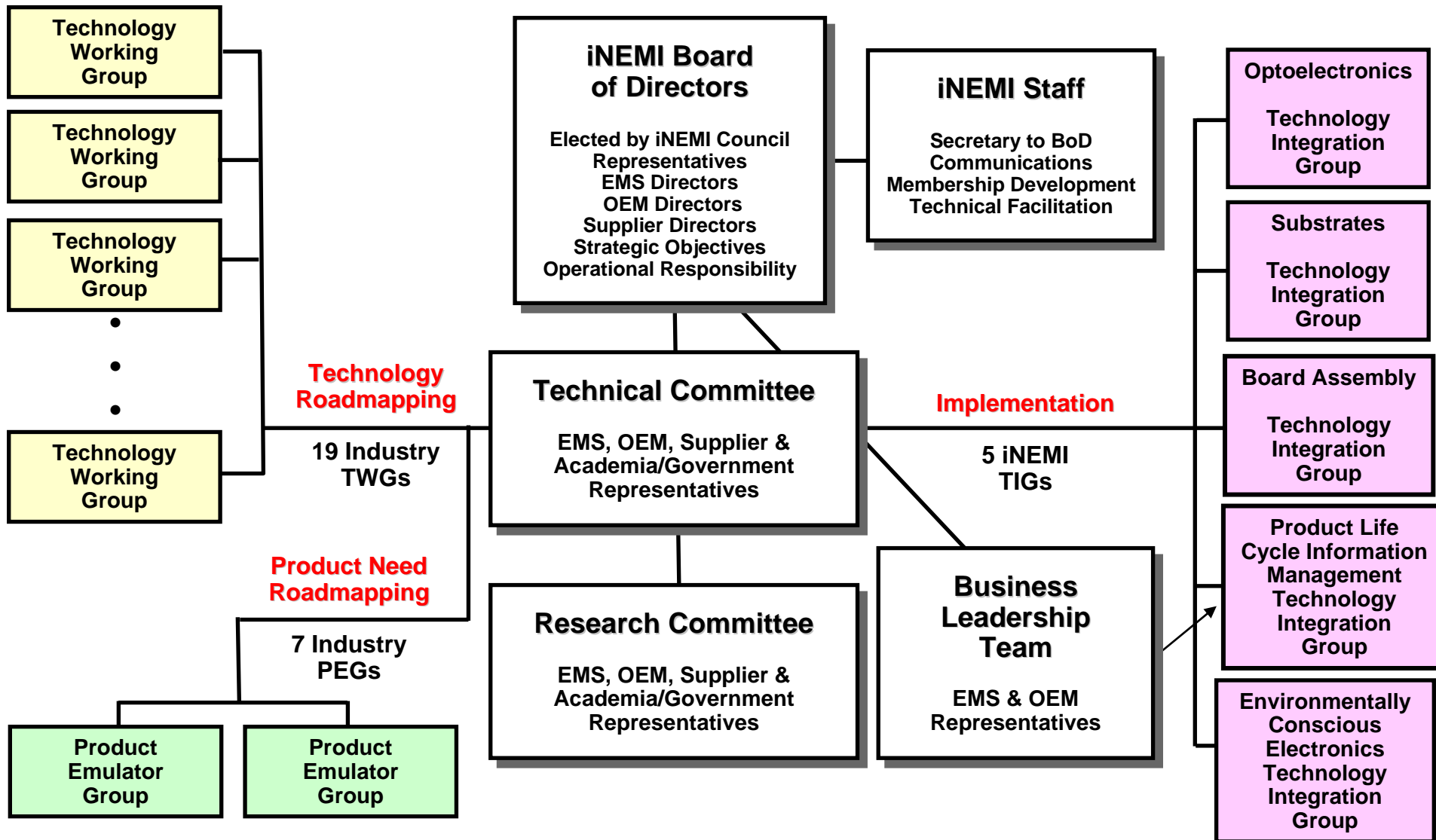
Chuck Richardson, iNEMI

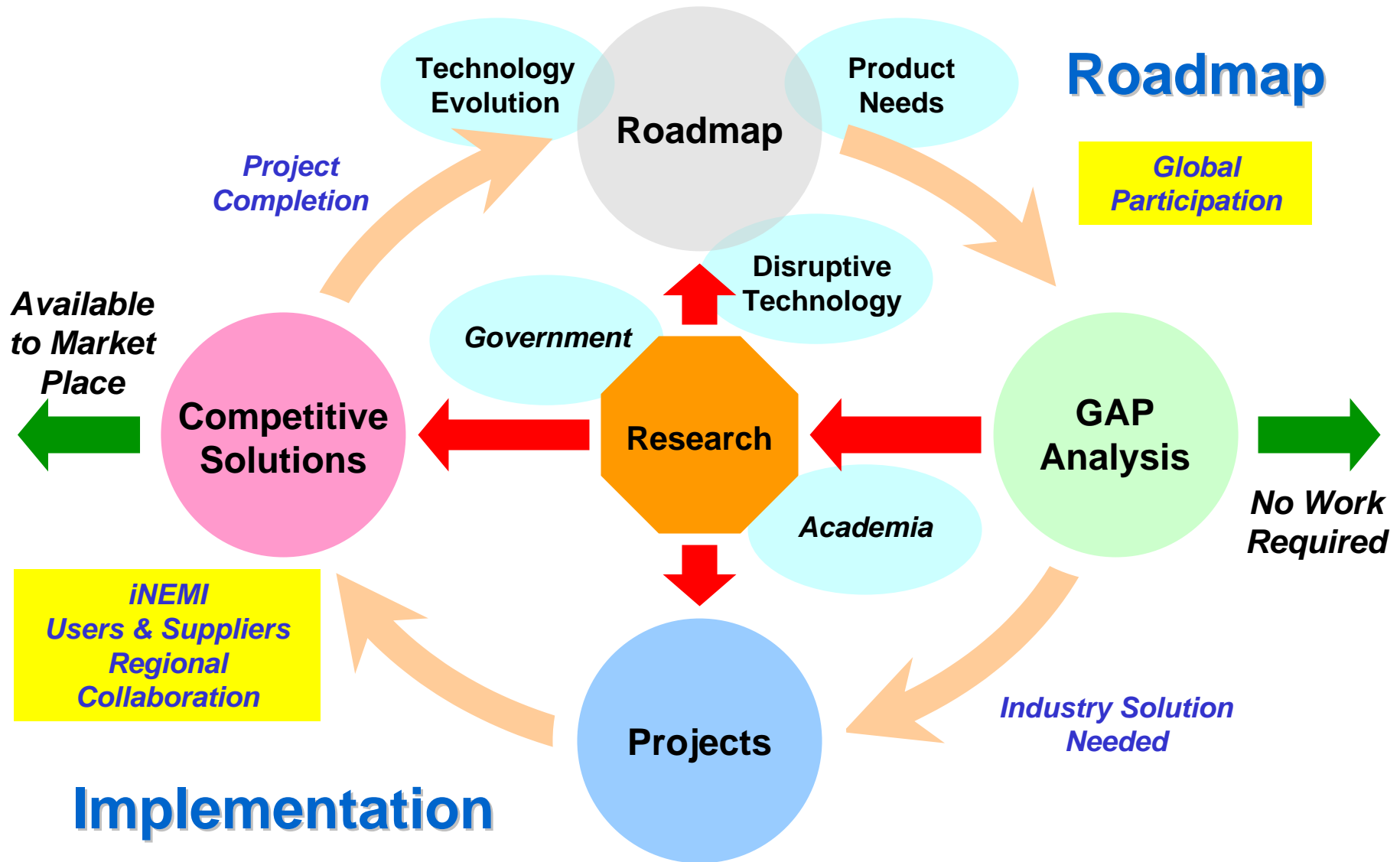
*Assure Leadership of the Global Electronics Manufacturing Supply Chain
for the benefit of members and the industry*



Leverage the combined power of member companies to provide industry leadership

- **iNEMI roadmaps the global needs of the electronics industry**
 - **- Evolution of existing technologies**
 - **- Prediction of emerging/innovative technologies**
- **iNEMI identifies gaps (both business & technical) in the electronics infrastructure**
- **iNEMI stimulates research/innovation to fill gaps**
- **iNEMI establishes implementation projects to eliminate gaps**
- **iNEMI stimulates worldwide standards to speed the introduction of new technology & business practices**
- **iNEMI works with other organizations to ensure that government policy recommendations are aligned with our mission.**





- **Distribute Schedule and Template to TIG Chairs / TC 2/1/05**
- **TIG Chairs Hold Gap Analysis Meetings as Follows:**
 - **iNEMI Board Assembly and Substrates TIG Meeting @ APEX 2/22/05**
 - **iNEMI SIP TIG Meeting - NEW @ APEX 2/23/05**
 - **iNEMI Environmental TIG Meeting @ APEX 2/24/05, @ ISEE 5/16-19/05**
 - **iNEMI PLIM TIG Meeting @ Intel 3/1-3/05**
 - **iNEMI OPTO TIG Meeting @ OFC 3/6-10/05**
- **TIG Chairs / TC Discuss Gaps / Technical Plan at APEX 2/25/05**
- **Research Committee Telecons 3/3/05, 4/7/05**
- **Drafts from TIGs and RC due 6/17/05**
- **T.C. Face to Face on Technical Plan / Research Priorities in Herndon 6/23-24/05**
- **Release 2005 Research Priorities @ BOD/EI Meetings in Herndon 9/14-15/05**
- **Release 2005 Technical Plan to Members @ SMTAI 9/25-29/05**

- **Outline for each TIG's Technical Plan input**
 - **Introduction**
 - **Gap Analysis and Five-year plan**
 - **What has changed**
 - **TIG Plan**
 - **Projects/programs to focus on short term -prioritize**
 - **Identify areas where research is needed -prioritize**
 - **Summary**

Drivers

Low volumes
Low cost
Bandwidth
Part # red'n

OPTOELECTRONICS ATTRIBUTES

10Gbps longhaul
Emerging module package standards (i.e., SFP, XFP, SNAP-12)
Pb-free incompatible (levels 1&2)
Sensitive materials (heat, handling, moisture and other environmental factors)
Light in-plane to substrate (fiber, flex)
Hybrid integrated optical & electronic systems
Little DFX
Out-of-plane bend issues: PCB fab, losses, coupling efficiency, reliability
Module heat @ 20W max
Component function/ λ stability strongly operating temperature dependent

DEPLOYED TECHNOLOGY

Semi-auto fiber alignment
Multi-step solder, weld, adhesive bond
MSAs define electrical I/O (only)
MEM/MOEMs

RESEARCH & DEVELOPMENT

Photonic band gap/optical crystals
New OE materials
Self/passive part alignment
Embedded waveguides
90° light bend with substrate
1550 nm VCSEL
Fiberless Level 2 assembly

2005

Drivers

Low Cost
Higher volumes
Bandwidth
Robust
Size reduction

OPTOELECTRONICS ATTRIBUTES

40 Gbps longhaul
Standard package types, pluggable (no fiber pigtailed)
Pb-free compatible
More robust OE materials
Out-of-plane light within substrate, optical via
Monolithic O-E integration
Some DFM & DFT
OE/thermal design tools
Bend radius within substrate thickness
Temperature tolerant devices

DEPLOYED TECHNOLOGY

Auto fiber alignment
Self/passive part alignment
Single step bonding
Waveguides couple to connectors
Standards for packages, assembly, datacom rel, etc

RESEARCH & DEVELOPMENT

Low cost SS OE devices, SOA, tuneable
Fiberless Level 2 assembly
All optical network
Optical self test modules
Nanostructures, nano-OEMs

2007

Drivers

Low cost
Higher volumes
Bandwidth
Robust
Size reduction

OPTOELECTRONICS ATTRIBUTES

40 Gbps longhaul
Integrated O-E organic substrates
Tunable, parallel sources/receivers
Monolithic O-E integration
Integrated design tools, for DFX
Transverse coupled waveguides
No active cooling requirement

DEPLOYED TECHNOLOGY

Fiberless Level 2 assembly
Self/passive part alignment
Waveguides coupling to devices
All adhesive bonding
Molded components
Many standards
System interoperability, protocol independent
Configurable optical network

RESEARCH & DEVELOPMENT

Photonic transistor & memory
Optical bit switching
Integrated OE modules based on PBG
Soliton transmission

2009/2011

	2005	2007	2009	2011	Need
Level-1: Device Technology					
VCSEL array yield & reliability, 1550 nm					D, I
Non-cooled, thermally tolerant devices					R, D
O-E integration, based on Si CMOS					R, D
Emerging SS devices, SOA, switches, OBG...					R
Level-2: Packaged component					
Design for manufacturing, test, cost (DFx)					D, I
Passive/self alignment					D, I
Hybrid O-E integration					D
Adhesives for attach & optical coupling					D, I
Pb-free compatibility					I
Waveguide-device coupling					D
Levels 3 & 4: module, sub-system					
Compatible electrical & optical assembly					D, I
Low temp, Pb-free solder attach					I
Fiber assembly (connector, fiber handling)					D, I
Embedded waveguides					D, I
Waveguide-connector coupling (in-plane)					D, I
Optical via (out-of-plane coupling)					D, I
Standards					
Packaging, assembly & test, e.g. IPC 0040					I
Interoperability at system/network level					D, I
Reliability for datacom/last mile applications					D, I
Test: critical parameters/reduced capex					I
Industry stnd optical interconnects					D, I

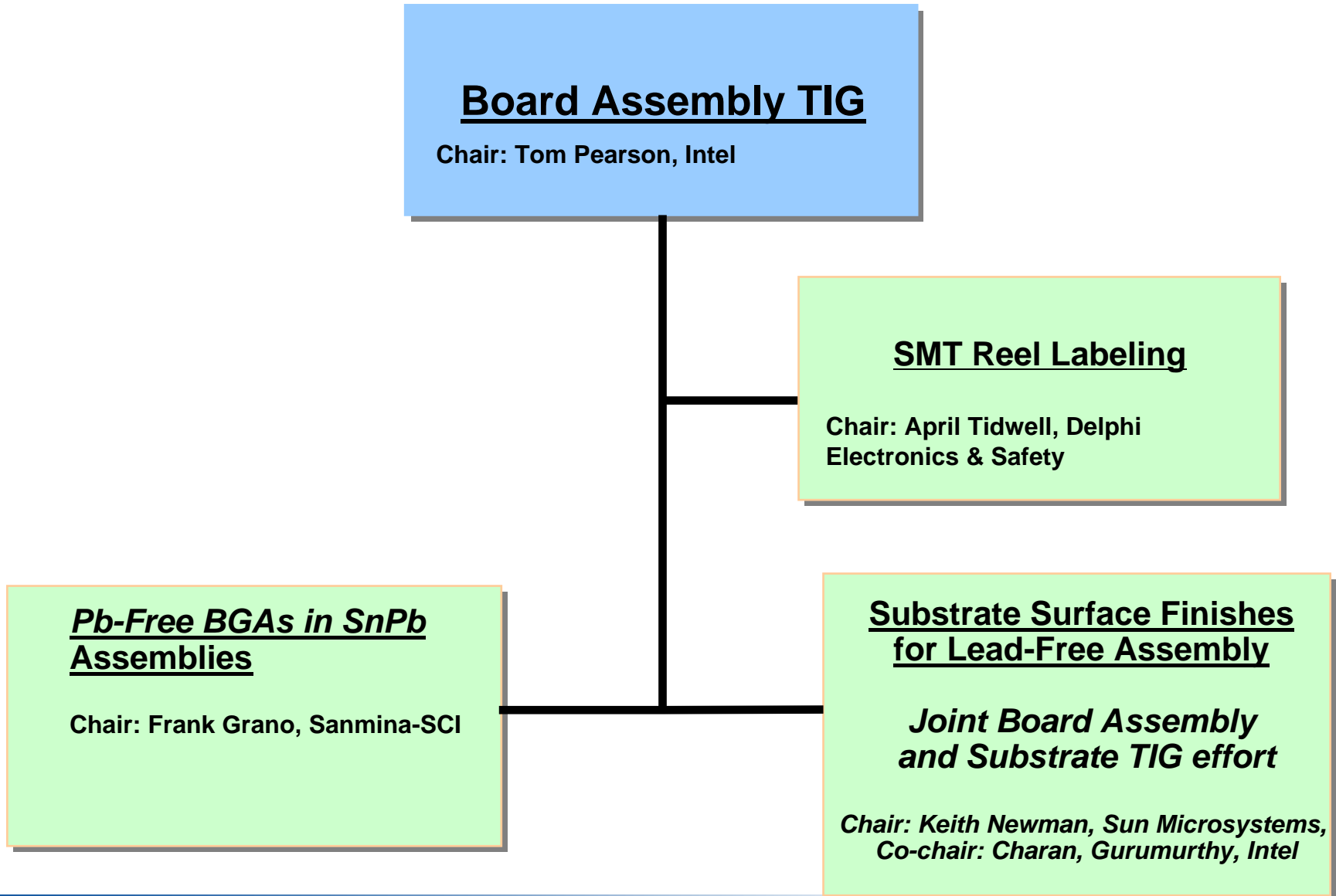


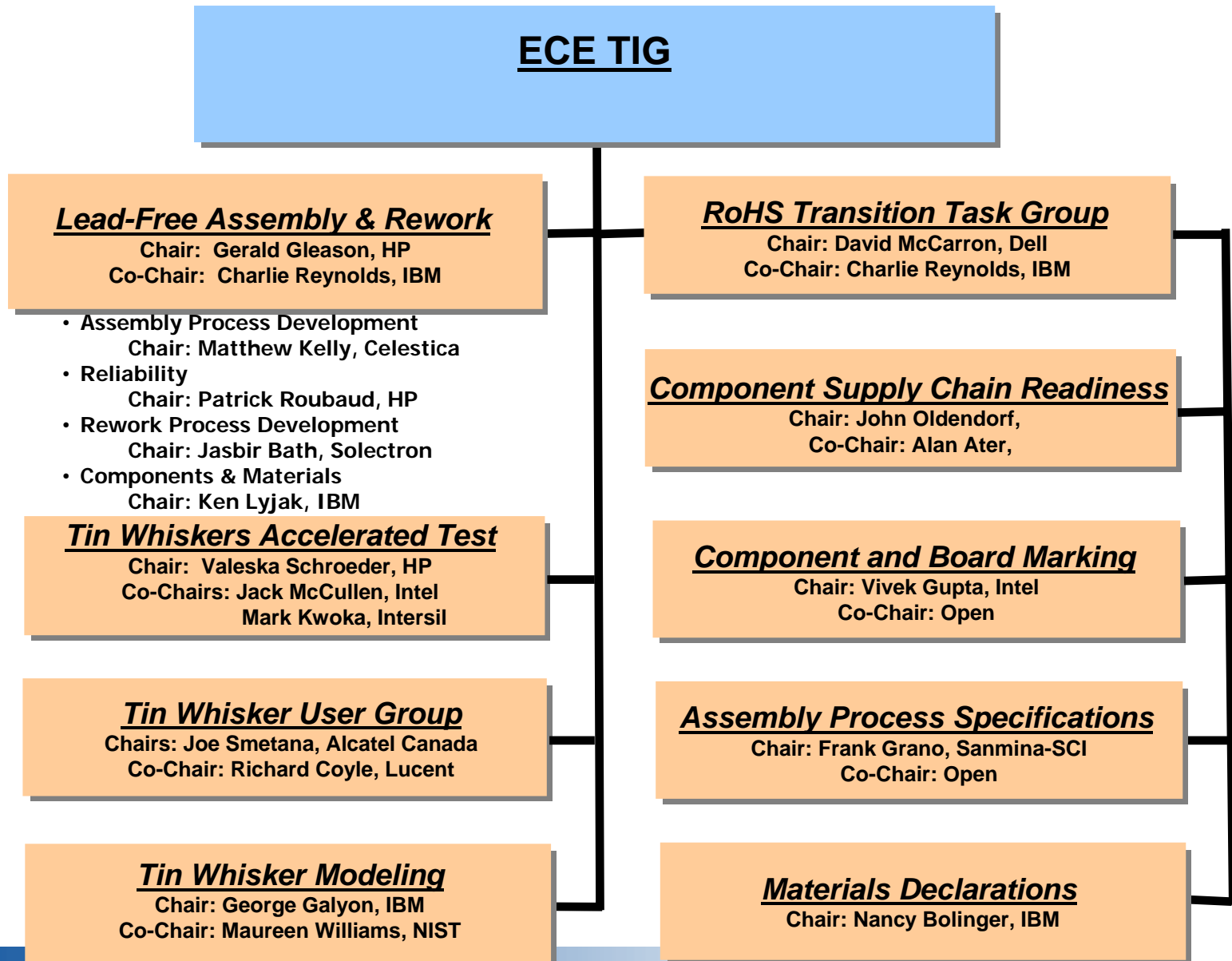
iNEMI Project Review

David Godlewski, iNEMI

New Projects:

- **Board Assembly TIG:**
 - SMT Reel Labeling Project
 - Pb-free BGAs in SnPb Assemblies Project
- **ECE TIG**
 - Pb-free Wave Soldering Assembly Process Project
- **PLIM & ECE TIG:**
 - Materials Composition Data Exchange Project
- **Optoelectronic TIG:**
 - Fiber Optic Splice Loss Measurement Project
 - Fiber Connector End-Face Inspection Project
- **Substrates TIG:**
 - Evaluation of Substrate Surface Finishes for Pb-free Assembly Project
 - Optoelectronics for Substrates Project
- **Five projects completed in 2004:**
 - Defects Per Million Opportunities
 - Fiber Optic Splice Improvement
 - Fiber Optic Signal Performance
 - Lead-Free Hybrid Assembly and Rework Project
 - High-Frequency Material Effects on HDI Formation Project





A diagram showing a blue box at the top labeled 'ECE TIG'. A vertical line descends from the bottom center of this box, then turns left to connect to the right side of an orange box below. The orange box contains text about a lead-free wave soldering assembly process and its chair/co-chair.

ECE TIG

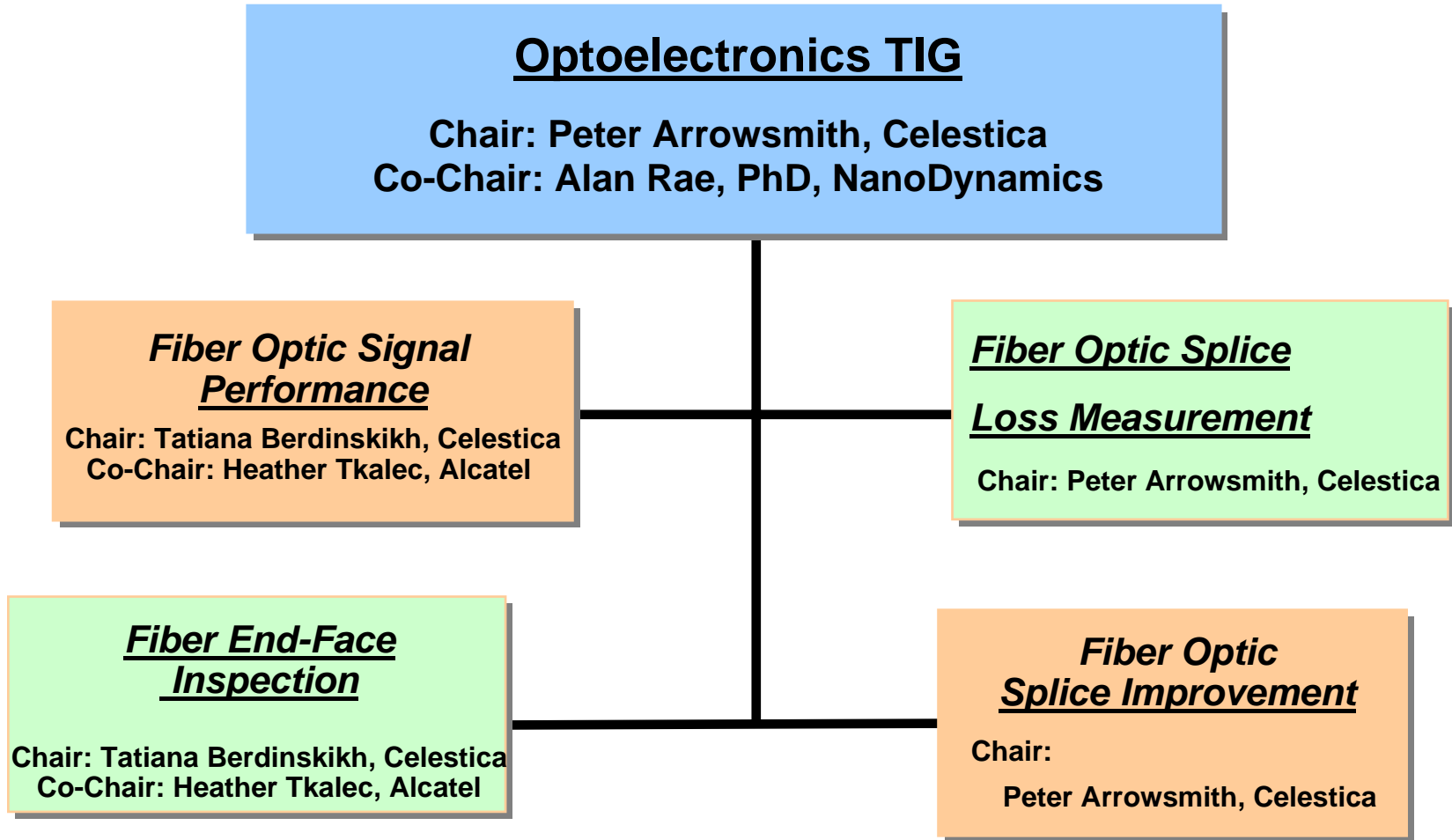
**Lead-Free Wave Soldering
Assembly Process**

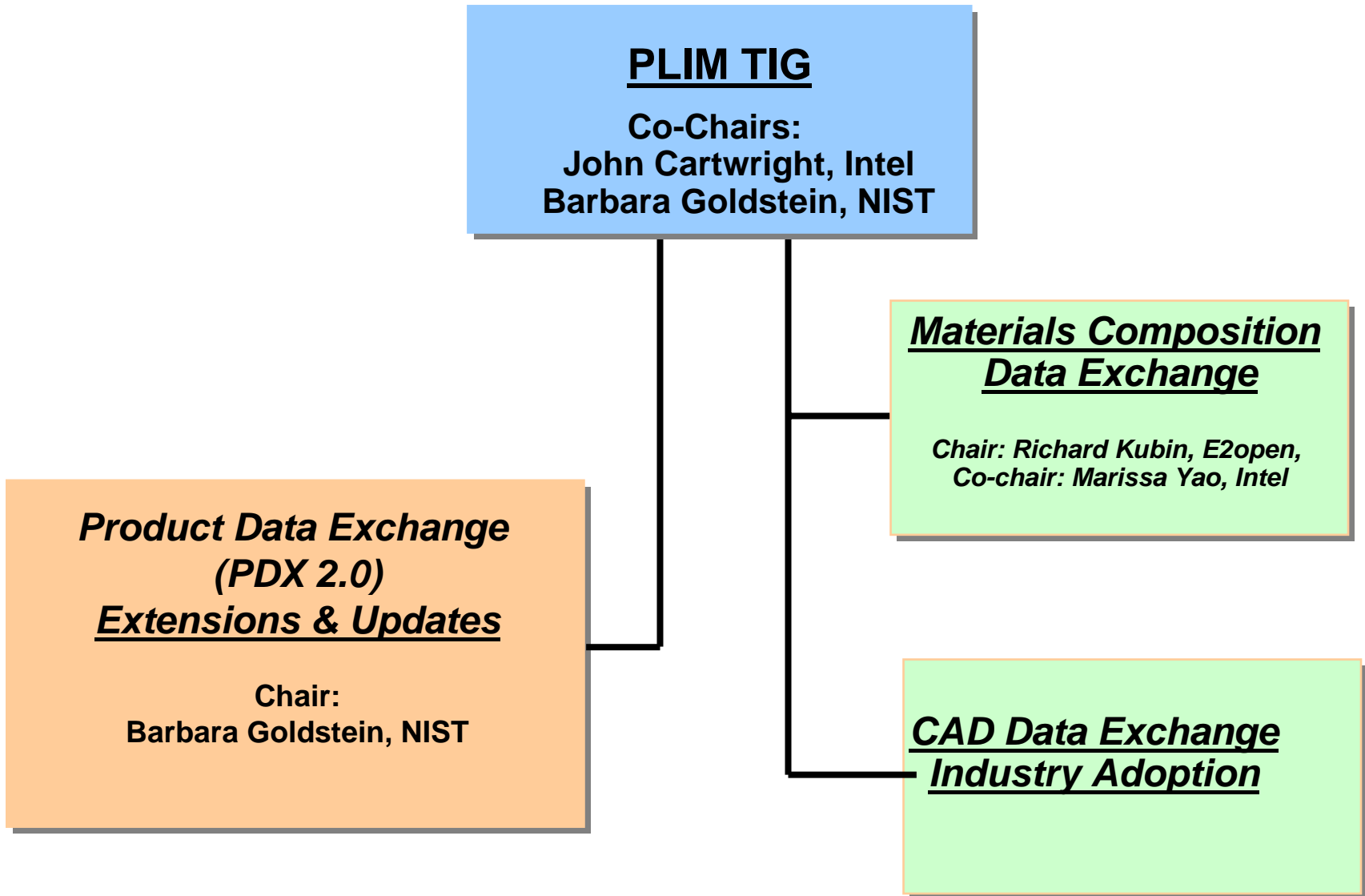
Chair: Denis Barbini, Vitronics Soltec
Co-chair Paul Wang, Sun Microsystems

Substrates TIG
Chair: Hamid Azimi, PhD, Intel

***High Frequency
Material Effects on HDI***
Chair: Hamid Azimi, PhD, Intel
Co-Chair: Jack Fisher, IPC

***Optoelectronics for
Substrates***
Chair: Jack Fisher, iNEMI/IPC







International Electronics Manufacturing Initiative

Technical Plan
Optoelectronics



Peter Arrowsmith

- **TIG Mission: To provide low cost and high yield assembly & test processes for optoelectronic systems and interconnects**
- **TIG Scope: Optical communications and related components & subsystems, as per the NEMI 2004 Roadmap**
- **Wide scope (telecom.. datacom, long haul.. FTTx, Jisso package levels 0..4) requires severe prioritization of gaps and technology integration plan**
- **Expand scope to other emerging photonics applications in next PEG, ready for 2006 Roadmap**

- **Netcom**
- **Mass Storage (excellent section on optical storage)**
- **Displays (thorough discussion of display technology)**
- **Organic Substrates**
- **Connectors**
- **Packaging**
- **Board Assembly**
- **Modeling, Simulation, and Design**

- This product emulator group spans a hardware product portfolio from consumer access to long-haul transport and addresses system capacities ranging from kilobits per second to terabits per second
- Common themes for next generation development have emerged: develop common design tools, manufacturing / test capabilities, and component specifications which can be leveraged across the communications hardware industry
- Telecommunications equipment is facing “a crisis in its ability to manage the thermal load in next-generation systems” (Netcom PEG)
- The need for flexible manufacturing is pervasive across the entire Netcom product portfolio
- The most profound paradigm shift is the change in the supply chain model, moving from completely vertically integrated companies to nearly completely horizontally integrated companies
- Two strong growth areas will be high-speed Internet access and VOIP (Voice Over IP)



International Electronics Manufacturing Initiative

**2004 Roadmap
Highlights from the
Optoelectronics
Roadmap**

*Contributed by:
Bob Pfahl*

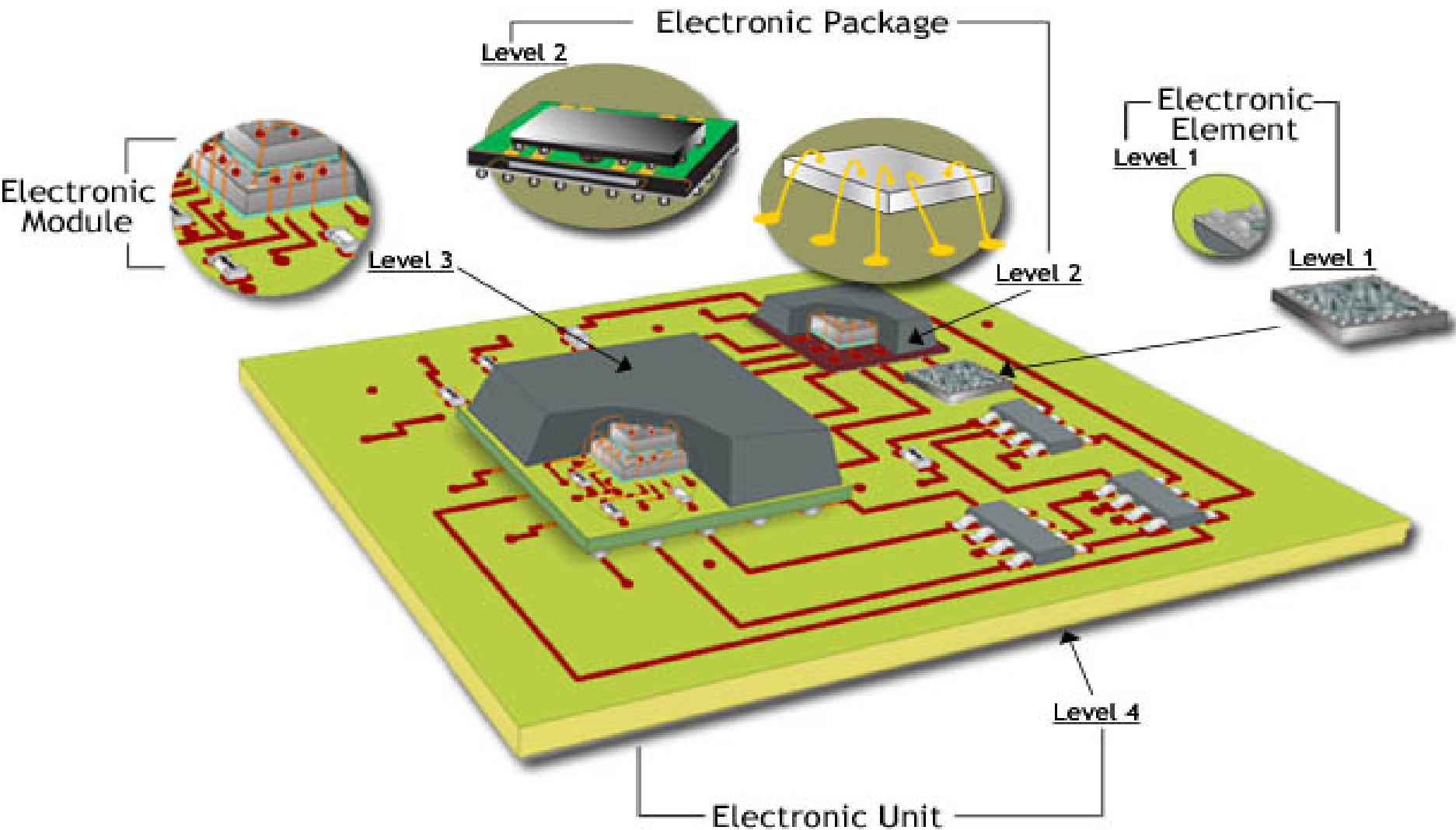
1998-2000: Growth approaching 100% per year

2001-2: Collapse of demand and subsequent revenue

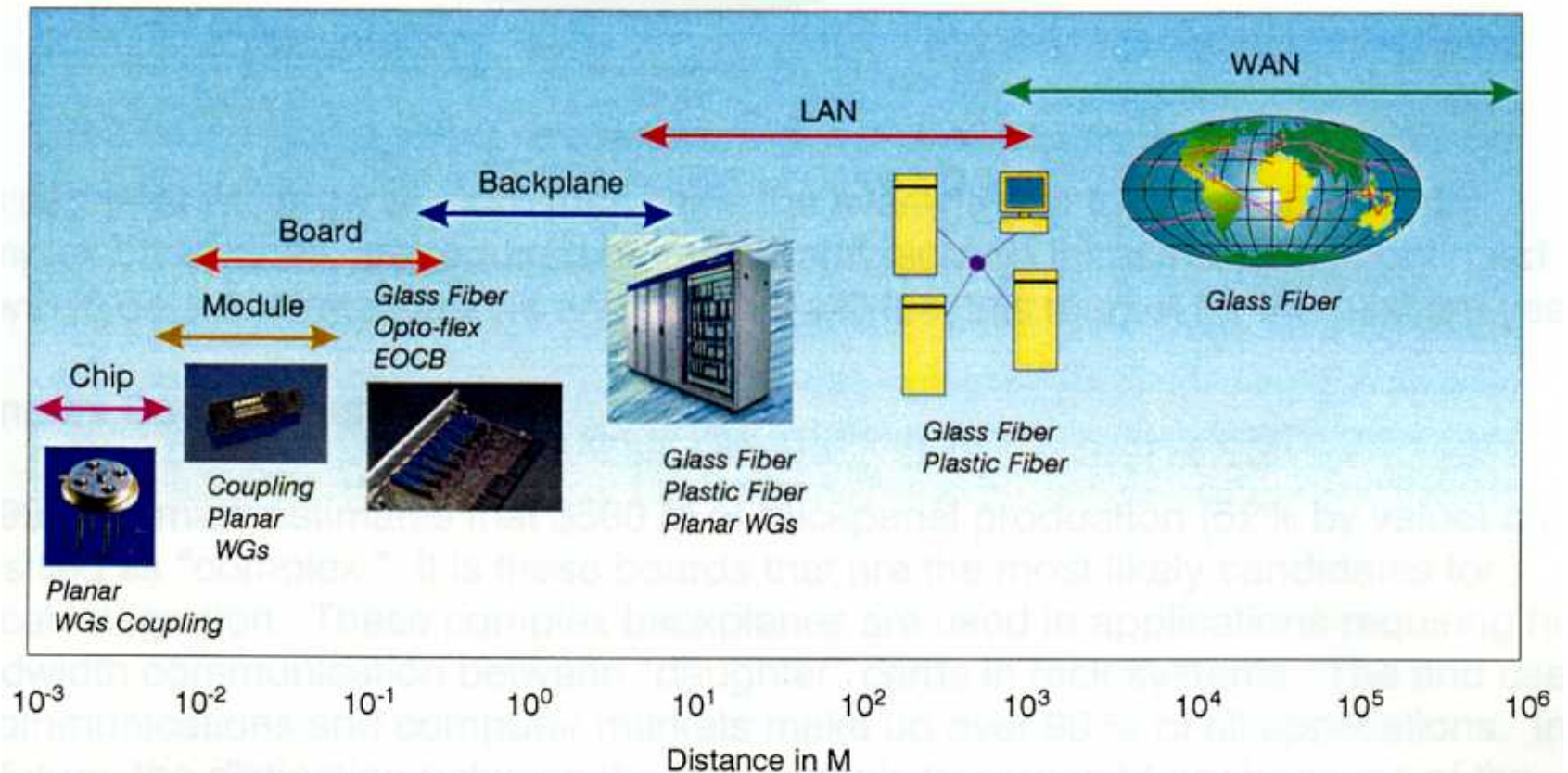
2003+: Growth resumes in specific areas

- In a situation analysis prepared by Prismark Partners LLC for NEMI it was noted that:
 - Global production of communications equipment driven primarily by internet use is expected to increase at an average rate of 6.5% per year to reach \$226B in 2008.
 - Two strong growth areas will be high speed internet and Voice Over IP (VOIP).

2004 Roadmap uses the JISSO Electronic Packaging Level Hierarchy



SCENARIO OF OPTICAL JOINING TECHNOLOGY



Source: W. Scheel EPC '99

- **The continuous development of chip technology is crucial for the advancement of optoelectronic systems.**
- **Much uncertainty surrounds the “likely” cost-performance of optical interconnect, especially for optical links within the system.** The objectives of NEMI’s “Optoelectronics Substrates Project” are to develop suitable cost-performance metrics and to compare several high-speed electrical and optical systems using cost models.
- **The move to optical interconnects within the system has been delayed by performance improvement in Cu-based methods but seems likely in three to five years.** The initial applications are likely to be in high performance switches, routers, servers, and computers. Interest continues in optical chip-to-chip connection on the system board to overcome bandwidth bottlenecks between the CPU (clock speed ~3 GHz), and the main memory or I/O bus (running at 100’s of MHz).
- **MSA (multi-source agreement) form factors for OE modules are being widely adopted.** The SFP MSA is being used for almost all optical transceiver applications below 10 Gbps. With growing availability of chipsets that can drive 10 Gbps differential links, the XFP multi-source agreement is expected to dominate at 10 Gbps.
- **A consensus has not yet emerged as to the best technology to supersede the “pigtail” era.** Integrated OECB (optical electrical circuit board) systems are a promising approach for eliminating fiber handling and complexity, but several hurdles remain to be overcome. The proposed alternatives for integrated opto-electronic systems interconnect must be evaluated as to their technical feasibility, reliability, manufacturability, and cost.

Jisso Level 1-optoelectronic element

- **Higher performance, e.g. 10 Gbps VCSELs**
- **Lower packaging complexity/cost**
- **Greater integration**

Jisso Level 2- optoelectronic package

- **Development of improved polymer materials for multimode optical transmission (optical “solder”)**
- **Development of optical chip-to-chip interconnects**
- **Development of specific optical connectors and package interfaces**
- **SMT compatible assembly processes with accuracies <10 μm**
- **New test procedures for monitoring of optical components and assessment of functionality in electro/optical systems and or complete optical systems**

Jisso Level 3-module

- **Integration of optical components to reduce packaging cost (laser and modulator, waveguides, wavelength multiplexer and demultiplexer).**

Jisso Level 2- optoelectronic package

- **Array packages are costly, with the result that array transceivers are not widely implemented. Volumes are required to reduce cost.**
- **Cost-effective packaging is required for long wavelength single mode VCSEL arrays.**

Jisso Level 3 and 4-module-unit

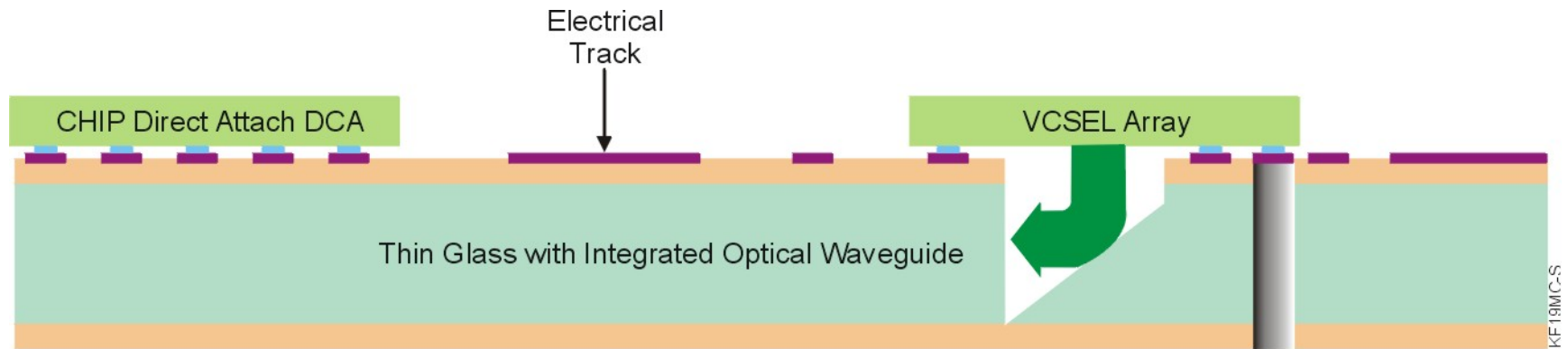
Reliability

- **The reliability of “datacom” components using lower cost innovative technology must be demonstrated to the satisfaction of users. Potential innovative examples include use of epoxy adhesives inside OE packages, non-hermetic materials, such as LCPs (liquid crystal polymers), etc.**
- **While testing to “telecom” standards, such as Telcordia GR1221 continues, the need is growing for “lite” standards, suitable for products with 10-15 years field life.**

Jisso Level 3 and 4-module-unit

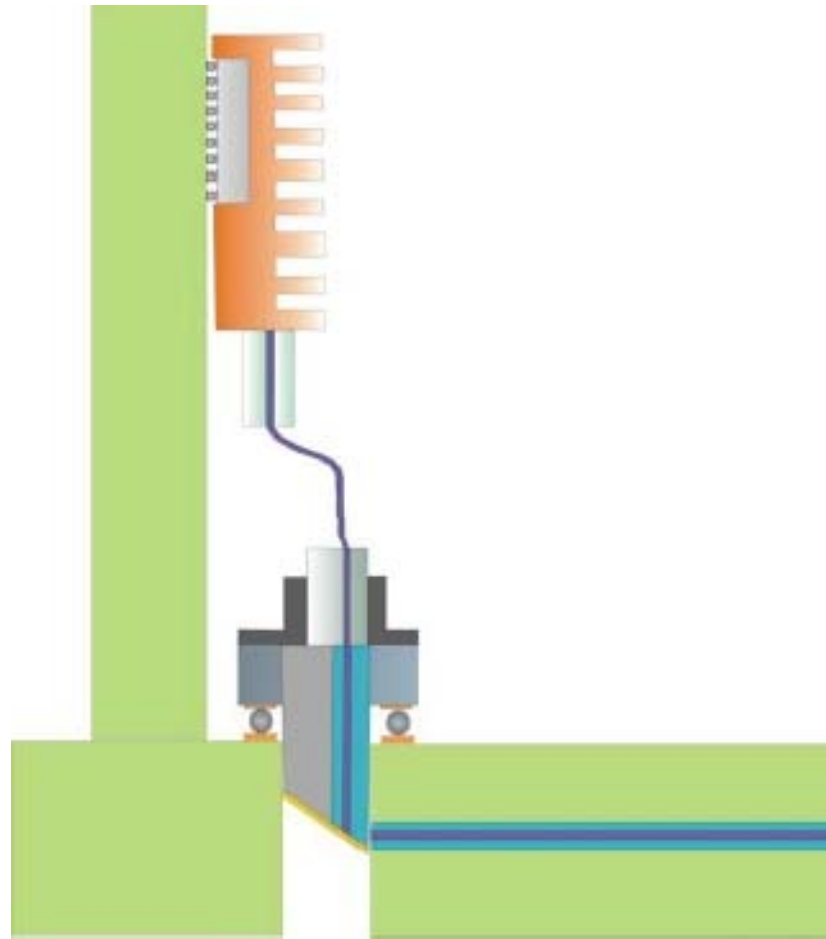
Assembly

- An effective Optical electronic circuit board (OECB) technology is needed to reduce, if not eliminate fiber handling cost and provide a “standard” assembly method that will develop higher volume and thus lower costs.
- Primary attach and rework processes are needed for Pb-free higher melting point SAC solder alloys that are compatible with OE components. These needs are similar to those for conventional Sn63 soldering in electronic assembly with the usual restrictions imposed by the relatively low temperature (<85 °C) tolerance of many OE components.



Source: PPC

Acknowledgement: BPA (2003)



•Source: Terahertz

Acknowledgement: BPA (2003)

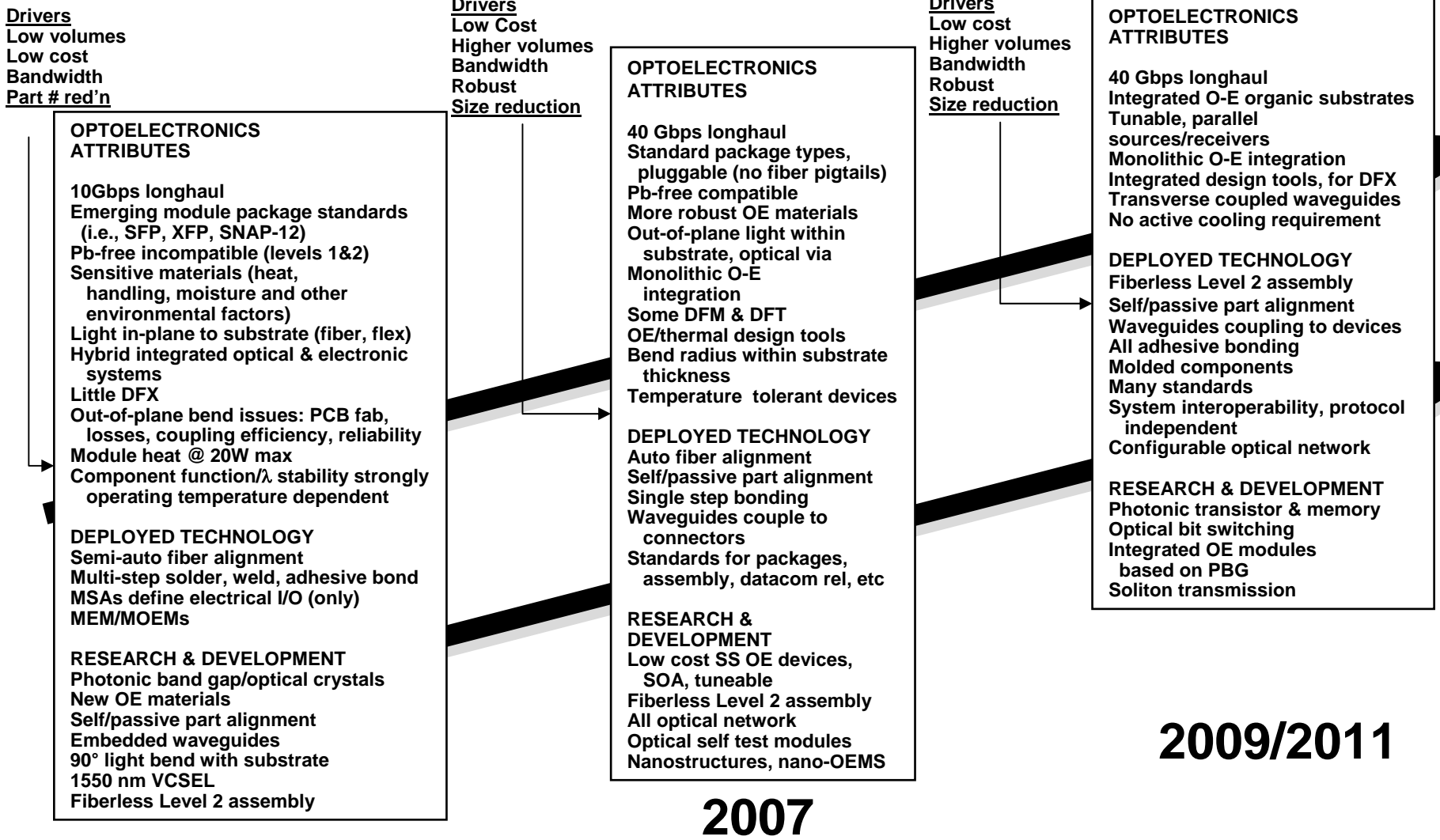
- **Develop a strategy to create a new integrated opto-electronic systems interconnect infrastructure, based on industries evaluation of alternatives for their technical feasibility, reliability, manufacturability, and cost.**
- **NEMI is willing take leadership to help enable industry standard OE interconnect(s). TIG would need to drive: bring in key players, set strategy, decide which aspect(s) to address.**

- **Other OE and OE-enabled applications have developed and now represent a larger business than communications.**
- **Future roadmaps should address these newly emerging applications and determine how the needs & gaps differ from those of netcom.**

Closing Needs through Research: A Challenge to be Strategic

- A Number of **Needs** Have appeared since the 1994 Roadmap
- We need be Innovative and look for disruptive business & technology **Solutions** to these **Needs**.
- We need to identify the research areas that would provide the technology **Solutions** to these **Needs**.
 - Materials: nanotechnology (thermal, O & E properties)
 - Devices: quantum dots, optical band-gap structures
 - Manufacturing Processes: flexibility and reconfigurability
 - Design: Rapid Modeling of Complex Systems
- Proviso: has to be better (smaller, faster, acceptable reliability..) and lower cost than the current technology

- **Primarily indicates areas for technology improvement/standardization to reduce cost and maintain (or enhance) performance & reliability**
- **Includes some applications expectations, e.g. needs and growth for last mile**
- **Not based on market factors and volume growth, e.g. 40G prediction**
- **Forecasting is difficult and usually wrong (or lucky)**
- **Highest priority areas are shown, with input from a few OEM members (Alcatel, Cisco, Nortel)**
- **Need wider industry/member feedback to prioritize projects, e.g. suppliers, equipment cos, EMS...**



	2005	2007	2009	2011	Need
Level-1: Device Technology					
VCSEL array yield & reliability, 1550 nm					D, I
Non-cooled, thermally tolerant devices					R, D
O-E integration, based on Si CMOS					R, D
Emerging SS devices, SOA, switches, OBG...					R
Level-2: Packaged component					
Design for manufacturing, test, cost (DFx)					D, I
Passive/self alignment					D, I
Hybrid O-E integration					D
Adhesives for attach & optical coupling					D, I
Pb-free compatibility					I
Waveguide-device coupling					D
Levels 3 & 4: module, sub-system					
Compatible electrical & optical assembly					D, I
Low temp, Pb-free solder attach					I
Fiber assembly (connector, fiber handling)					D, I
Embedded waveguides					D, I
Waveguide-connector coupling (in-plane)					D, I
Optical via (out-of-plane coupling)					D, I
Standards					
Packaging, assembly & test, e.g. IPC 0040					I
Interoperability at system/network level					D, I
Reliability for datacom/last mile applications					D, I
Test: critical parameters/reduced capex					I
Industry stnd optical interconnects					D, I





International Electronics Manufacturing Initiative

Optoelectronics TIG Plan

Completed in 2004

- Optical Fiber Splice Improvement (Ldrs. P.A, Rob Suurmann)
- Optical Connector Signal Performance (Ldrs. Tatiana Berdinskikh, Heather Tkalec)
- MOU with TIA

In-progress

- Fiber Connector End-Face Inspection Requirements (Oct '04)
 - Connector Cleanliness Spec: IPC-8497-01, “Cleaning Methods and Contamination Assessment for Optical Assembly”, in review
 - Finalize pass/rejection inspection criteria, in collaboration with IEC
 - Development cleanliness specification for receptacle
- Optical Substrates: cost model comparison of electrical vs. optical backplanes for high performance systems (Ldr. Jack Fisher)
- Fiber Splice Loss Measurement Specification, with the TIA

From the 2002 & 2004 OE roadmaps, discussion with members, sessions at APEX, OIDA workshops...

- Splicer loss estimator accuracy metric
- Automated inspection of connectors
- Near hermetic package sealing
- Datacom “Lite” reliability standard
- New approaches to lower cost assembly & packaging
- Industry standard optical interconnect
- ROHS compliance, Pb-free assembly (see 2004 gaps)
- Thermal (see 2004 gaps)
- Non-telecom applications, e.g. bio/medical photonics
- Others?

Project objectives, statement of work are defined by the team
(list is not closed, or in any priority)

- We have more suggested projects than available resource
- Take on 1 or 2 new projects, possibly more if short term/quick wins
- Ensure projects benefit the participants, as well as the wider industry
- Looking for input & feedback
- Survey members, to rank projects based on:
 - expected benefit
 - likelihood of success
 - level of enthusiasm
 - has similar been done previously (y/n)
 - other criteria?
- Prioritize to top 3-5 projects
- Calls for project participation at APEX and OFC

APEX, Anaheim, Feb 22-24, 2005

- Optical substrates project meeting: Weds, Feb 23, 1-3 pm
- OE TIG open meeting, new projects call for participation (TBC)

OFC/NFOEC, Anaheim, March 6-11, 2005

- OE TIG open meeting: Monday, March 7
 - Connector cleanliness acceptance project meeting, 9:00-12:00
 - Splice loss measurement methods project meeting, 1:00-3:00
 - 2004 Roadmap gap analysis, new projects call for participation, 3:00-5:00 pm
- Follow-up conference call, March/April

- **The optoelectronics industry is down but not out, existing infrastructure will run out of bandwidth**
- **Growth & higher volumes in Access/Metro/FTTx**
- **Optoelectronic assembly will continue to be a key skill required of OEM and EMS manufacturers.**
- **Fiber interconnect technologies will be continue to be used, in modules (e.g. EDFA), box-to-box and longer reach**
- **Embedded waveguides will be used because they are compatible with automated assembly, but some significant issues need to be addressed**
- **Lack of standardization is key inhibitor**
- **Looking for Member input to OE roadmap, gap analysis & project selection**

Chair: Peter Arrowsmith, parrowsm@celestica.com

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Tel (717) 651-0522

Comments welcome!

Thank You