



International Electronics Manufacturing Initiative

**Optoelectronics TIG
OFC/NFOEC Conference**



Monday, March 7, 2005
Anaheim Marriott

9:00-12:00 am PST

**iNEMI Fiber Connector End-Face Inspection Project:
Tatiana Berdinskikh, Celestica**

1:00-2:00 pm PST

**iNEMI Fiber Optic Splice Loss Measurement Project:
Peter Arrowsmith, Celestica**

2:00-3:00 pm PST

**I NEMI Optoelectronics for Substrates Project:
Peter Arrowsmith, Celestica**

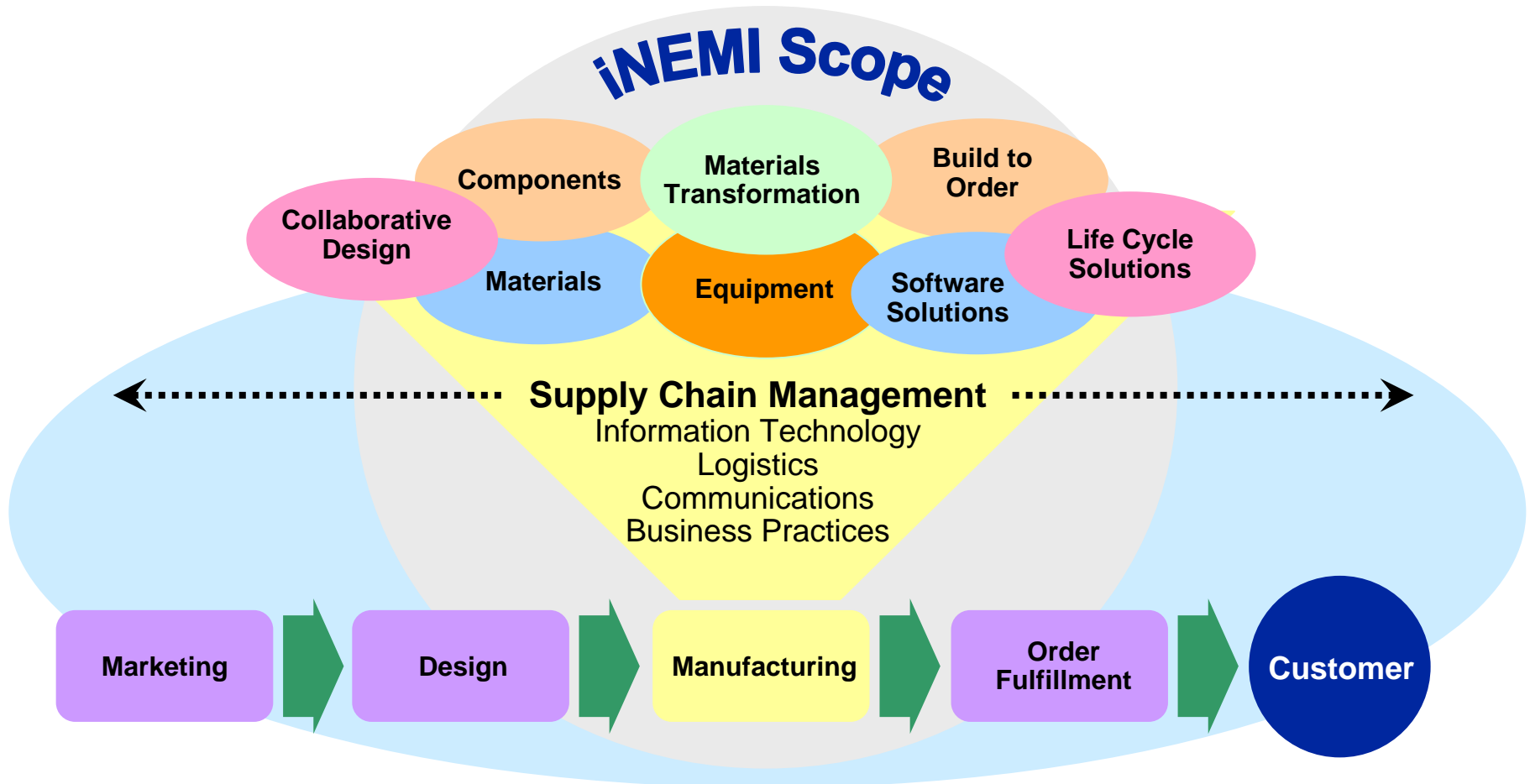
3:00-5:00 pm PST

**iNEMI Optoelectronic TIG Gap Meeting:
Peter Arrowsmith, Celestica**

iNEMI Process

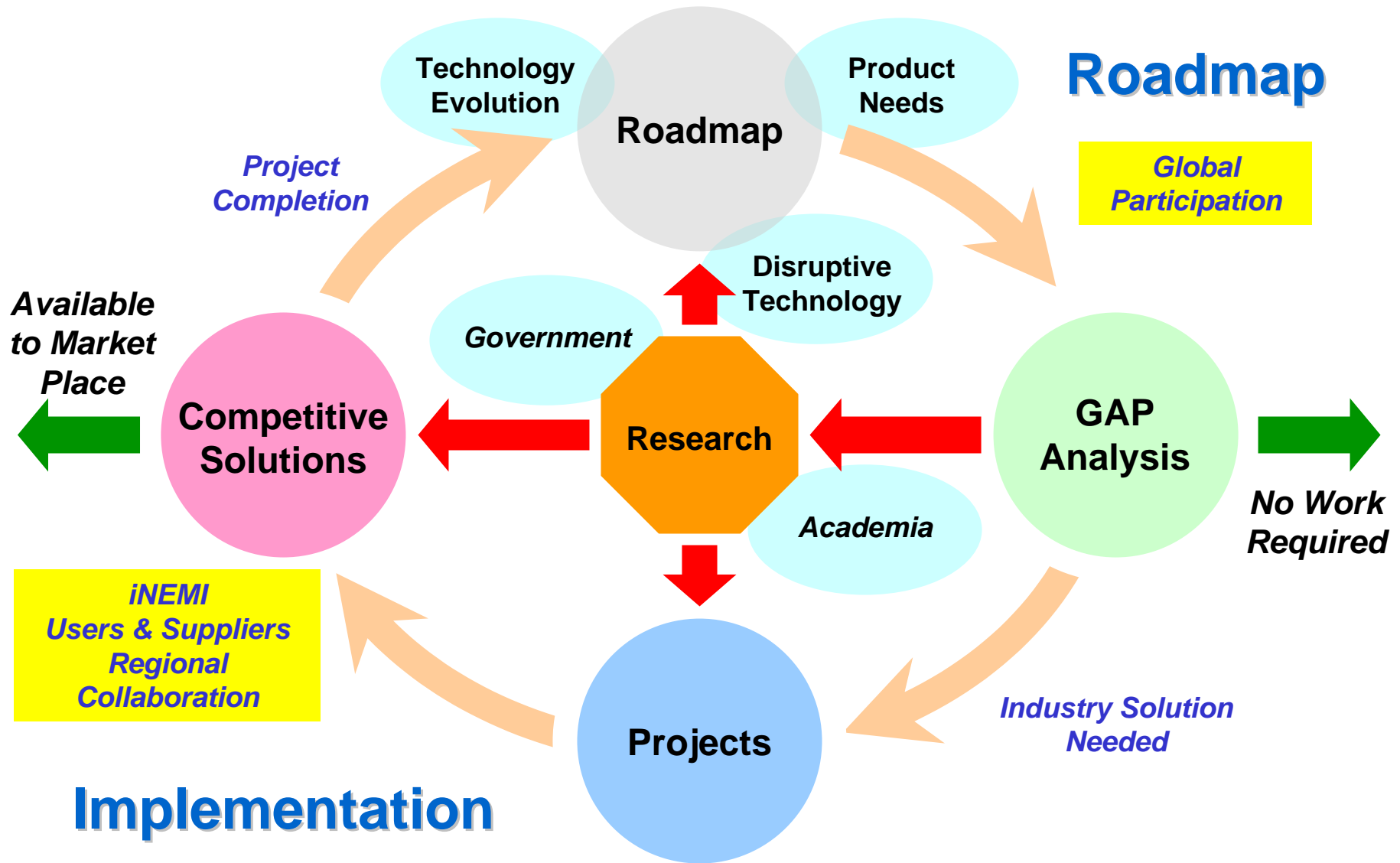
David Godlewski, iNEMI

*Assure Leadership of the Global Electronics Manufacturing Supply Chain
for the benefit of members and the industry*



Leverage the combined power of member companies to provide industry leadership

- **iNEMI roadmaps the global needs of the electronics industry**
 - **- Evolution of existing technologies**
 - **- Prediction of emerging/innovative technologies**
- **iNEMI identifies gaps (both business & technical) in the electronics infrastructure**
- **iNEMI stimulates research/innovation to fill gaps**
- **iNEMI establishes implementation projects to eliminate gaps**
- **iNEMI stimulates worldwide standards to speed the introduction of new technology & business practices**
- **iNEMI works with other organizations to ensure that government policy recommendations are aligned with our mission.**



- **Distribute Schedule and Template to TIG Chairs / TC 2/1/05**
- **TIG Chairs Hold Gap Analysis Meetings as Follows:**
 - **iNEMI Board Assembly and Substrates TIG Meeting @ APEX 2/22/05**
 - **iNEMI SIP TIG Meeting - NEW @ APEX 2/23/05**
 - **iNEMI Environmental TIG Meeting @ APEX 2/24/05, @ ISEE 5/16-19/05**
 - **iNEMI PLIM TIG Meeting @ Intel 3/1-3/05**
 - **iNEMI OPTO TIG Meeting @ OFC 3/6-10/05**
- **TIG Chairs / TC Discuss Gaps / Technical Plan at APEX 2/25/05**
- **Research Committee Telecons 3/3/05, 4/7/05**
- **Drafts from TIGs and RC due 6/17/05**
- **T.C. Face to Face on Technical Plan / Research Priorities in Herndon 6/23-24/05**
- **Release 2005 Research Priorities @ BOD/EI Meetings in Herndon 9/14-15/05**
- **Release 2005 Technical Plan to Members @ SMTAI 9/25-29/05**

- **Outline for each TIG's Technical Plan input**
 - **Introduction**
 - **Gap Analysis and Five-year plan**
 - **What has changed**
 - **TIG Plan**
 - **Projects/programs to focus on short term -prioritize**
 - **Identify areas where research is needed -prioritize**
 - **Summary**

Drivers

Low volumes
Low cost
Bandwidth
Part # red'n

OPTOELECTRONICS ATTRIBUTES

10Gbps longhaul
Emerging module package standards (i.e., SFP, XFP, SNAP-12)
Pb-free incompatible (levels 1&2)
Sensitive materials (heat, handling, moisture and other environmental factors)
Light in-plane to substrate (fiber, flex)
Hybrid integrated optical & electronic systems
Little DFX
Out-of-plane bend issues: PCB fab, losses, coupling efficiency, reliability
Module heat @ 20W max
Component function/ λ stability strongly operating temperature dependent

DEPLOYED TECHNOLOGY

Semi-auto fiber alignment
Multi-step solder, weld, adhesive bond
MSAs define electrical I/O (only)
MEM/MOEMs

RESEARCH & DEVELOPMENT

Photonic band gap/optical crystals
New OE materials
Self/passive part alignment
Embedded waveguides
90° light bend with substrate
1550 nm VCSEL
Fiberless Level 2 assembly

2005

Drivers

Low Cost
Higher volumes
Bandwidth
Robust
Size reduction

OPTOELECTRONICS ATTRIBUTES

40 Gbps longhaul
Standard package types, pluggable (no fiber pigtailed)
Pb-free compatible
More robust OE materials
Out-of-plane light within substrate, optical via
Monolithic O-E integration
Some DFM & DFT
OE/thermal design tools
Bend radius within substrate thickness
Temperature tolerant devices

DEPLOYED TECHNOLOGY

Auto fiber alignment
Self/passive part alignment
Single step bonding
Waveguides couple to connectors
Standards for packages, assembly, datacom rel, etc

RESEARCH & DEVELOPMENT

Low cost SS OE devices, SOA, tuneable
Fiberless Level 2 assembly
All optical network
Optical self test modules
Nanostructures, nano-OEMs

2007

Drivers

Low cost
Higher volumes
Bandwidth
Robust
Size reduction

OPTOELECTRONICS ATTRIBUTES

40 Gbps longhaul
Integrated O-E organic substrates
Tunable, parallel sources/receivers
Monolithic O-E integration
Integrated design tools, for DFX
Transverse coupled waveguides
No active cooling requirement

DEPLOYED TECHNOLOGY

Fiberless Level 2 assembly
Self/passive part alignment
Waveguides coupling to devices
All adhesive bonding
Molded components
Many standards
System interoperability, protocol independent
Configurable optical network

RESEARCH & DEVELOPMENT

Photonic transistor & memory
Optical bit switching
Integrated OE modules based on PBG
Soliton transmission

2009/2011

	2005	2007	2009	2011	Need
Level-1: Device Technology					
VCSEL array yield & reliability, 1550 nm					D, I
Non-cooled, thermally tolerant devices					R, D
O-E integration, based on Si CMOS					R, D
Emerging SS devices, SOA, switches, OBG...					R
Level-2: Packaged component					
Design for manufacturing, test, cost (DFx)					D, I
Passive/self alignment					D, I
Hybrid O-E integration					D
Adhesives for attach & optical coupling					D, I
Pb-free compatibility					I
Waveguide-device coupling					D
Levels 3 & 4: module, sub-system					
Compatible electrical & optical assembly					D, I
Low temp, Pb-free solder attach					I
Fiber assembly (connector, fiber handling)					D, I
Embedded waveguides					D, I
Waveguide-connector coupling (in-plane)					D, I
Optical via (out-of-plane coupling)					D, I
Standards					
Packaging, assembly & test, e.g. IPC 0040					I
Interoperability at system/network level					D, I
Reliability for datacom/last mile applications					D, I
Test: critical parameters/reduced capex					I
Industry stnd optical interconnects					D, I

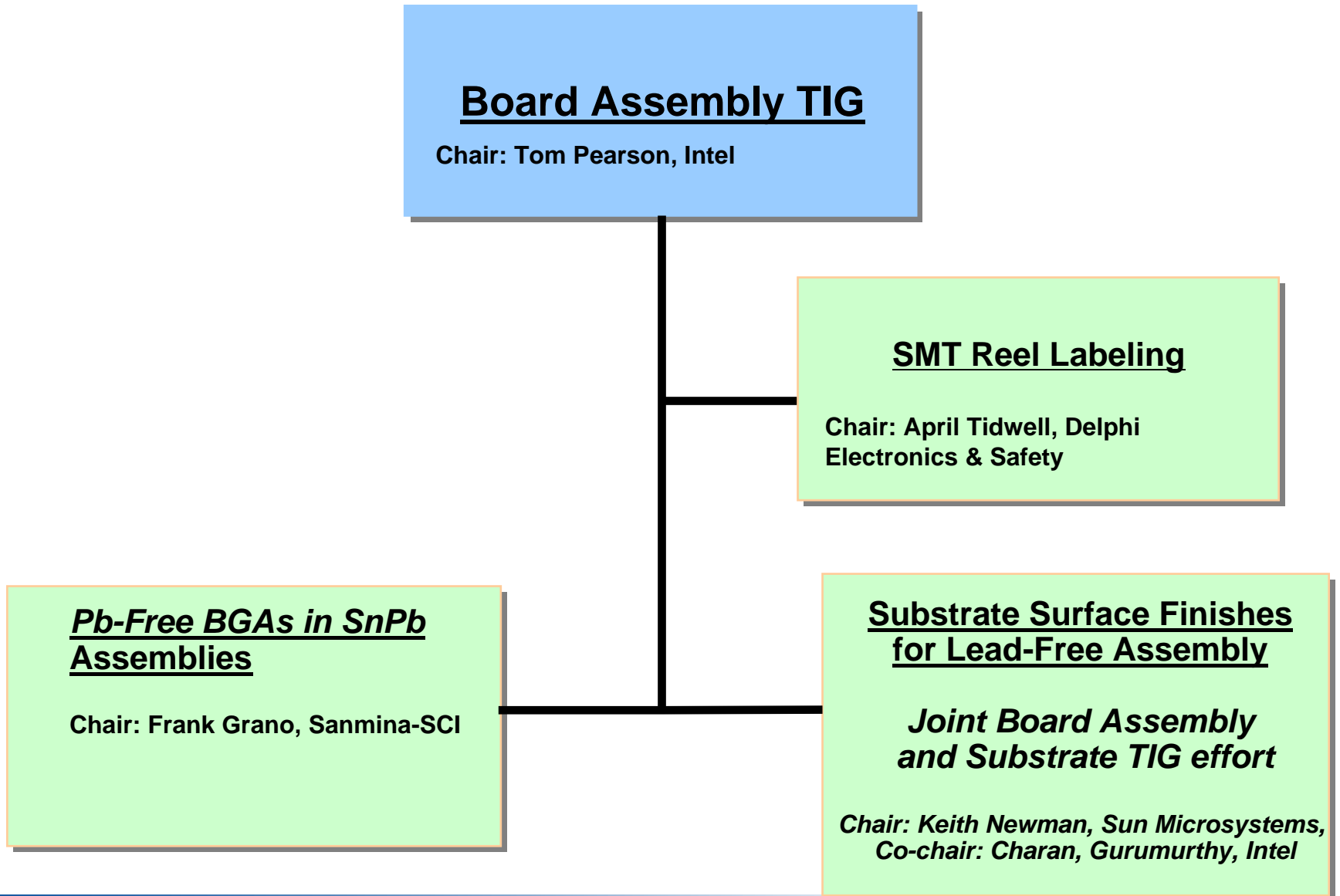


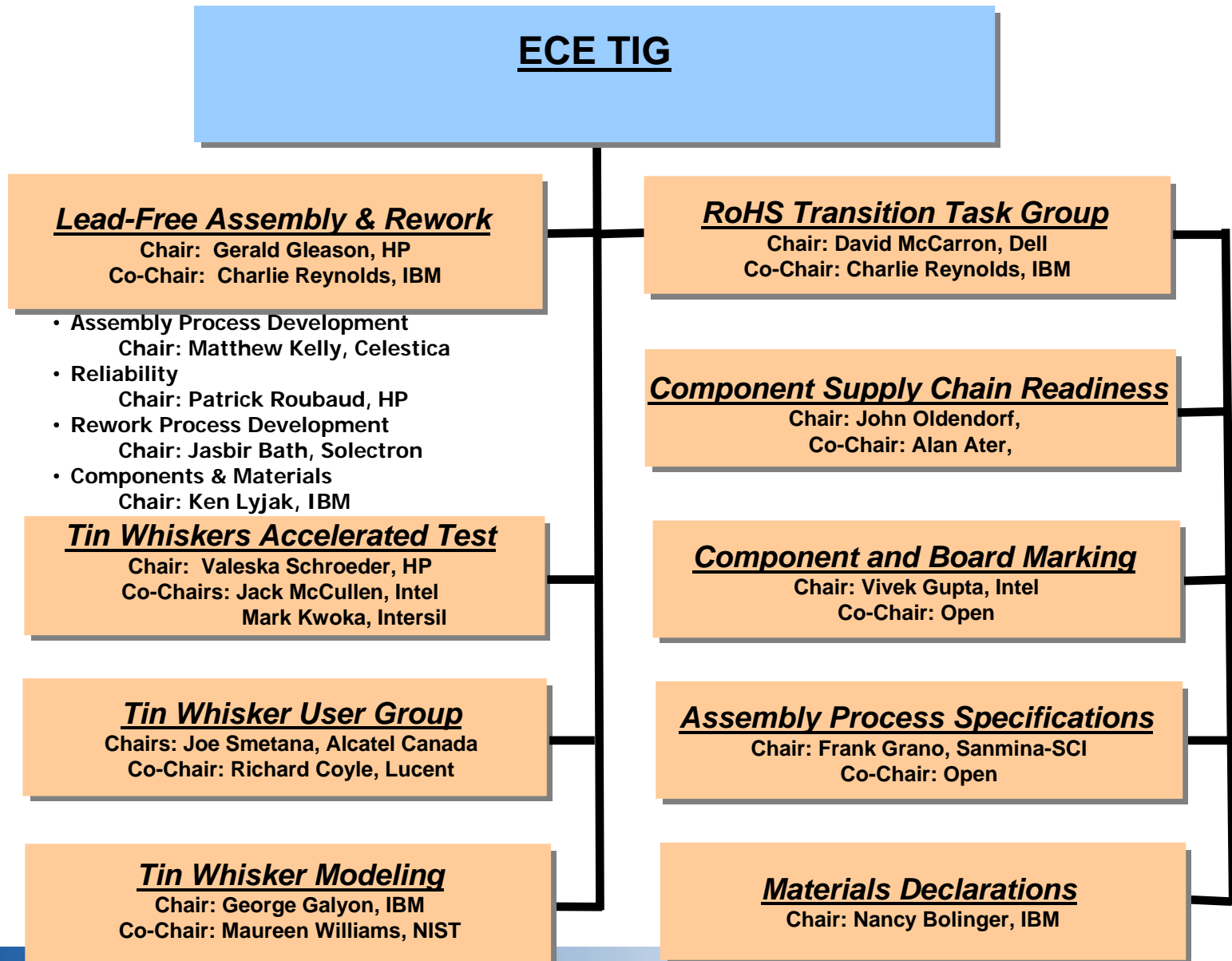
iNEMI Project Review

David Godlewski, iNEMI

New Projects:

- **Board Assembly TIG:**
 - SMT Reel Labeling Project
 - Pb-free BGAs in SnPb Assemblies Project
- **ECE TIG**
 - Pb-free Wave Soldering Assembly Process Project
- **PLIM & ECE TIG:**
 - Materials Composition Data Exchange Project
- **Optoelectronic TIG:**
 - Fiber Optic Splice Loss Measurement Project
 - Fiber Connector End-Face Inspection Project
- **Substrates TIG:**
 - Evaluation of Substrate Surface Finishes for Pb-free Assembly Project
 - Optoelectronics for Substrates Project
- **Five projects completed in 2004:**
 - Defects Per Million Opportunities
 - Fiber Optic Splice Improvement
 - Fiber Optic Signal Performance
 - Lead-Free Hybrid Assembly and Rework Project
 - High-Frequency Material Effects on HDI Formation Project







ECE TIG

The diagram shows a hierarchical structure. At the top is a light blue rectangular box containing the text "ECE TIG". A vertical line descends from the bottom center of this box, then turns 90 degrees to the left, and then turns 90 degrees downwards again to connect to the top right corner of an orange rectangular box below it.

**Lead-Free Wave Soldering
Assembly Process**

Chair: Denis Barbini, Vitronics Soltec
Co-chair Paul Wang, Sun Microsystems

Substrates TIG
Chair: Hamid Azimi, PhD, Intel

***High Frequency
Material Effects on HDI***
Chair: Hamid Azimi, PhD, Intel
Co-Chair: Jack Fisher, IPC

***Optoelectronics for
Substrates***
Chair: Jack Fisher, iNEMI/IPC

