



INEMI[®]

International Electronics Manufacturing Initiative

**2009
International
Test Conference
Update**

*Austin, Texas
November 5, 2009*

Advancing manufacturing technology

IEEE Board Test Workshop Update

- **Agenda**
 - **iNEMI Test TIG Update**
 - **2010 Test Projects**

Board & Systems Test TIG

- **Chair: Rosa Reinosa (HP)**
- **Co-Chair: James Grealish (Intel)**

Test

- **To improve the effectiveness of the test process and the quality of electronic products in a global manufacturing environment**
- **Scope includes test technology and process improvement for boards and systems (e.g. automated inspection, electrical test, boundary scan, functional test, system test)**

Test TIG Projects 2010

TEST TIG

Chair: Rosa Reinoso

Co-Chair: JJ Grealish

Board Flexure Initiative

Chair: Elizabeth Benedetto (HP)
Co-Chair: Alan McAllister (Intel)

Boundary Scan (Phase II)

Chair: Phil Geiger (Dell)
Co-Chair: Steve Butkovich (Cisco)

BIST

Chair: Zoe Conroy (Cisco)
Co-Chair: Yang Yang (Huawei)



Summary of 2009 activities

Accomplishments

- **Completion of iNEMI 5 Year Test Technology Roadmap to be published by iNEMI. Special thanks to and recognition of participants:**
 - Huawei (Victor Chen); Cisco (Steve Butkovitch); Dell (Phil Geiger); Agilent (Ken Parker, Mark Lau); HP (Skip Meyers, Rosa Reinoso); TRI (Floyd Conner); Boston Scientific (Max Cortner); Asset (David Bonnet); Jabil (David Anthus, Mark Dickson); Delphi (Mike Reagin); Plexus (Tim Kruse); Intel (James Grealish); EMC (Dick Miller, Mark Bisceglia, Jeff Moore); iNEMI Asia (Haley Fu); Teradyne (Mike Smith); Delphi (Aik Peng Ng)
- **Completed gap analysis**
- **Identified and reviewed proposals for 2010 projects**
- **Completed Functional Test Coverage project**



Board Flexure Initiative Project

2009 Update

- **New Spherical Bend Test Method Standard (IPC/JEDEC 9707) is being completed**
- **Gathering feedback from JEDEC and IPC 6-10d committees**
- **Authorized to ballot through JEDEC**
- **Proposal will go for ballot in IPC & JEDEC in Nov 2009**

Phase II

- **Starting in 2010**
- **Goal: Update IPC 9702 (Monotonic Bend Test Method) and IPC 9704 (Strain Gauge Standard)**
- **ITC working session planned from 11:30-12:30, hosted by Rosa Reinoso (Chair) & Alan McAllister (Co-chair)**



Boundary Scan Project

2009 Update

- **Industry Survey (completed)**
- **Survey analysis (completed)**
- **Webinars hosted by iNEMI on 10/13 (completed)**
- **ITC paper (completed and presented)**

- **More in depth update at 10:45-11:15 by Phil Geiger (Chair)**

Phase II - TBD

- **Members only ITC working session planned from 1:30-3:00pm, hosted by Phil Geiger (Chair) & Steve Butkovich (Co-chair)**



Functional Test Coverage Project

2009 Update

- **Project has been completed**
- **Webinar hosted by iNEMI on 8/12/09**
- **Results will be made available to the industry**
- **Completed in 2009**

2010 TBD

- **Status & next steps discussion 11:15-11:30 by Tony Taylor (Chair)**



BIST Project

New in 2010

- Project approved by iNEMI tech council
- Statement of Work (SOW) complete
- Project Statement complete
- Currently in open enrollment until 11/11
- Goal Summary
 - to develop and promote the adoption of chip BIST at the board/system level
- Working session hosted this AM (8:15-10:15) by Zoe Conroy (Chair) and Yang Yang (C-Chair)

Potential Project Steps:

- Survey (current state of BIST in the industry)
- BIST as an ICT alternative Investigation
- Promotion of existing component BIST reused in board/system level
- Development of Related Standards
- New BIST Board Level Standard Proposal
- White Paper

iNEMI Test Cost Model (Phase II)

- **Project's SOW was presented to the iNEMI Technical Committee for review and approval, during the Committee's October 9, 2009 meeting**
- **The project was not approved by the Technical Committee as currently defined**
- **Test Cost Model (Phase II) project formation group is working toward redefining its SOW by conducting an industry survey as to better define requirements of an updated Test Cost Model**



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