



INEMI[®]

International Electronics Manufacturing Initiative

BI ST Project

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ITC, Austin, TX
Nov 5th, 2009*

Advancing manufacturing technology

BIST Project - Scope of Work and Phase 1

This project's focus is on “Chip” Built in Self Test (BIST) study and its promotion for board and system-level applications.

Purpose of Project

- Presently, there are no Standard Chip level interfaces or algorithms for Built in Self Test (BIST), which limits the introduction of BIST at board level test. Most “chip” level BISTs are designed to aid IC manufacturing; these algorithms are often not suitable or available to run at the board level.
- The goal of this project is to develop and promote the adoption of chip BIST at the board/system level, encourage IC vendors to provide standard chip BIST interfaces and algorithms and encourage ATE/Instrument providers to develop products based existing related standards for BIST design, for example, an IEEE 1500/P1687a globalized Test Cost Model useful throughout the industry.



BIST Project - Scope of Work and Phase 1

The project is divided into 3 phases:

Phase 1

- This phase is being presented as a “standalone project” and will be used as the baseline in defining the second and third phases.
 - This phase is a survey of the industry on current BIST capabilities and future requirements.
 - The goal of this phase is to get feedback from the industry on board level BIST that will assist in fine tuning the scope of Phase 2.

BIST Project Phase 2

Phase 2:

The current vision is that the second phase will be comprised of the following 3 parts:

1. Identification of Chip BIST technologies, which can be migrated to run at board/system-level test.
2. Investigation of BIST tests that enable PCBA testing without or minimal use of fixture/ICT (In Circuit Test) system (currently the typical manufacturing test approach) to lower cost of test and enhance test coverage for high speed interconnects.
3. Promotion of the development of existing related standards for BIST design.

BIST Project – Phase 2

Some examples of BIST techniques are list below :

BIST Technique	Fault coverage	Study Directions
Internal MBIST	IC internal defects: stuck at fault, dynamic fault	Algorithms
External MBIST	External memory Defects: DDR, RLDRAM, FCRAM, TCAM, SSRAM stuck at fault, dynamic fault. Interconnect defects: process defect PCOLA/SOQ and SSN	Algorithms , Diagnosis
High speed IO BIST	Interconnect defect - SI /noise defects.	Algorithms , interconnect between different vendors ICs, interconnect over backplanes
Logic BIST	IC internal defects	Applications , resolve NTFs issues
Frame BIST	IC internal defects, process defect, and system-level malfunctions	Instruments - - Protocol based pattern generation, Algorithms, diagnosis
On chip instruments	IC internal defects, board and interconnect defects. Process defects	Algorithms , interconnect between different vendors ICs, interconnect over backplanes, voltage and temperature measure
Analog and mixed signal BIST	IC internal defects, and interconnect defects	Algorithms , Diagnosis

BIST Project – Phase 3

Phase 3

- The third phase is the development of guidelines and recommendations for a new standard for PCBAs to run BIST tests, and the transfer of the implementation to the appropriate standards body
- Phase 3 will take place if the outcome of Phase 2 recommends it

BIST Project Current Team and Companies

Zoe Conroy (Chair)	Cisco
Yang Yang (Co chair)	Huawei
Qiang Chen	Huawei
Zihua Jiang	Alcatel Bell
Jun Balangue	Agilent
Hui Li	Agilent
Bill Eklow	Cisco
Rosa Reinoso	HP
TJ Choo	HP
James Grealish	Intel
tony Taylor	Intel
David Godlewski	iNEMI
Jim Arnold	iNEMI
Haley Fu	iNEMI

Prospective Participants

- **Participant companies should also include:**
 - Chip design companies (memory, microprocessor, ASIC, datacom)
 - TI, Micron, Marvell, Broadcom, IBM, LSI, Maxim, Micrel, Vitesse (ASIC vendors/manufacturers)
- **Board and system design companies (PC, networking, test)**
 - Dell, Delphi, Lenovo, Quanta. Sun Microsystems, etc
- **EMS, CMs, ATE Suppliers, ICT Fixture suppliers,**
 - Celestica, Flextronics Foxconn, Plexus, Sanmina-SCI, Teradyne, Stats ChipPac, Jabil, Verigy, ECT
- **Boundary scan suppliers**
 - Asset, JTAG, Intellitech
- **Participating companies need to be iNEMI members.**



Schedule with Milestones:

Task		Months						
		1	2	3	4	5	6	7
	<u>Phase 1 Survey</u>							
1.0	Plan the survey							
1.1	Define questionnaire (questions)							
1.2	Define survey hosting and data analysis method							
1.3	Prepare survey recipient list							
2.0	Prepare logistics of survey (post/host survey, notify recipients)							
3.0	Conduct survey / Distribute Questionnaire							
4.0	Collect and analyze data							
5.0	Review/Share survey data with project members							
6.0	Identify the key areas for further discussion							
6.1	Identify data to support scope for items in Phase 2							
7.0	Prepare report of the survey result							
7.1	Internal report for iNEMI Project team							
7.2	Summary report for iNEMI membership							
8.0	Phase 2 preparation, project plan, SOW (output from Phase 1)							

Phase 1 – Proposed Survey Background

IC design and test	Bd/system design & test
Who designs the BIST in your Co? Inside or IP from outside?	Do you want to use BIST at the system? Which test steps?
Do you give out BIST info to customers? If no, why?	If no, What is stopping you getting there?
Is the BIST designed to be run at the PCBA level? If yes, do you use it in house at the board level?	What coverage do you expect? What coverage would you like?
If no, what stops the BIST being run at the PCBA level?	What is stopping you getting the coverage you need?
What stops you designing the BIST to be run at the PCBA?	How critical is BIST for future coverage and fault isolation?
	Do you seeing it replacing In Circuit Testing for assembly defects?

What is stopping us running BIST at the board level?

- Not designed to run there – so what does it take to do that?
- Suppliers do not want to give customers data/info on how to use the BIST test – why not?
- Designers never thought of running it there, so did not design it as such

What will it take for comp suppliers to design it to run at the board level?

- Si space, time overhead, package pins, opening up IP?



Sample of Proposed Survey Questions

1. Does your company use BIST technique in product test?
 2. Who provides the IC with BIST IP function to your company?
 3. Are BIST designs and implementations consistent across products within your company?
 4. Are BIST tests (the IP) proprietary to your company?
 5. Do you give the BIST information on how to run it out to your customers?
 6. How is BIST operation documented / communicated?
 7. How is the BIST function accessed usually within the IC ?
(Can choose more than one answer)
 8. What reason drives you to use BIST in product test?
(change to why do you use BIST)
- Now to continue as working meeting



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