

Boundary-Scan Adoption

An Industry Snapshot
with Emphasis on the
Semiconductor Industry

Philip B. Geiger



Steve Butkovich



2009 International Test Conference



Purpose

- Gauge the penetration of IEEE 1149.x boundary-scan implementation today.
- Identify familiarity with existing, new, and proposed boundary-scan standards.
- Identify issues encountered while implementing boundary-scan.
- Identify reasons why boundary-scan currently is not used.
- Identify research areas for future iNEMI projects

Outline

- iNEMI's Boundary-scan Adoption Project
- Survey Methodology
- Survey Results
- Conclusions

iNEMI's Boundary Scan Adoption Project

- Organized under the Board and Systems Manufacturing Test Technology Integration Group (TIG).
- Goals:
 - to promote wider adoption of boundary-scan (JTAG/IEEE 1149.x)
 - to gauge the adoption level of boundary-scan
 - encourage semiconductor suppliers to include the technology in their products

Survey Methodology

- Survey focused on two groups
 - Board/System Engineering
 - Semiconductor Engineering
- Three Question Categories
 - General information
 - Name, Company info, area of responsibility
 - Board/System Engineering
 - 51 questions covering the survey objectives
 - Semiconductor Engineering
 - 23 questions covering the survey objectives

Survey Results – Respondent Statistics

- Total of 238 respondents to the survey representing:
 - 131 companies
 - 27 countries
- 86% were Board/System Engineers
- 14% were Semiconductor Engineers

Survey Results – Respondent Statistics

- Board/System Engineers (205 respondents)
 - 44% Test Engineers
 - 23% Engineering/Manufacturing Managers
 - 33% Development/Service/Apps Engineers
- Semiconductor Engineers (33 respondents)
 - 34% DFT/Test Engineers
 - 18% Engineering Managers
 - 48% IC Development Engineers

Survey Results – Respondent Statistics

- Board/System Engineer Industry Sector Statistics
 - 28% Netcom
 - 17% Test Equipment/Services Provider
 - 11% Military/Aerospace
 - 11% Office/Large Business Systems
 - 10% Consumer/Portable
 - 23% Other/CM/Medical/Automotive

Survey Results – Respondent Statistics

- Semiconductor Engineer Industry Sector Statistics (Primary Business)
 - 52% Semiconductor Design
 - 15% Semiconductor Fabricator
 - 15% Semiconductor Services Companies
 - 6% OEMs
 - 6% Test Equipment Providers

Survey Results – Boundary-Scan Standards and Initiatives

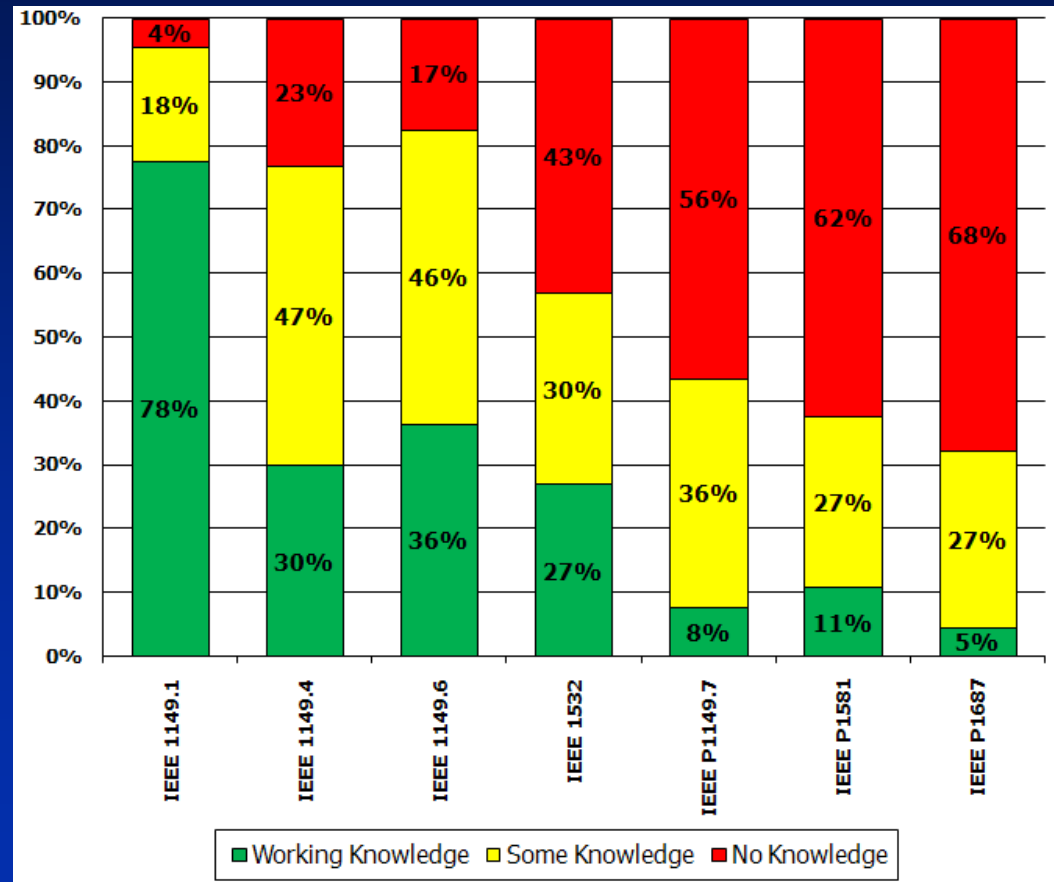
Board/System Engineer Knowledge of Standards

The standards that are most well known are the oldest:

1149.1, 1149.6,
1149.4

The newer proposed standards are the least well known:

P1581, P1149.7,
P1687



Survey Results – Boundary-Scan Standards and Initiatives

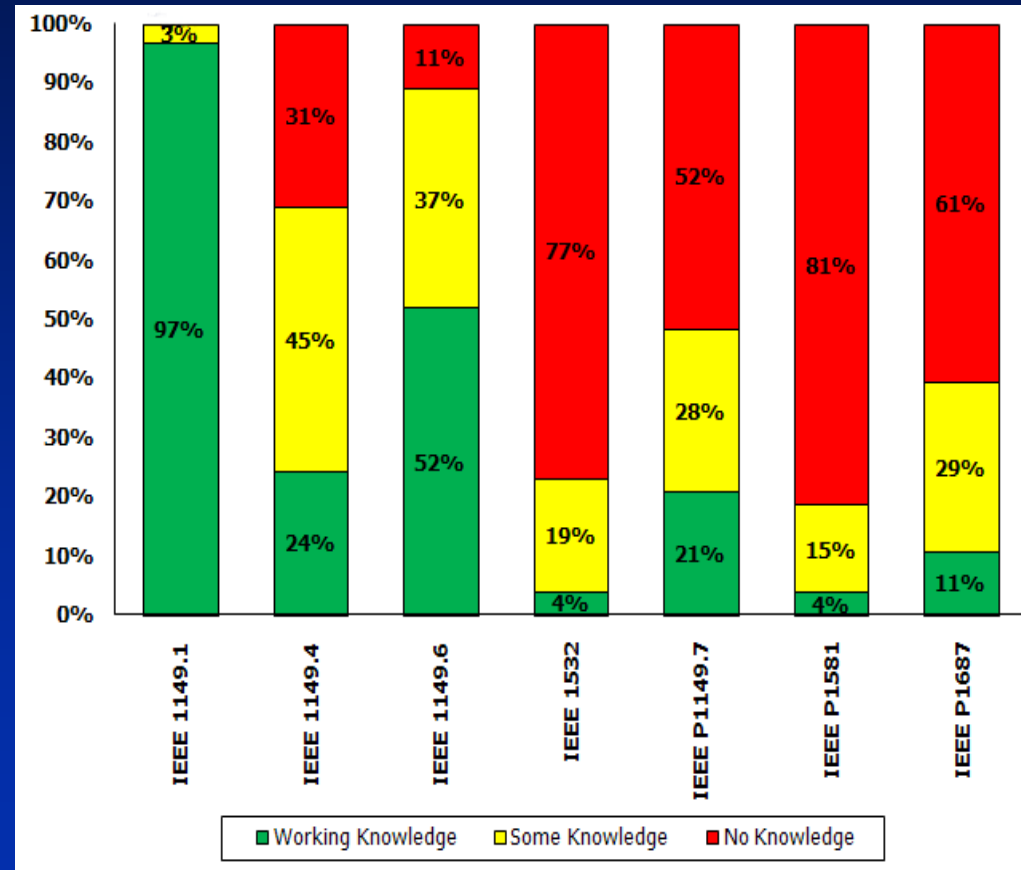
Semiconductor Engineer Knowledge of Standards

The oldest standards are the most well known:

1149.1, 1149.6

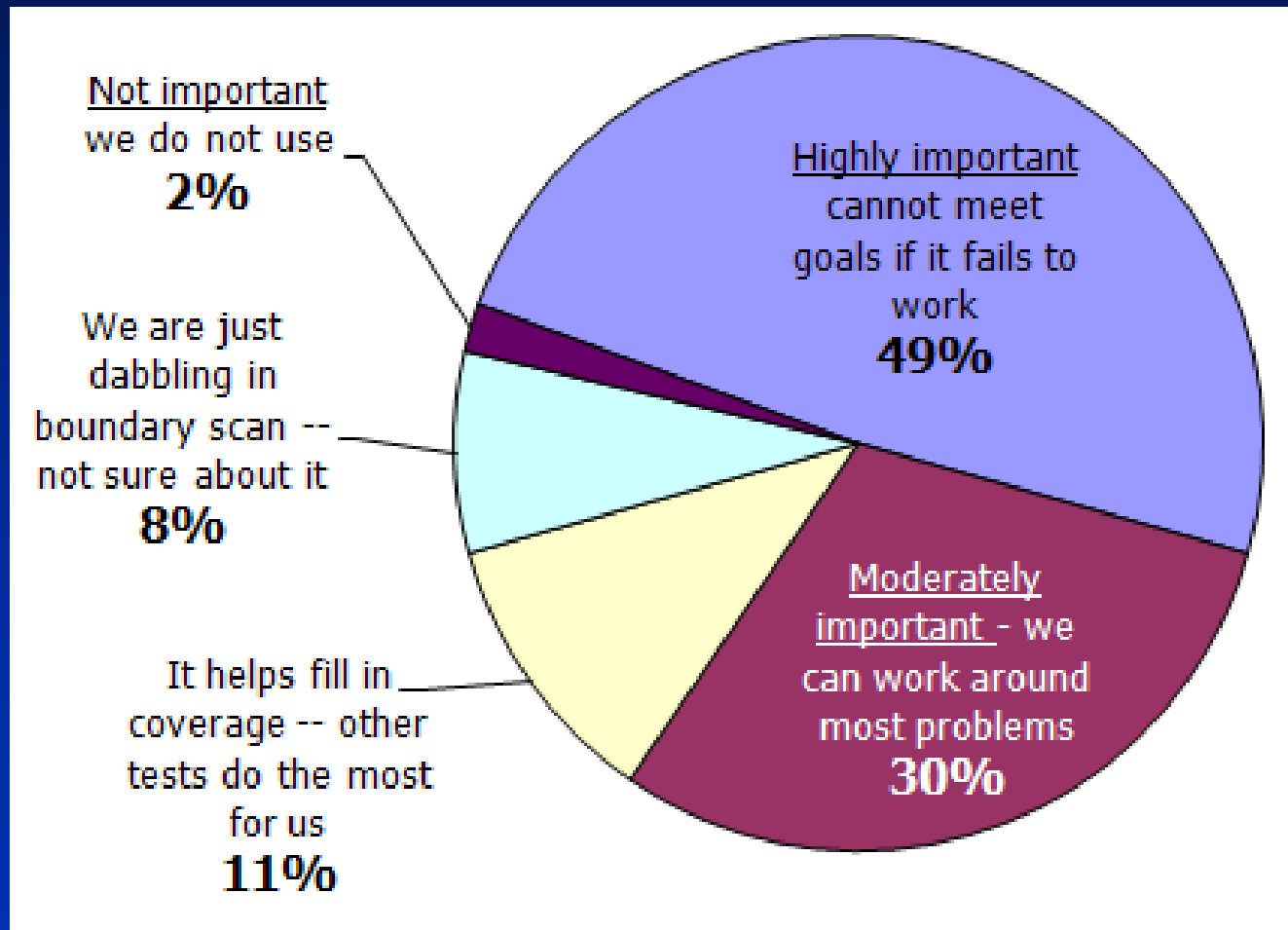
The newer proposed standards are the least well known:

P1581, P1149.7, P1687



Survey Results – Board/System Engineering

How important is Boundary Scan?

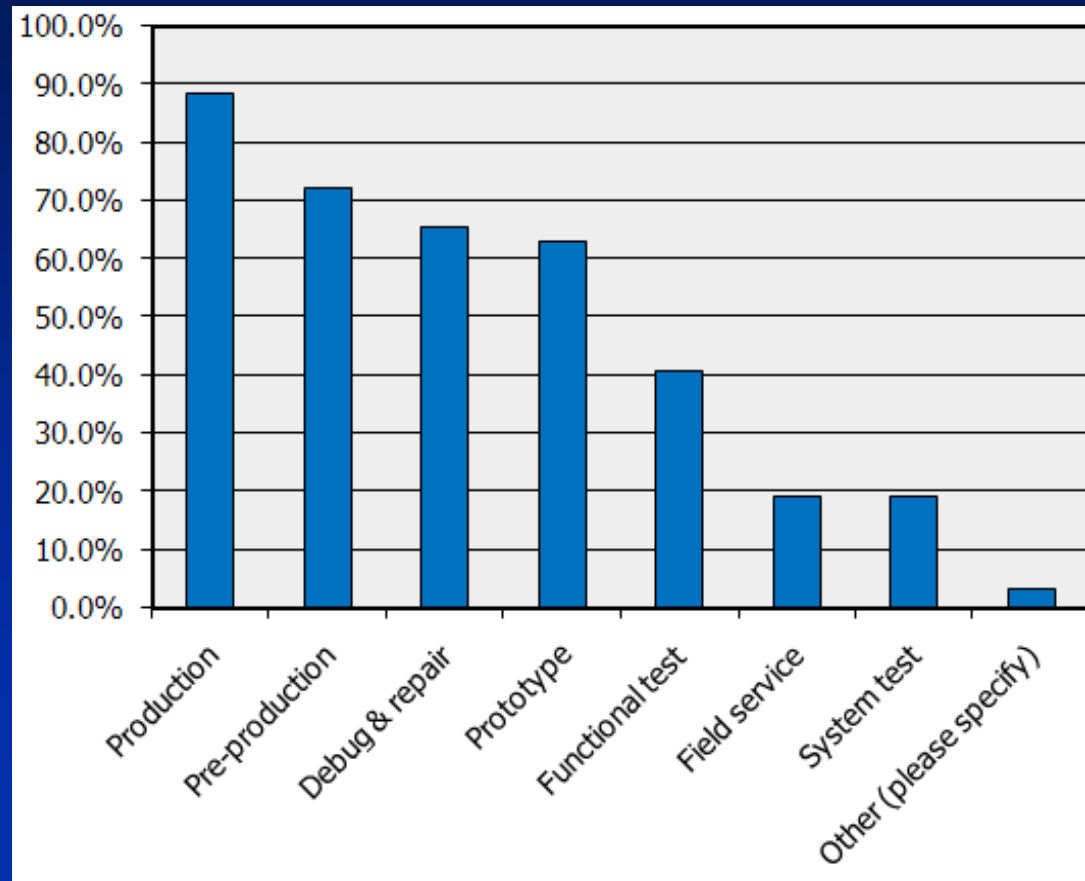


Survey Results – Board/System Engineering

Areas in which Boundary-scan is Used

Top 5 Uses for Boundary Scan:

- Structural Test
- Part Programming
- Device Version Verification
- Circuit Board Debug and Diagnosis
- Nail Reduction for ICT Fixtures



Survey Results – Board/System Engineering

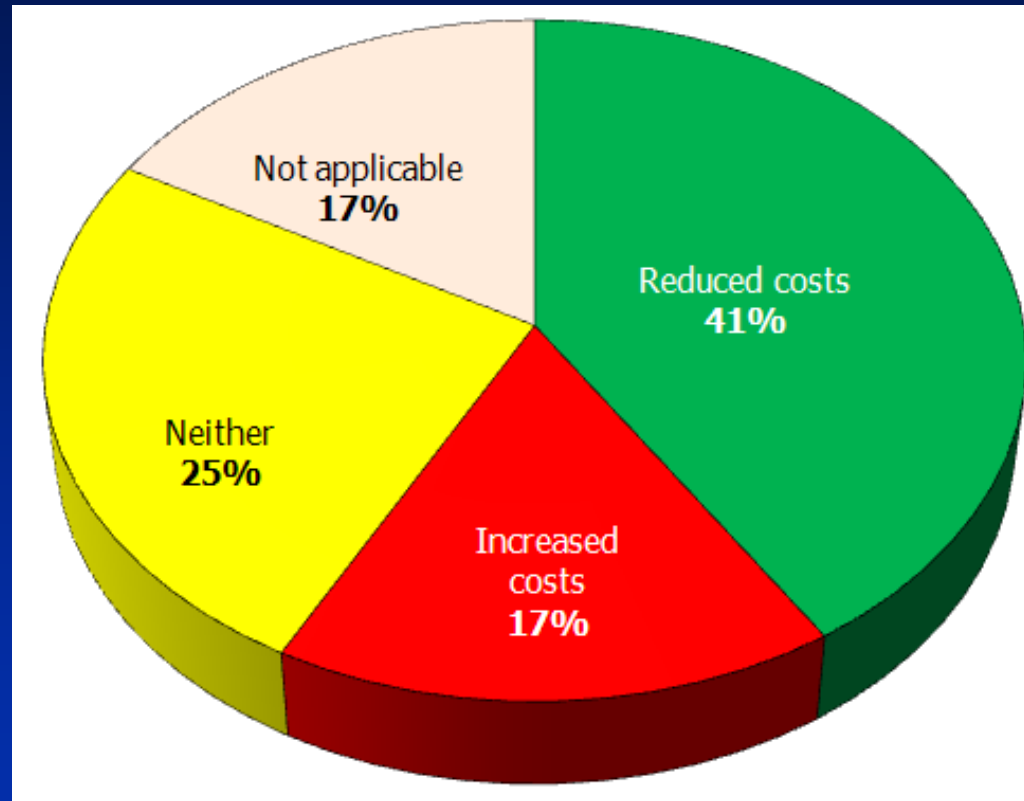
Boundary-Scan Cost Impact

Examples of Reduced Cost:

- Faster debug of prototypes
- Faster prototype turn time at no cost
- Reduced cost of ICT

Examples of Increased Costs:

- Cost of boundary-scan hardware and software
- Boundary-scan parts more expensive than traditional parts



Survey Results – Board/System Engineering

Boundary-Scan Time Impact

Reduced Time

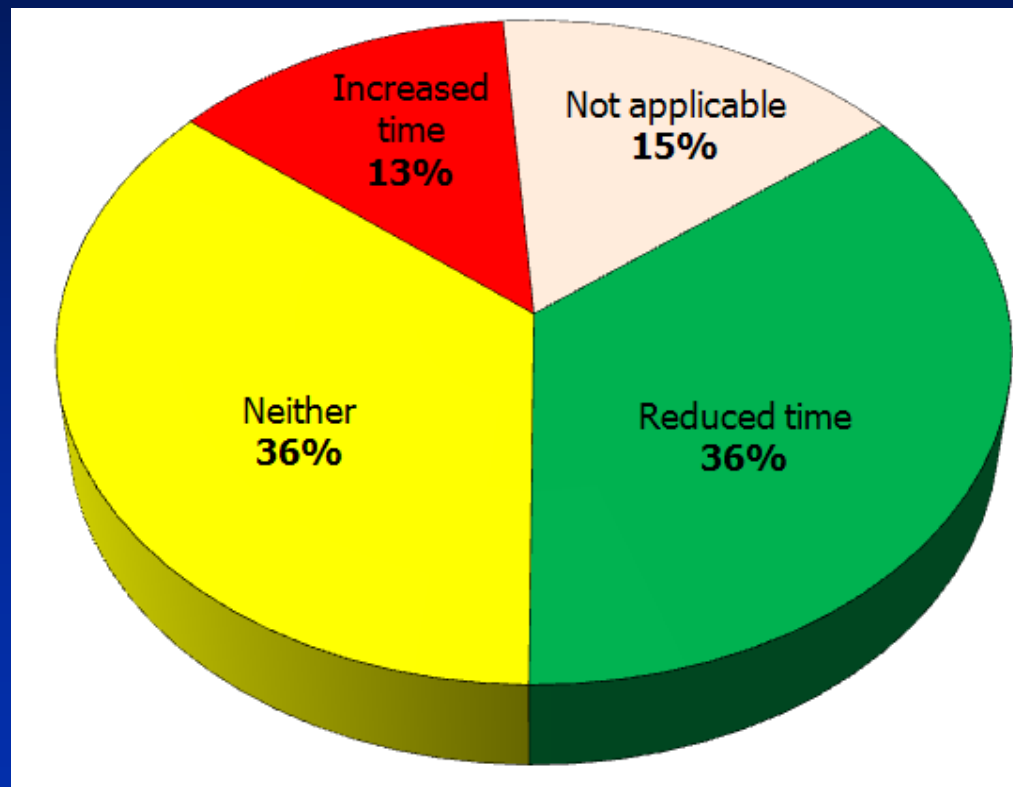
Examples:

- Faster debug of prototypes
- Faster ICT and Functional Test development
- Simplified process for part programming
- Less expensive test tooling due to reduced testpoint requirements

Increased Time

Example:

- Additional time for DFT implementation in designs



Survey Results – Board/System Engineering

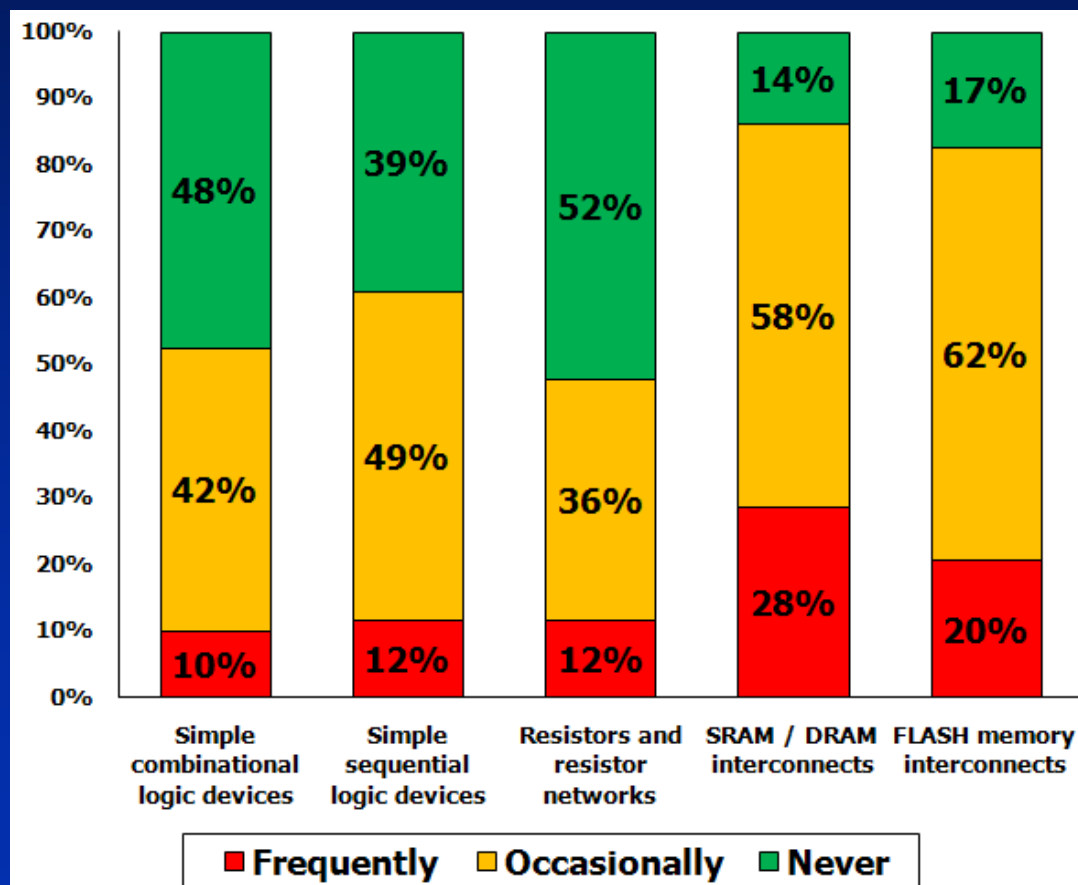
- Board/System engineers report using boundary-scan to test the following non-boundary-scan devices:
 - 74% test simple combinational logic
 - 66% test simple sequential logic
 - 65% test resistors
 - 80% test SRAM/DRAM interconnects
 - 74% test FLASH memory interconnects

Survey Results – Board/System Engineering

Frequency of Encountering Problems Using Boundary-Scan to test non-Boundary-Scan Devices

Biggest Issues:

- SRAM/DRAM interconnects
- FLASH memory interconnects
- Simple sequential logic devices



Survey Results – Board/System Engineering

Do your companies do anything to verify JTAG compliance of semiconductors?

- 48% replied YES, 52% replied NO
- Those who replied YES provided descriptions that can be categorized as:
 - We verify by developing production tests
 - We verify during component validation
 - We run a BSDL file syntax check
 - We specify compliance in contracts
 - We do DFT and/or verify with data sheets

Survey Results – Board/System Engineering

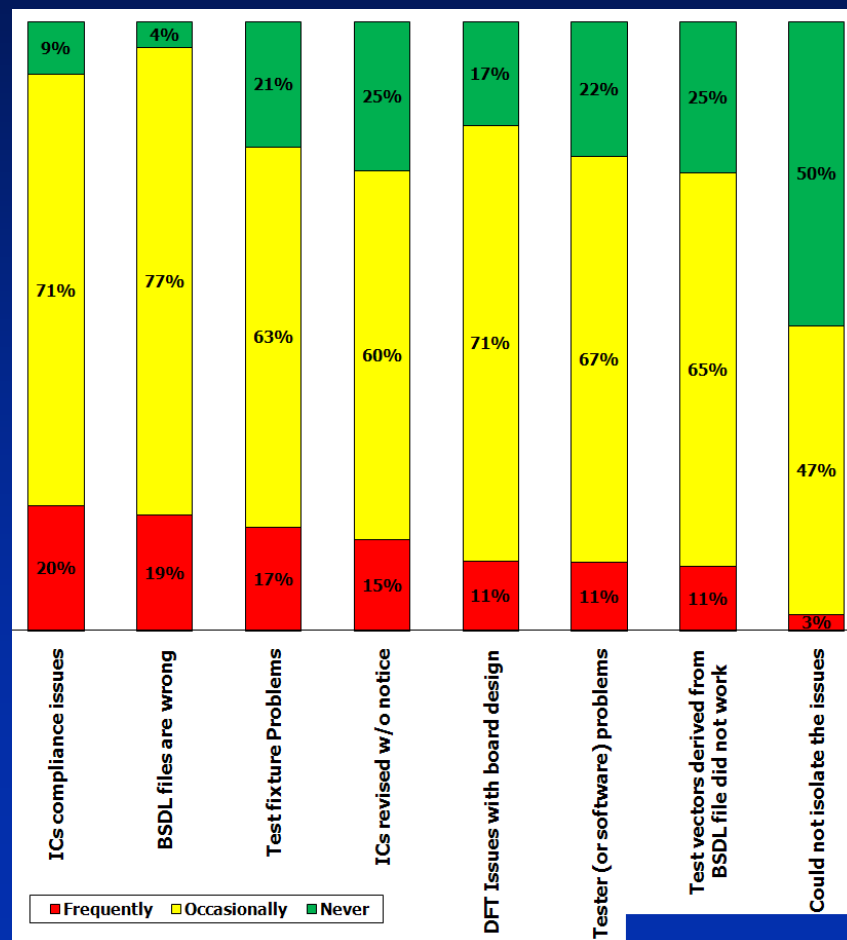
- Issues encountered when implementing boundary-scan
 - 44% had no issues
 - 40% had minor issues
 - 16% had major issues
- Top three major issues
 - Non-compliant, “bad”, or “wrong” BSDs
 - Devices non-compliant to 1149.x
 - DFT issues

Survey Results – Board/System Engineering

Frequency of Issues Implementing Boundary-Scan

Biggest Issues:

- BSDL files are “wrong”
 - 19% frequently
 - 77% occasionally
- IC compliance issues
 - 20% frequently
 - 71% occasionally
- DFT issues
 - 11% frequently
 - 71% occasionally



Survey Results – Board/System Engineering

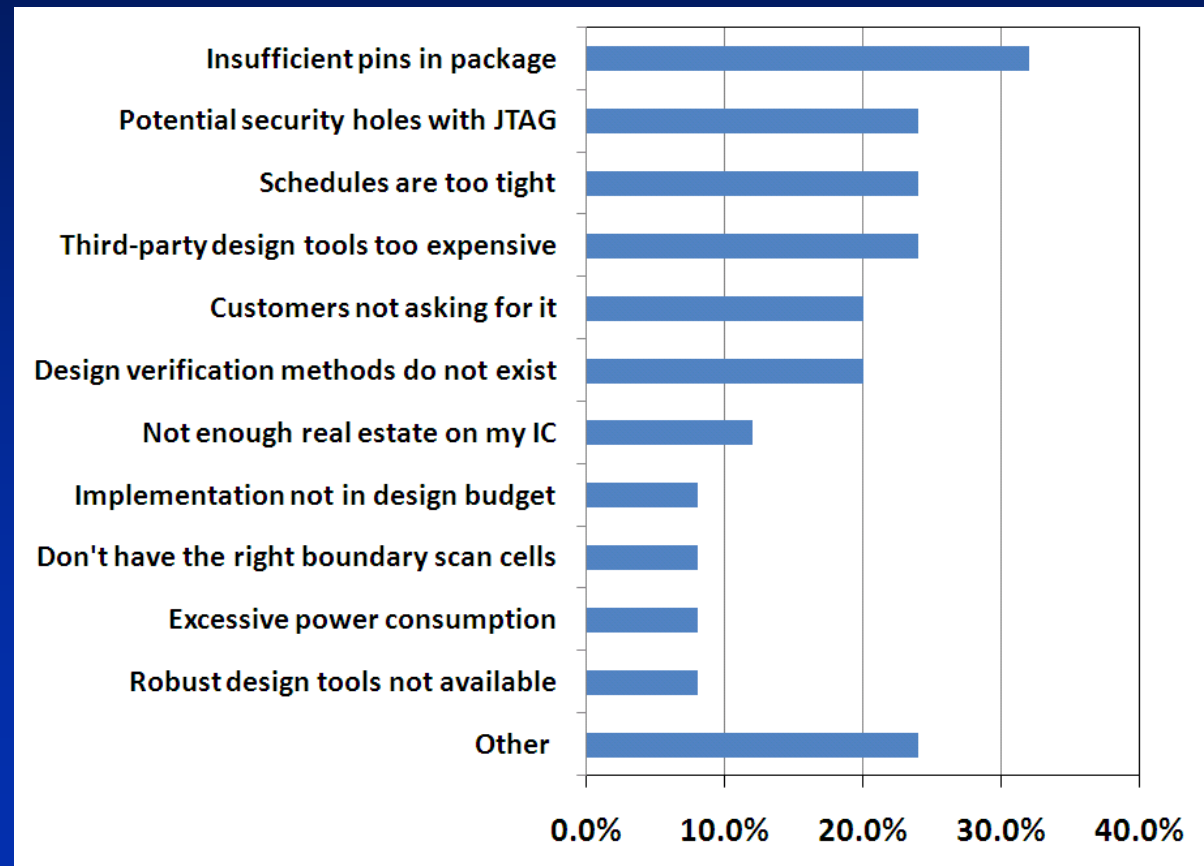
- Attributes important when choosing a semiconductor supplier
 - 80% regard boundary-scan support features as “Important” or “Very Important”
 - Features of greatest importance
 - Boundary-scan cells on a high number of device signal pins
 - Accuracy of device documentation
 - Availability of BSDL files

Survey Results – Semiconductor Engineering

What could hinder successful implementation of IEEE 1149.1 boundary scan on your next IC design?

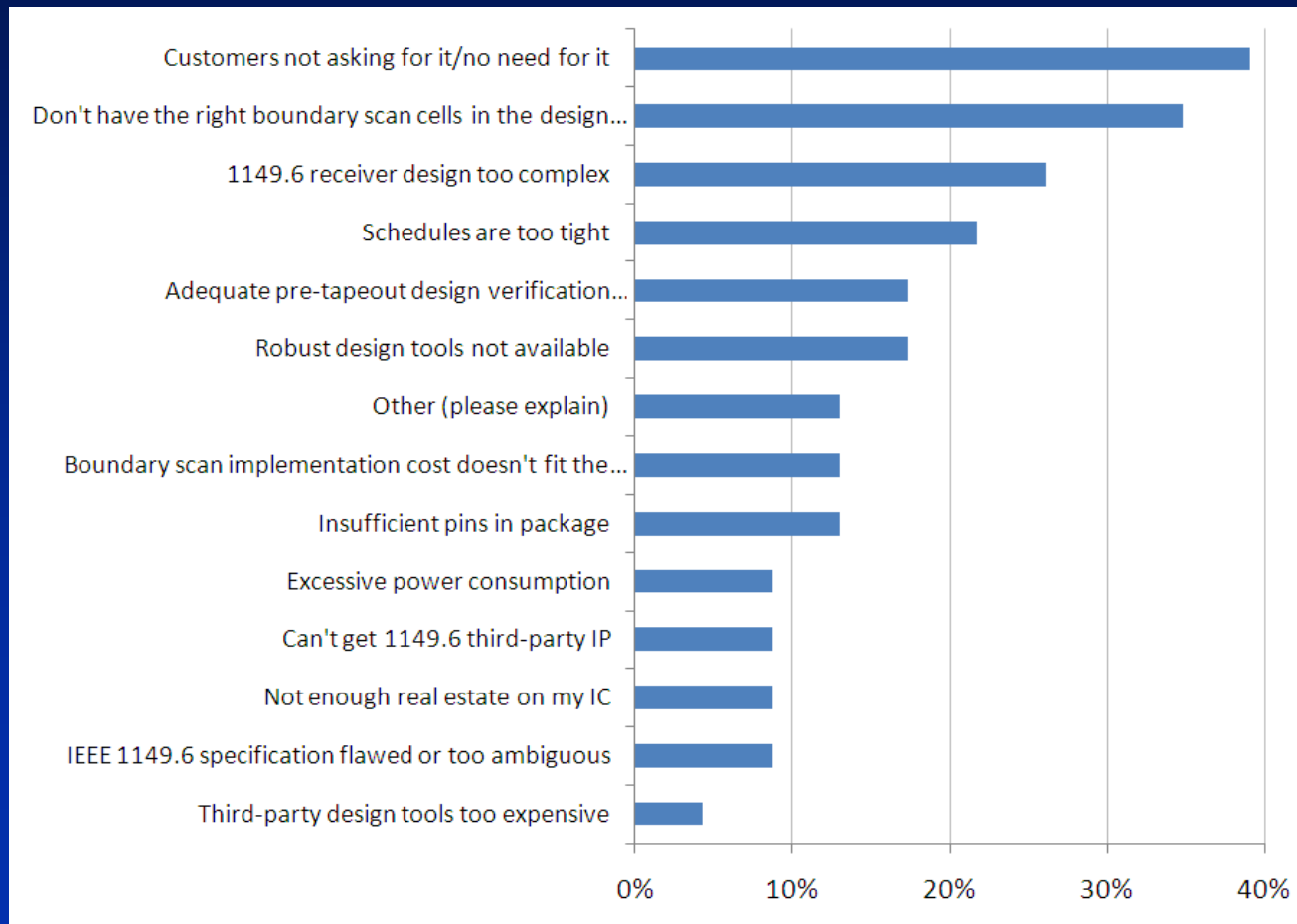
* Check all that apply

The most frequent “Other” issue cited was implementing 1149.1 on high-speed/low voltage complex I/O cells



Survey Results – Semiconductor Engineering

What could hinder successful implementation of IEEE 1149.6 boundary scan on your next IC design?

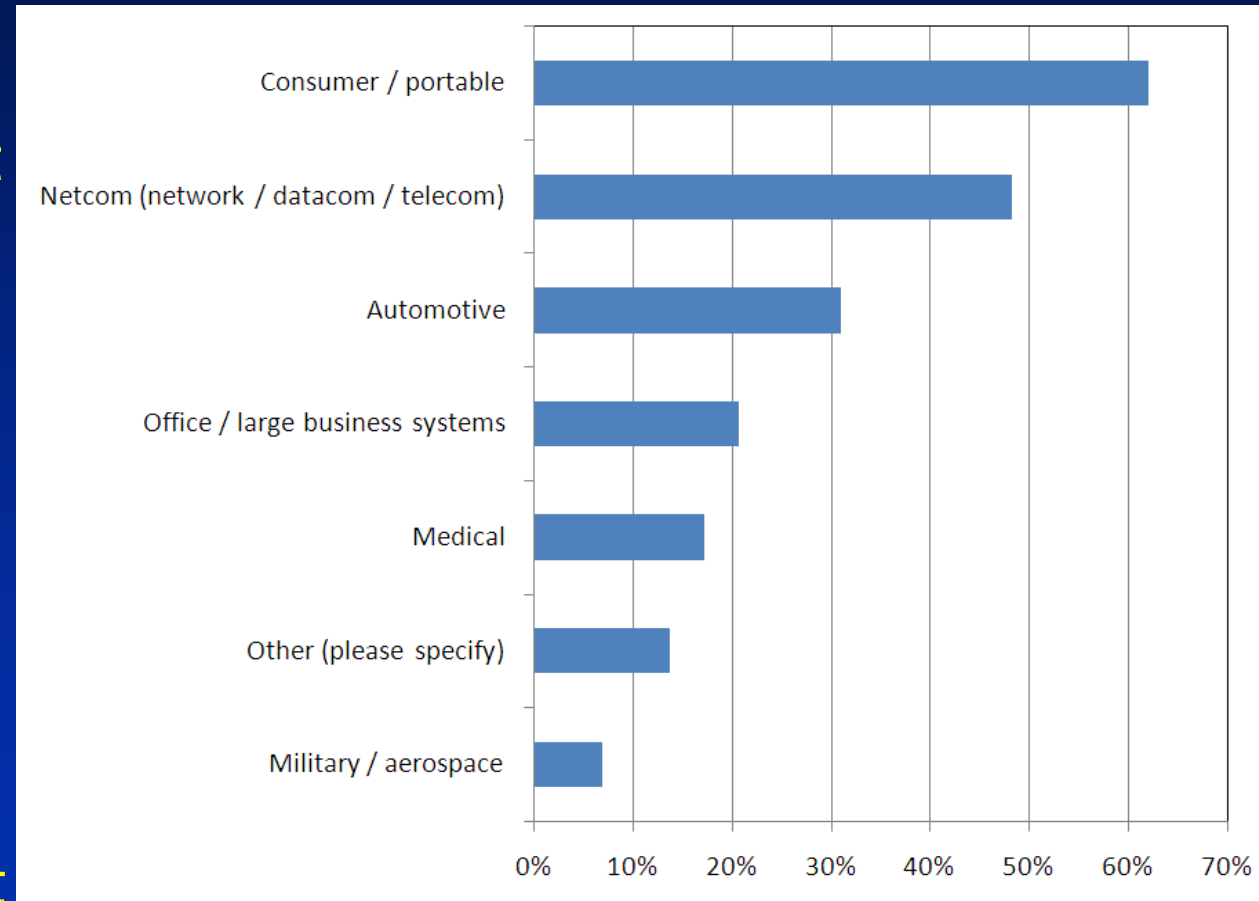


*** Check all that apply**

Survey Results – Semiconductor Engineering

Target applications for semiconductor designs

- Price Sensitive Consumer Market Represents the Largest Use Category
- The “Other” category included the test equipment market

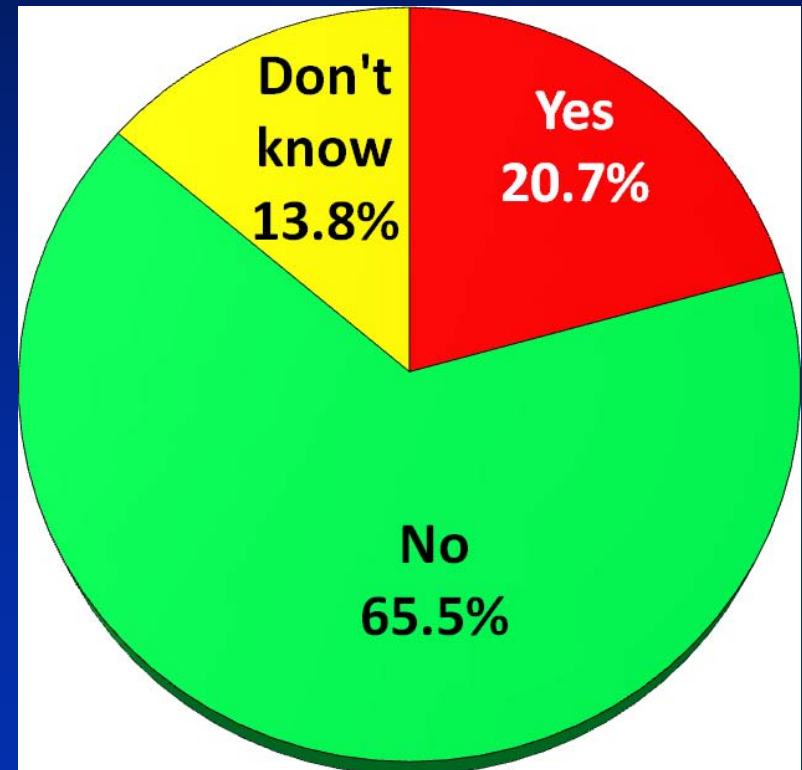


* Check all that apply

Survey Results – Semiconductor Engineering

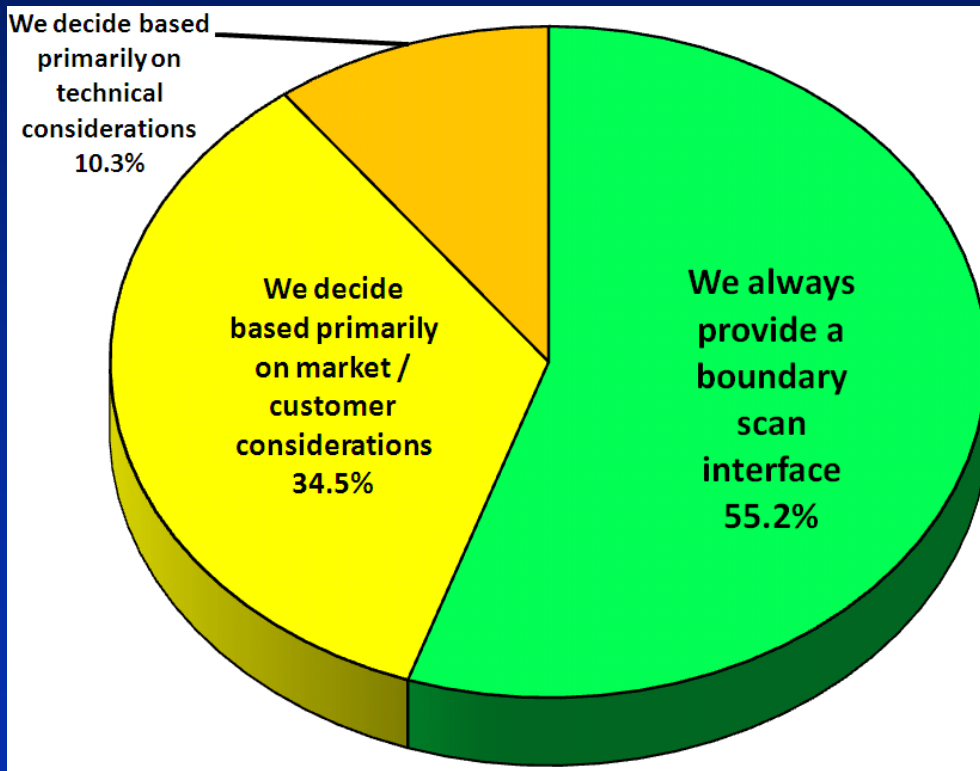
Would adding boundary scan have a negative impact on any of the parts your work group designs?

- If Yes, Why?
 - Takes a lot of engineering resources to add and validate bscan support to legacy on-chip I/O buffer designs
 - Impacts performance security, interoperability with other modes
 - Additional implementation effort
 - Potential loading effects on high speed interfaces.



Survey Results – Semiconductor Engineering

What is your company's policy regarding providing boundary scan interfaces in its devices?

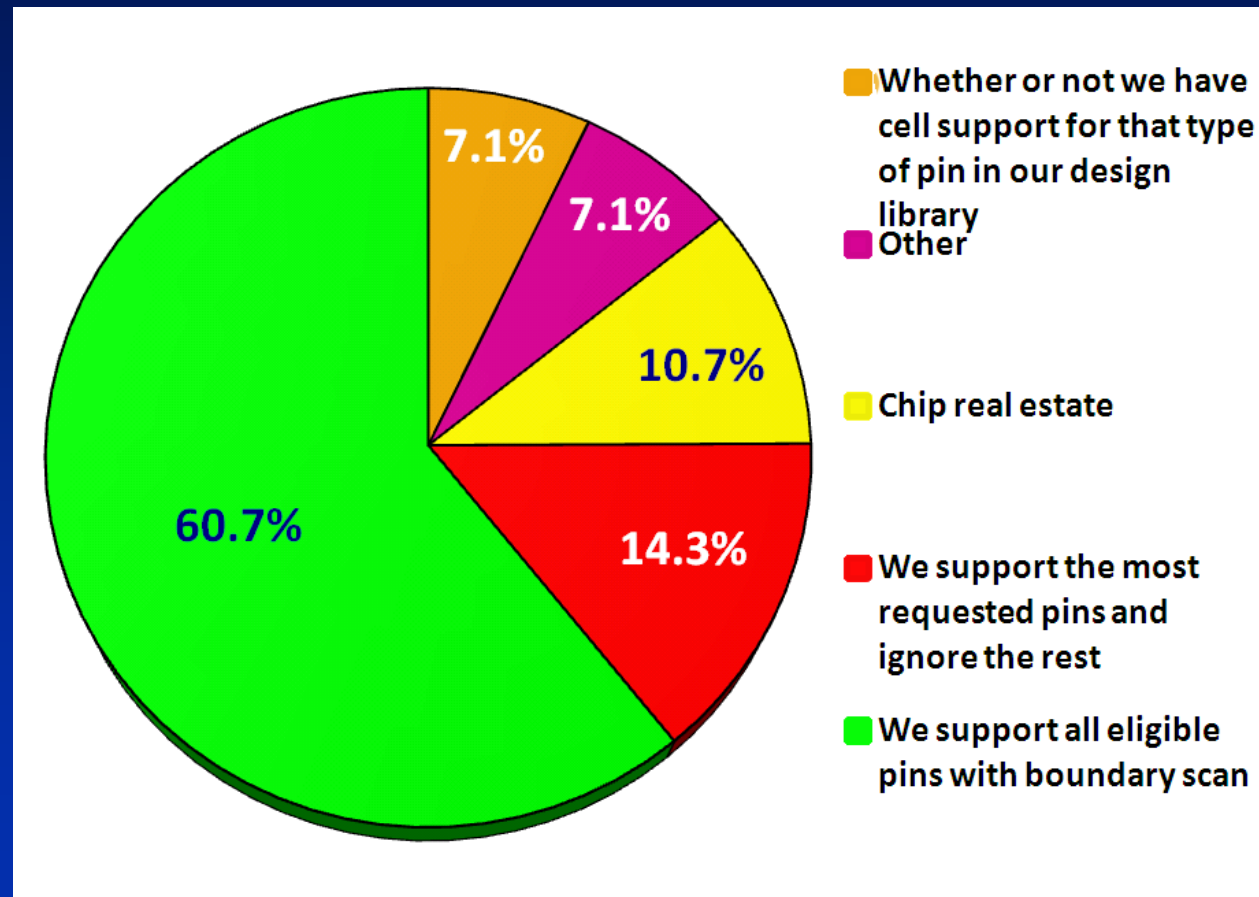


- 0% never provide a boundary-scan interface
- Based on responses, implementation seems to be increasing

Survey Results – Semiconductor Engineering

What determines which eligible pins will have a boundary scan cell?

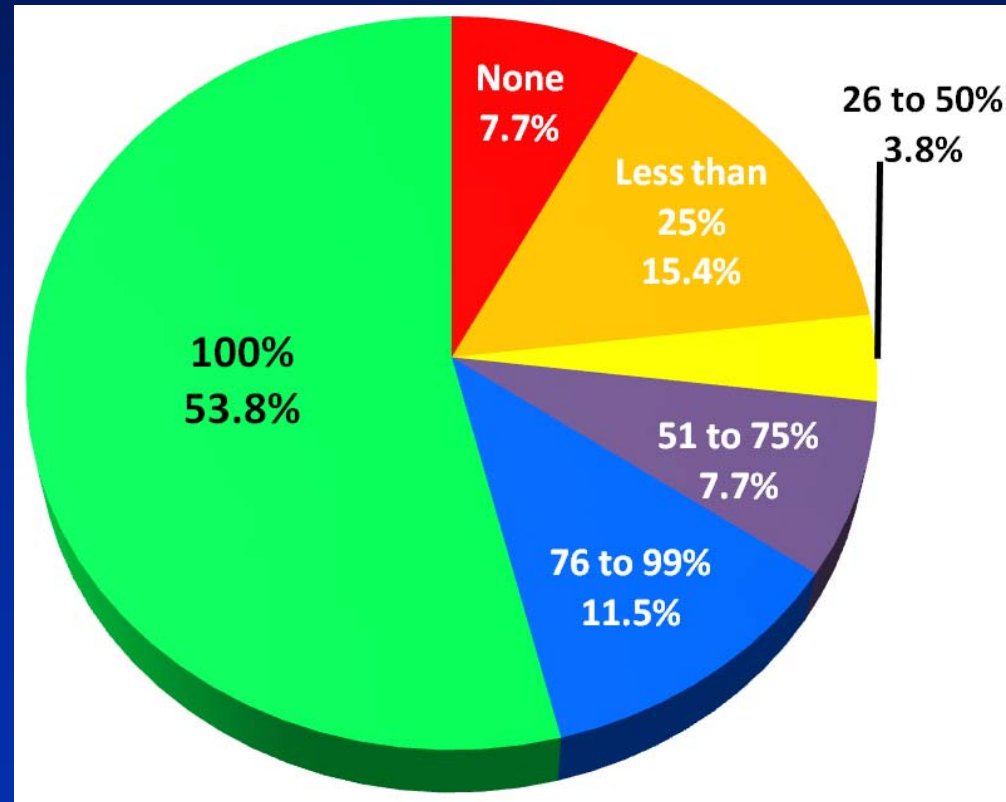
- Most common issue with support is interface speed.



Survey Results – Semiconductor Engineering

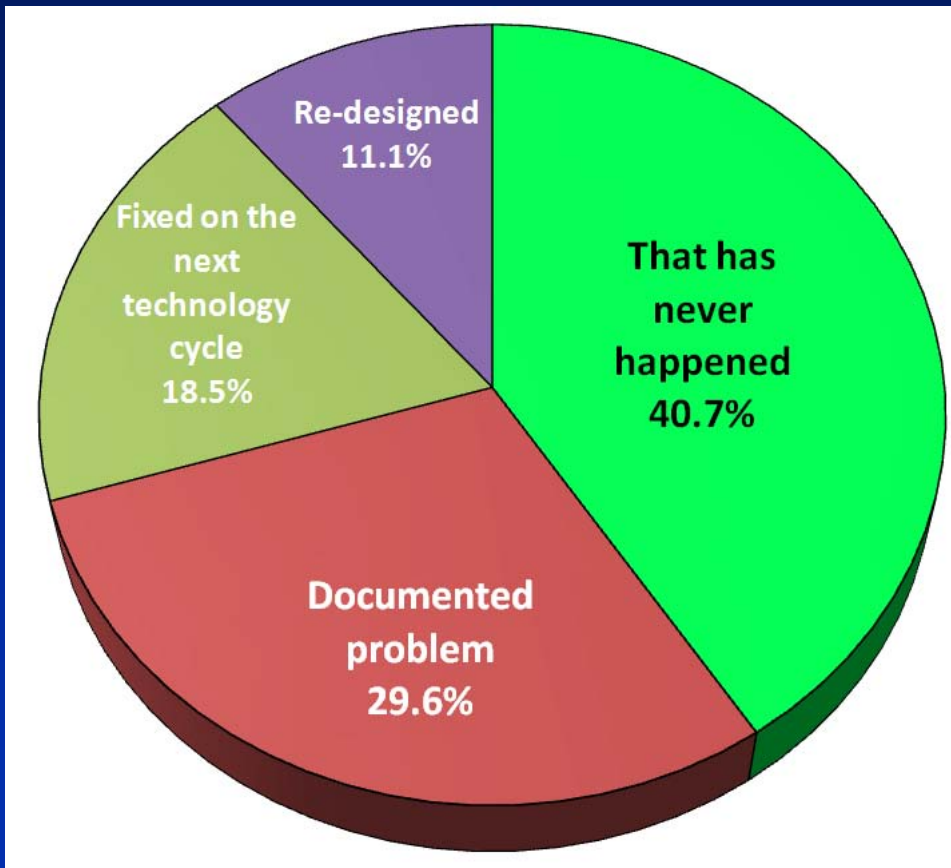
What percentage of devices your group worked on were intended to be IEEE 1149.1 compliant?

- Most semiconductor suppliers plan to include boundary scan as part of all devices
- Less than 8% work on devices not intended to be IEEE 1149.1 compliant



Survey Results – Semiconductor Engineering

When a device intended to be compliant with IEEE 1149.1 that was found to be non-compliant, what action did you take to resolve the issue?

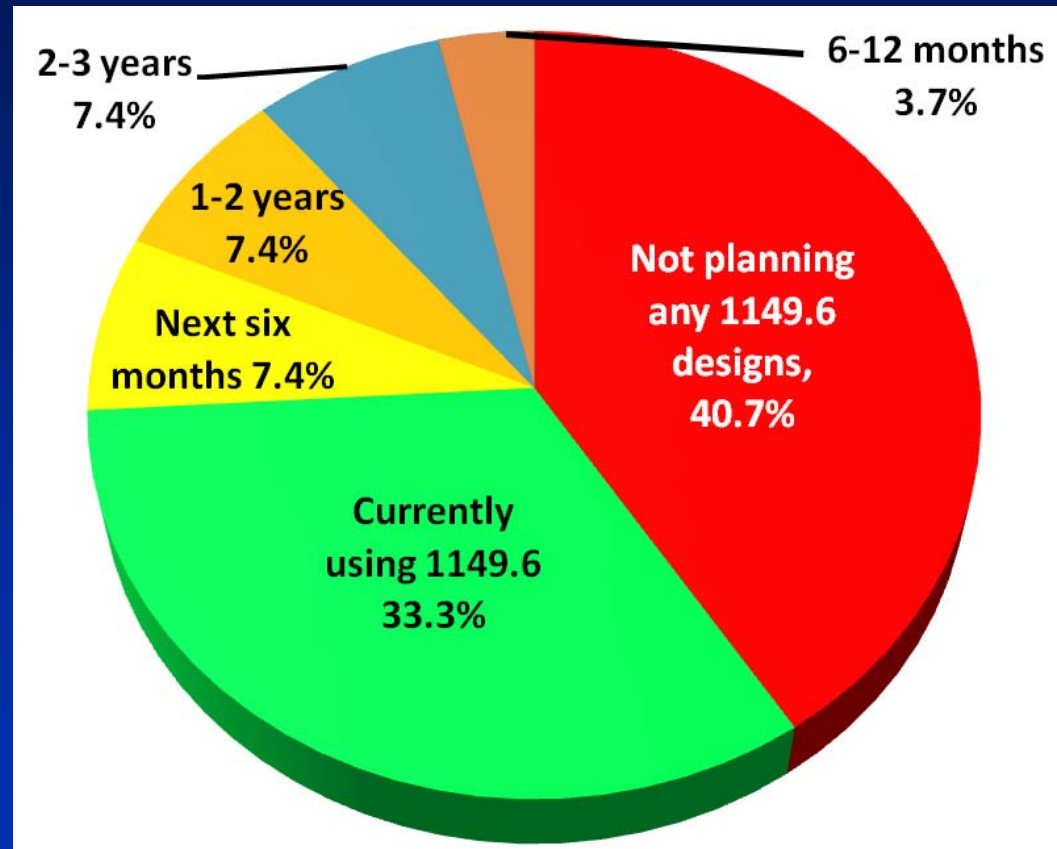


- When problems occurred they are frequently not repaired
- Most common action is to document the problem

Survey Results – Semiconductor Engineering

What are your company's current or future plans to produce IEEE 1149.6 designs?

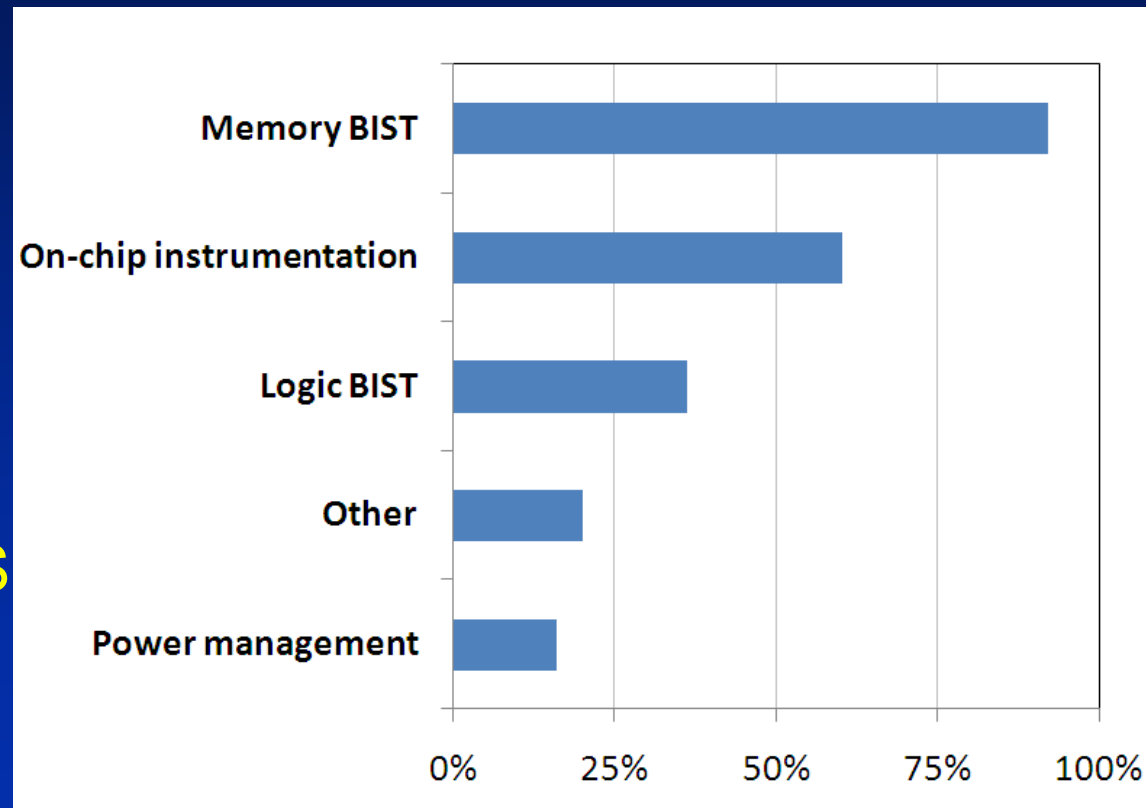
- 1149.6 - “AC Boundary Scan” - is gaining slower acceptance than other boundary-scan standards



Survey Results – Semiconductor Engineering

If you design advanced boundary scan features in devices, indicate which features are provided.

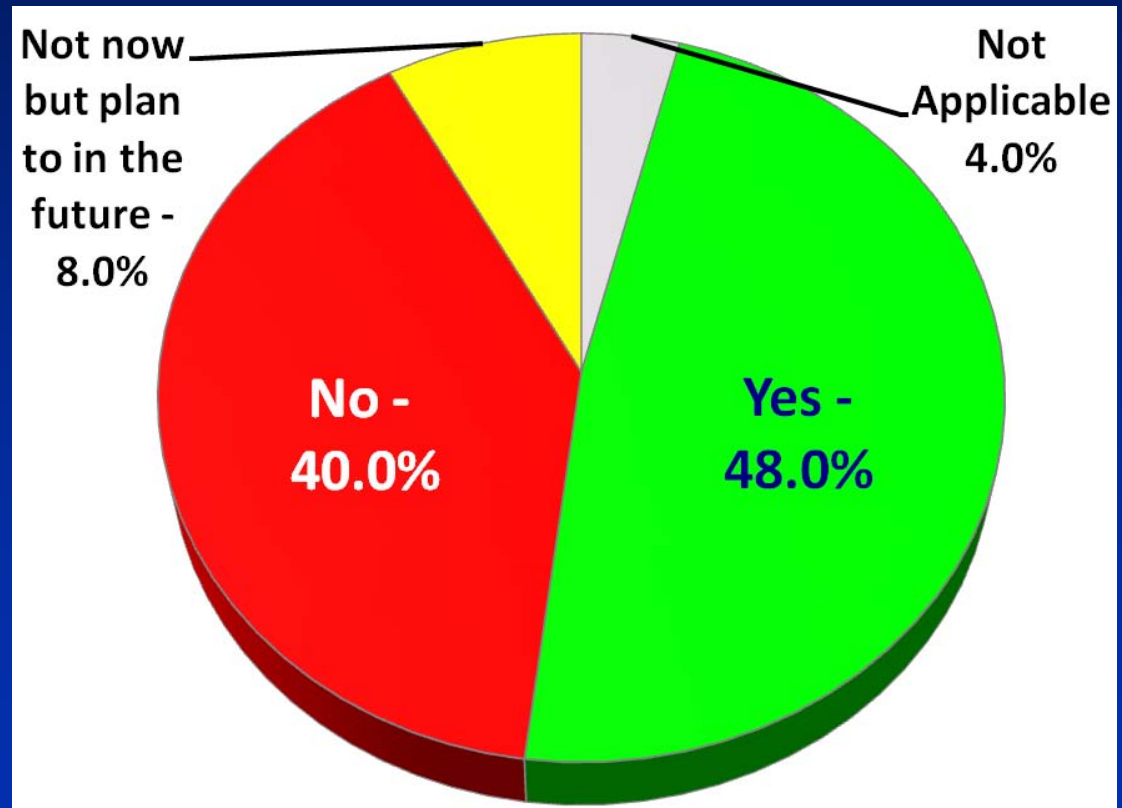
- “Other” Features include
 - ARM JTAG debug
 - All test mode control
 - Scan test compression PRBS control
 - Flash memory and On-Chip Debug



Survey Results – Semiconductor Engineering

If you design in advanced boundary-scan features in devices, do you allow customers access to those features via the boundary scan port?

- Almost half of the respondents provide advanced feature support via the 1149.x Test Access Port



Survey Results – Semiconductor Engineering

Does your company consider a BSDL file a company confidential document?

- Almost 20 percent considered the BSDL confidential
- BSDL is made available to direct customers under NDA

Conclusions

- Boundary-scan is a VERY important feature to Board/System engineers!
 - 98% of respondents use boundary-scan
 - 79% rated it as highly or moderately important
 - It is widely used in circuit board test and debug
- Semiconductor engineers have a good working knowledge of released boundary-scan standards and in general, support it.
- Based on input from Board/System Engineers, what can the semiconductor industry do better?

Conclusions

- Make a greater effort to produce correct and compliant BSDLS
 - The #1 issue reported was BSDLS problems
- BSDLS files need to be easier to obtain
 - 45% of the Board/System Engineers reported this
- A better job needs to be done verifying JTAG hardware compliance
 - Non-compliance is typically found when a test is generated and it doesn't work!

Conclusions

- Get involved with the P1581 working group and implement the standard in future memory devices
 - 80% of the respondents struggle to test memory devices with no on-chip testability
- Increase involvement by the semiconductor industry in boundary-scan proposed standards working groups
 - Semiconductor involvement is critical for successful early adoption of new standards