

Boundary-Scan Adoption – An Industry Snapshot with Emphasis on the Semiconductor Industry

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Abstract

Increasing circuit densities and speeds are quickly reducing electrical test point access for printed circuit assembly test. Boundary-scan (JTAG/IEEE 1149.x) is a technology that will allow continued testability of printed circuit assemblies, but its use requires that it be designed into semiconductor devices. Currently, not all semiconductor suppliers support boundary-scan. Wider availability of complying devices is necessary to enable cost-efficient and effective board test for future designs.

This paper presents the results of a boundary-scan survey developed by the International Electronics Manufacturing Initiative (iNEMI). The survey was intended to gauge the current adoption rate of boundary-scan, identify any impediments to widespread use, and select areas for future research.

1. Introduction

iNEMI is an industry-led consortium of more than 65 manufacturers, suppliers, industry associations and consortia, government agencies and universities. Its mission is to identify and close technology gaps.

Based in Herndon, Virginia, iNEMI has regional offices in Shanghai, China and Limerick, Ireland. For additional information about iNEMI, visit <http://www.inemi.org>.

The iNEMI Boundary-Scan Adoption Project was organized under the Board and Systems Manufacturing Test Technology Integration Group (TIG). The project's goal is to promote wider adoption of boundary-scan (JTAG/IEEE 1149.x) throughout the electronics industry, encourage semiconductor suppliers to include the technology in their products, and promote the development of tools by ATE (automated test equipment) suppliers to support boundary-scan based board test.

The initial focus of this project was to conduct an industry survey to determine how boundary-scan is currently being used, identify what issues boundary-scan users encounter, and how those issues impact results. The project team developed an online questionnaire and solicited participation from the iNEMI membership and team member contacts, and promoted the survey through trade publications and the iNEMI website.

In this paper we present a description of the boundary-scan survey, significant results of the survey, and the conclusions derived from those results, with emphasis given to issues related to the semiconductor industry.

2. The iNEMI Boundary-Scan Survey

2.1 Survey Objectives

The objectives of the boundary-scan survey were as follows:

- gauge the penetration of IEEE 1149.x boundary-scan implementation in several industry sectors;
- identify familiarity with existing, new, and proposed boundary-scan standards;
- identify issues encountered by survey respondents while implementing boundary-scan;
- identify reasons why boundary-scan currently is not used;
- identify research areas for future iNEMI projects.

2.2 Survey Methodology

It was determined that the survey should focus on two groups; Board/System Engineering and Semiconductor Engineering. Each group brings its own unique perspective to designing and implementing boundary-scan.

The first section of the survey consisted of general information, such as name, company name and primary business sector, company's annual sales, and respondent's primary area of responsibility (Board/System Engineering or Semiconductor Engineering).

Depending on their answers, the respondents were then directed to either the Board/System Engineering section or the Semiconductor Engineering section.

The Board/System Engineering section consisted of 51 questions that covered such topics as:

- industry (product) sector the respondent works in;
- knowledge level of assorted released and proposed 1149.x and related standards;
- importance of boundary-scan to design or production goals;
- current implementation level of boundary-scan based processes in product development and production test;
- frequency and impact of issues encountered in implementing boundary-scan;
- advantages/disadvantages of boundary-scan;
- plans for future implementation of boundary-scan in board/system level design and production test processes;
- types of devices for which the respondents would like to see boundary-scan offered in the near future.

The Semiconductor Engineering section consisted of 23 questions that covered:

- knowledge of released and proposed 1149.x and related standards;
- current and planned support for boundary-scan standards;
- issues that have or could hinder successful implementation of boundary-scan in IC designs;
- target applications for the respondents' designs;
- boundary-scan design, simulation, and verification processes and associated issues;
- plans for future implementation of boundary-scan in IC designs.

3. Boundary-Scan Survey Results

3.1 Respondent Statistics

A total of 240 people, from 131 companies and 27 countries responded to the survey.

Of the respondents, 205 (86%) classified themselves as Board/System Test Engineering and 33 (14%) classified themselves as Semiconductor Engineering.

3.1.1 Board/System Test Engineering Respondent Demographics

Company size (in annual sales) for Board/System Test Engineering respondents broke down as:

- 51% greater than \$500 million;
- 34% in the \$10-\$500million range
- 15% less than \$10 million.

When asked about their specific job functions, nearly half (44.3%) of the Board/System Test Engineering respondents said they were Test Engineers.

Table 1 shows the overall job function breakdown for the Board/System Test Engineering respondents.

Job Function	Response
Test Engineer	44.3%
Development/Test Engineering Manager	17.2%
Test Equipment Provider	9.9%
Designer	9.4%
DFT Consultant	8.9%
Manufacturing Manager	5.4%
System Architect	1.5%
Service and Support	1%
System-Level Applications	1%
Other	.9%
Field Service Engineer	0.5%

Table 1 Board /System Test Respondent Job Functions

The majority of Board/System Test respondents (27.7%) were in the Netcom industry sector (telecom, datacom, and networking), followed by Test Equipment/Services Providers (17.3%) and Military/Aerospace (11.4%). The majority of "Other" respondents were involved in Industrial Equipment/Controls.

Table 2 shows the overall industry sector break-down for the Board/System Test Engineering respondents.

Industry Sector	Response
Netcom	27.7%
Test Equipment/Services	17.3%
Military/Aerospace	11.4%
Office/Large Business Systems	10.9%
Consumer/Portable	9.9%
Other	8.4%
EMS/Contract Manufacturer	5.9%
Medical	5.4%
Automotive	3.0%

Table 2 Industry Sector Break-down for Board/System Test Respondents

3.1.2 Semiconductor Engineering Demographics

Company size (in annual sales) for Semiconductor Engineering respondents broke down as:

- 55% greater than \$500 million;
- 27% in the \$10-\$500million range;
- 18% less than \$10 million.

The top three respondent job functions chosen for Semiconductor Engineering were IC DFT/Test Engineer (34.4%), IC Logic Designer (25%), and IC Engineering Manager (18.1%).

Table 3 shows the overall job function break-down for the Semiconductor Engineering respondents.

Job Function	Response
IC DFT/Test Engineer	34.4%
IC Logic Designer	25.0%
IC Engineering Manager	18.1%
IC Architect	12.5%
IC Floorplan Designer	3.1%
IC I/O Designer	3.1%
Other	0%

Table 3 Semiconductor Respondent Job Functions

When asked what their company's primary business is, the majority of Semiconductor Engineering respondents answered "IC designer" (51.5%), followed by a tie between IC fabricator (15.2%) and "Other" (15.2%). The majority of "Other" responses were third-party semiconductor services companies. OEMs and test equipment providers were tied for third place (6.1% each).

3.2 Boundary-Scan Standards and Initiative Knowledge and Support

"Boundary-scan" is a generic term commonly used to describe several IEEE standards released since 1990, with 1149.1 and 1149.6 being the most common. Several initiatives for new standards that enhance or extend the effectiveness of boundary-scan for newer technologies are in process. Table 4 describes the currently released boundary-scan standards and working group initiatives.

All respondents were asked questions about their knowledge of and current and future support for these standards and initiatives.

IEEE Std	Revision	Test Type	Application
1149.1-2001 (BSDL added 1994)	Update (1 st Release 1990)	Digital BSCAN	Connectivity (DC)
1149.4-1999	1 st Release 1999	Analog BSCAN	Connectivity (Mixed signal)
1149.6-2003	1 st Release 2003	Advanced I/O BSCAN	Connectivity (AC-coupled) Differential, Serial Bus, High-Speed I/O, SerDes.
P1149.7 (cJTAG) Initiative	In Review. Vote expected in CY2009. (Superset of 1149.1)	Compact JTAG. BSCAN with reduced TAP pin count (2 rather than 4 pins) total.	Extended functionality of device integration, power management, application debug, and device programming. SoC and SiP test.
1500-2005	1 st Release 2005	Embedded Core BSCAN	Multi-core ASIC Test
1532-2002	1 st Release 2002	In-System Configuration BSCAN	In-system access & configuration of Programmable Devices. FPGA, ePLD, FlashRAM, etc.
P1581 Initiative	In Review. Draft to IEEE expected in CY2009	I/O Loopback (w/o adding pins to device). Augments 1149.1	Non-BSCAN Memory Device Test (DDR, SRAM, FLASH)
P1687 (iJTAG) Initiative	In Review. Vote expected in CY2010	Embedded Instrument Gateway access through 1149.1 TAP	Embedded Instrumentation control and access
SJTAG Proposed Initiative (IEEE has not assigned a number yet)	Request to IEEE for PAR in CY2009	Inter-module and Backplane BSCAN	System-based Connectivity (DC)
P1149.8.1 Selective-Toggle Initiative	In Review. Vote expected in CY2009.	Analog-Digital BSCAN.	Connector & Non-BSCAN Device Test. Powered OPENS Test.

Table 4 Current Boundary-Scan Standards and Initiatives

3.2.1 Board/System Test Engineering Support for Boundary-Scan Standards and Initiatives

When asked about their familiarity with boundary-scan standards Board/System Test Engineers replied as shown in Figure 1.

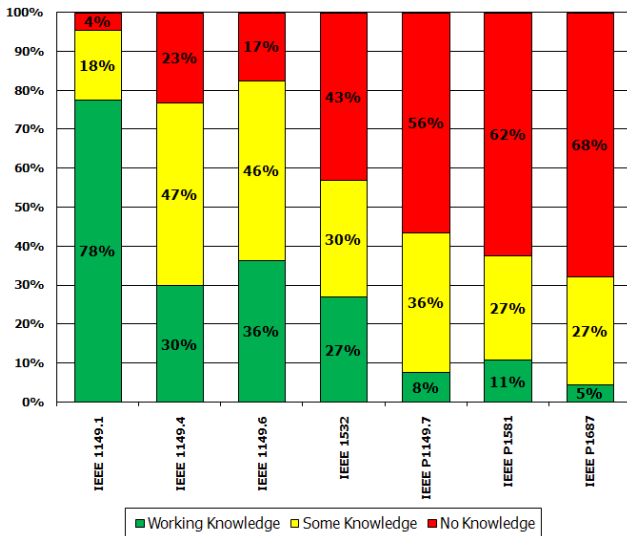


Figure 1 Board/System Test Engineer Familiarity with Boundary-scan Standards

The standards with which respondents have the most working knowledge are the oldest: 1149.1, 1149.6, and 1149.4. Newer proposed standards had the least amount of familiarity: P1687, P1581, and P1149.7.

3.2.2 Semiconductor Engineering Support for Boundary-Scan Standards and Initiatives

Semiconductor Engineers were also asked about their familiarity with boundary-scan standards to gauge knowledge of the standards that are commonly used for loaded circuit board test.

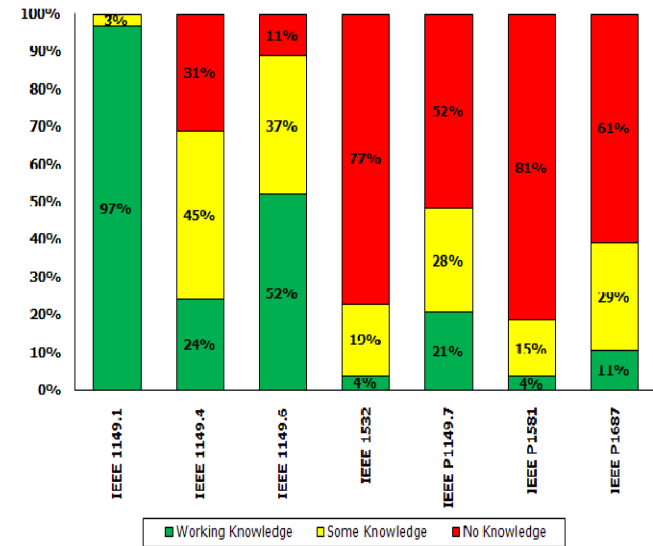


Figure 2 Semiconductor Engineer Familiarity with Boundary-Scan Standards

As shown in Figure 2, there is widespread familiarity with the long existing 1149.1 boundary-scan standard, but newer standards such as 1149.7 [1] and P1687 are virtually unknown.

Lack of a large number of responses from programmable logic device suppliers may have resulted in the low familiarity rate with the IEEE 1532 standard.

Several IEEE proposed standards, such as P1581 Static Component Interconnection Protocol and P1687 Methodology for Access to Embedded Test and Debug Features, are still in the

development stage and have not been widely promoted to the technical community.

3.3 Board/System Engineering Survey Results

The Board/System Engineering section of the survey included in-depth questions on a broad range of topics related to boundary-scan. The responses discussed in this paper highlight the extent to which boundary-scan is used, its importance in board and system design and development, and the standards that are supported.

3.3.1 How Important is Boundary-Scan to Board/System Test Engineers?

When Board/System Test Engineers were asked how important boundary-scan is to their production goals, more than three-quarters (79%) of the respondents said it was “Important”. Nearly half (49%) identified boundary-scan as “Highly important,” stating that they cannot meet goals if it fails to work, and 30% rated it as “Moderately important,” stating that they could work around most unsolvable boundary-scan issues encountered. Another 19% said that they only use boundary-scan to fill in test coverage or are “dabbling” in it; and only 2% stated that it is “Not important” and that they do not use it.

Figure 3 illustrates the response distribution.

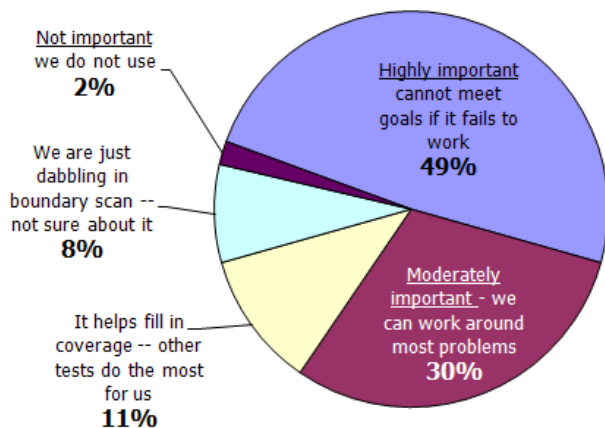


Figure 3 Importance of Boundary-Scan to Production Goals

Another indication of how important boundary-scan is to Board/System Engineers is the extent to which it is used in their development and production processes.

According to respondents, boundary-scan is most often used in production and pre-production circuit board testing (88% and 72%, respectively). In addition, 65% said they use it in circuit board debug and repair; 63% use it on prototypes, and 41% use it in circuit board functional test.

Figure 4 clearly shows significant use of boundary-scan throughout the engineering development and production processes.

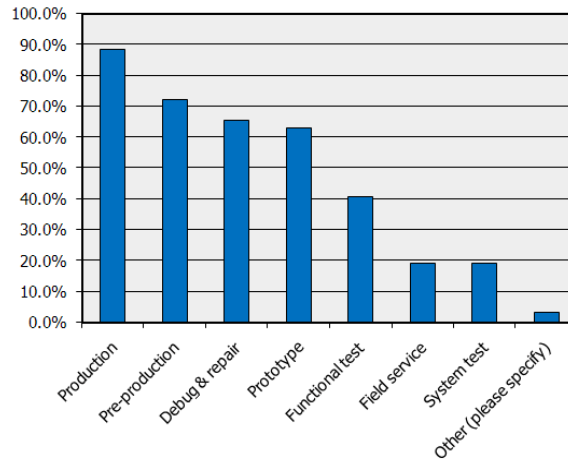


Figure 4 Areas of Development and Manufacturing in which Boundary-Scan is Used

When asked more detailed usage questions the respondents indicated that the following are the top five places boundary-scan is currently used:

- structural test (opens/shorts, ICT, memory interconnect);
- programming FLASH and programmable logic devices;
- device version verification;
- debug and diagnosis on production and prototype circuit boards;
- nail reduction for ICT fixtures.

Sixty percent of the respondents reported that they use boundary-scan in multiple functional areas on the same product.

3.3.2 How Does Boundary-Scan Affect Product Development Time and Cost?

When asked if boundary-scan had increased or reduced product development costs, 41% of respondents reported cost reductions, 25% were neutral, and 17% reported increased cost. These responses are represented in Figure 5.

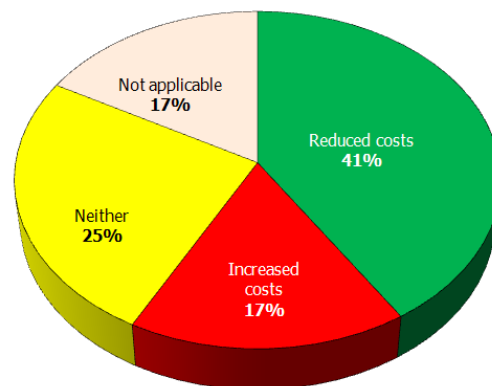


Figure 5 Boundary-Scan Cost Impact

People noted in comments that, although there may be up-front costs, boundary-scan saved money in the long run.

When asked to give specific examples of how boundary-scan has reduced development costs, 50 people responded. The majority of their answers can be summarized as:

- significantly faster debug of manufacturing defects in prototypes, allowing development engineers to concentrate on design verification;
- faster prototype turn time at no additional cost;
- reduced cost of in-circuit test fixturing and development.

The survey also asked for examples of how boundary-scan had increased development costs. Twenty-three people replied, and the majority of their answers can be summarized as:

- Cost of boundary-scan hardware and software;
- Boundary-scan parts more expensive than traditional parts.

Respondents were asked if implementing boundary-scan reduced or increased development time. “Reduced time” and “Neither” were tied at 36%; and 13% reported that boundary-scan increased development time, as shown in Figure 6.

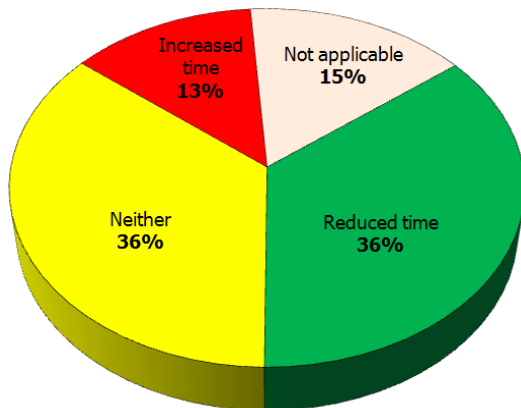


Figure 6 Boundary-Scan Time Impact

Many of the examples provided by the 39 respondents who said boundary-scan decreased development time were similar to those given for decreased development cost:

- faster test and debug of prototype boards, resulting in faster prototype turn time and higher quality prototypes delivered with few, if any, manufacturing defects;
- easier and faster development of in-circuit and functional board test;
- simplified FLASH and PLD part programming process;
- reduced testpoint requirements result in less expensive test tooling.

Fifteen respondents gave examples of ways that boundary-scan increased cost. The most common theme in those responses was added time for DFT implementation in the designs.

The Board/System Engineers were asked what benefits were derived from boundary-scan other than cost/time improvements. There were 109 responses to this question, many of which were similar to the cost or time responses.

- increased PCBA test coverage at prototype builds;
- higher fault coverage in production than with standard tests with increased fault identification;

- ability to maintain structural test coverage at ICT despite reduction in test point access ;
- easier and faster FLASH and PLD part programming and verification;
- ensures product quality and reliability (at reduced development time and cost).

3.3.3 Using Boundary-Scan to Test Non-Boundary-Scan Devices

The majority of Board/System Engineers said they use boundary-scan to test standard devices, including:

- simple combinational logic (74%);
- simple sequential logic (66%);
- resistors and resistor networks (65%);
- SRAM/DRAM interconnects (80%);
- FLASH memory interconnects (74%).

“Other” devices respondents tested using boundary-scan included LEDs, I2C/SPI parts, A/D or D/A converters, and connectors/sockets.

Significant issues were reported when testing non-boundary-scan devices. SRAM/DRAM interconnects were cited most often for causing problems when tested with boundary-scan (58% said they occasionally encountered problems and 28% said they frequently did), followed by FLASH memory interconnects (62% occasionally and 20% frequently). Responses are shown in Figure 7.

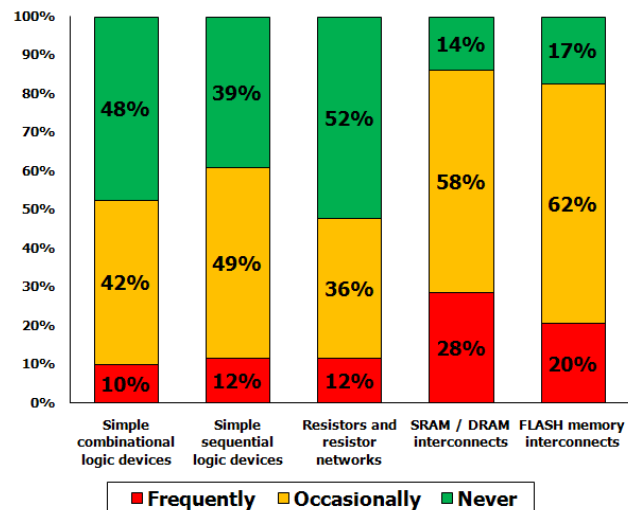


Figure 7 Frequency of Problems Encountered Using Boundary-Scan to Test Non-Boundary-Scan Devices

3.3.4 Verifying Semiconductor JTAG Compliance

Board/System Test Engineers were asked if their companies do anything to verify that the devices they receive from semiconductor suppliers are JTAG compliant.

Of the respondents, 48% replied “Yes” and 52% replied “No”. The 93 respondents who said “yes” were asked to describe the method used to verify compliance, and 70 of them provided descriptions, the majority of which can be categorized as follows:

- we verify boundary-scan functionality in the silicon during component validation;

- we verify the devices by developing production tests that use boundary-scan;
- we run a BSDL file syntax check;
- we specify compliance in our procurement contracts;
- we do DFT and/or verify boundary-scan is in data sheets.

3.3.5 Issues Encountered When Implementing Boundary-Scan

Respondents were asked what percentage of time they encountered major, minor, or no issues with boundary-scan, based on their experience with new printed circuit boards entering production. The responses were averaged and 44% had no issues, 40% had minor issues, and 16% had major issues.

The top 3 major issues reported were:

- problems related to BSDL files (non-compliant, “bad” or “wrong” BSDLs);
- non-compliant devices (devices that stray from IEEE1149.x standards);
- DFT issues.

The most common problem cited was bad BSDL files. Seventy-five percent of respondents said they occasionally had problems with bad BSDL files, and 18% said they frequently had problems. Other leading sources of problems were board design not being correctly implemented for boundary-scan, compliance issues with ICs and problems with tester or software, as shown in Figure 8.

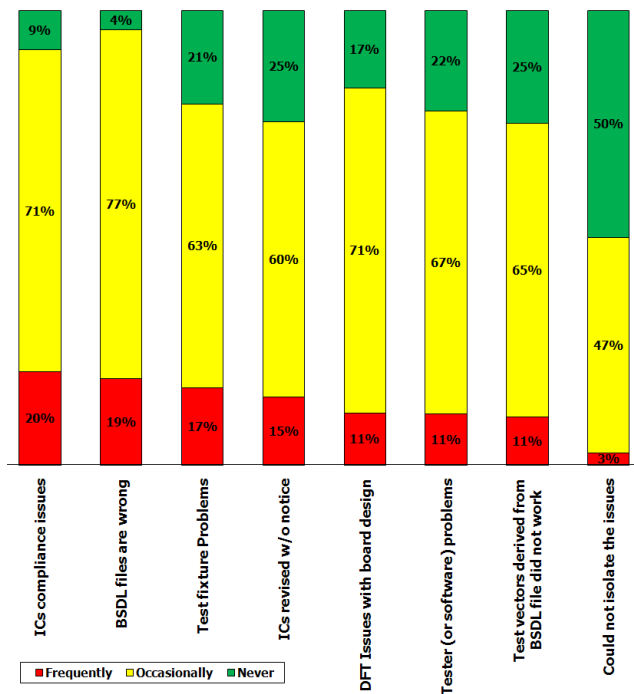


Figure 8 Frequency of Issues Encountered Using Boundary-Scan

When asked how boundary-scan issues affected them, 60% of Board/System test engineers said problems occur but are basically acceptable. Additional resources are required for success according to 25% of the respondents, 20% said they have very

few issues, and 10% question the value versus cost of boundary-scan.

When identifying issues that would prevent Board/System Engineers from using boundary-scan, the number one response was that devices don’t support boundary-scan (78%), followed by poor DFT on the board (49%). An additional 44% say they cannot get BSDLs from silicon suppliers and 12% cited concerns about potential security holes in the boundary-scan interface.

3.3.6 Attributes Important to Board/System Engineers When Choosing a Semiconductor Supplier

Board/System test engineers were asked what attributes they consider the most important in influencing the choice of semiconductor suppliers for design-for-test purposes as shown in Figure 9. This influence could be important in cases where there are choices of multiple suppliers.

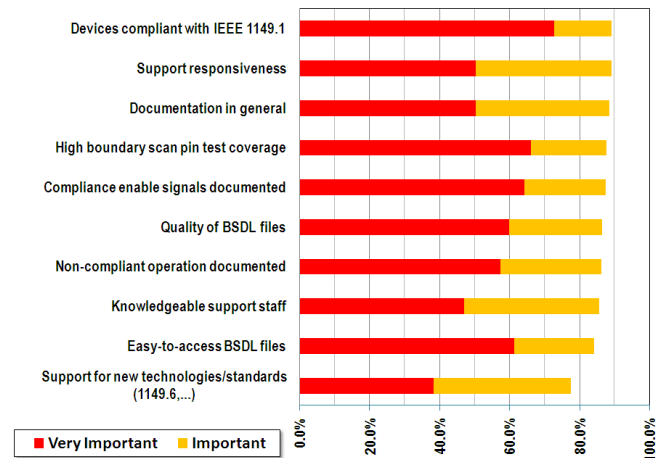


Figure 9 Attributes of Semiconductor Manufacturers

More than 80% regarded boundary-scan support features as either “Important” or “Very important” in device selection. The factors that were of greatest importance to the Board/System Test Engineers were the availability of boundary-scan cells on a high number of the device signal pins, the accuracy of the device documentation and the availability of BSDL files.

3.4 Semiconductor Engineering Survey Results

3.4.1 Current and Planned Support for Boundary-Scan in Semiconductor Devices

The survey data indicates that the general intention of many semiconductor designers is to support boundary-scan. No semiconductor engineers responded that they *never* support boundary-scan.

This information is contrary to the perception of many board test engineers that many semiconductor suppliers do not support boundary-scan. There were no respondents that indicated that they never provide a boundary-scan interface when applicable, and more than half indicated that it is always a requirement for their designs.

When asked what factors determine which pins will have boundary-scan cells attached, 61% said that they support all eligible pins and 14% said they support the most requested pins and ignore the remainder. Silicon real estate is the limiting factor for 11% of the respondents, and 7% cited library cell support.

In most cases there is an attempt to assign a boundary-scan cell to any eligible pin. Note that this does not mean that all of the device pins will receive boundary-scan cells. Other factors, such as operational speed or differential and analog signals were indicated as factors in the ability to place a boundary-scan cell.

3.4.2 Factors Hindering Successful Implementation of Boundary-Scan in IC Designs

Respondents were asked what factors would hinder implementation of IEEE 1149.1 boundary-scan in future semiconductor designs. The responses are shown in Table 5.

The problem noted most often (32%) was the lack of sufficient additional pins on the device to support the test access port. Designers and semiconductor providers are unwilling to expand package size to accommodate the four additional TAP pins required for 1149.1 implementation.

Recognizing this problem, IEEE organized the P1581 [2] standards group to devise a standard for adding combinatorial loopback in devices that are controlled by 1149.1 devices, making them slaves to the boundary-scan master devices. As a result, a P1581 device may be designed with no new pins dedicated to test mode. A P1581 device in test mode simply routes its inputs to outputs using combinational logic that allows for full shorts and opens detection in the interconnect between master and slave.

Answer Options	Response
Insufficient pins in package	32.0%
Third-party design tools too expensive	24.0%
Schedules are too tight	24.0%
Potential security holes with the boundary-scan/JTAG/TAP interface	24.0%
Other (please explain)	24.0%
Adequate pre-tapeout design verification methodologies do not exist	20.0%
Customers not asking for it/no need for it	20.0%
Boundary-scan implementation not critical path	12.0%
Not enough semiconductor real estate	12.0%
Robust design tools not available	8.0%
Excessive power consumption	8.0%
Correct boundary-scan cells not in the design library	8.0%
Boundary-scan implementation cost doesn't fit the design budget	8.0%

Table 5 Factors that Hinder Successful Implementation of IEEE 1149.1 Boundary-Scan on Future IC Designs

Cost/existence of tools to allow the designer to place boundary-scan in devices and tight schedules were cited as equal challenges.

The question of security holes that may be caused by boundary-scan was raised in this survey and has also been noted in several industry papers [3,4]. While the extent of the risk still remains uncertain, there are several methods of disabling the boundary-scan interface that can be used to mitigate that risk.

One of the original intentions of the iNEMI survey was to gauge the *demand* for the technology from users of the semiconductor

devices through design and manufacture of the end product vs. the perception of the use of that technology from those who design semiconductor devices. A significant portion (20%) of the Semiconductor Engineers participating in this survey noted “Customers are not asking for it/there is no need for it.” However, as discussed previously, 79% of the boundary-scan “users” (Board/System Engineers) said that boundary-scan was important to their production goals, and only 2% said it was not important.

Twelve percent of the respondents reported that the time needed to implement boundary-scan was not part of the design schedule. These responses were possibly common with the “doesn’t fit the design budget” response reported by an additional 8%.

In the “Other” category, the issue mentioned most frequently was that 1149.1 functionality is becoming more difficult to incorporate into high-speed/low-voltage complex I/O cells. This difficulty is a recognized problem with the use of boundary-scan. As circuits operate at higher speeds, the use of older methods, such as placing of test points for bed-of-nails test, is widely expected to become impractical. The Semiconductor Engineers’ reference to this problem indicates what has been seen by many printed circuit assembly test engineers: higher speed networks that do not have test points often have boundary-scan omitted from the devices as well.

Semiconductor Engineers were asked the same question (What would hinder implementation on future designs?) regarding IEEE 1149.6 boundary-scan. The responses are shown in Table 6.

Answer Options	Response
Customers not asking for it/no need for it	39.10%
Don't have the right boundary-scan cells in the design library	34.80%
1149.6 receiver design too complex	26.10%
Schedules are too tight	21.70%
Robust design tools not available	17.40%
Adequate pre-tape out design verification methodologies do not exist	17.40%
Insufficient pins in package	13.00%
Boundary-scan implementation cost doesn't fit the design budget	13.00%
Other (please explain)	13.00%
1149.6 specification flawed or ambiguous	8.70%
Not enough real estate on my IC	8.70%
Can't get 1149.6 third-party IP	8.70%
Excessive power consumption	8.70%
Third-party design tools too expensive	4.30%

Table 6 Factors that Hinder Successful Implementation of IEEE 1149.6 Boundary-Scan on Future IC Designs

In this case, the largest category (39.1%) was “Customers not asking for it”, indicating a perception within semiconductor engineering teams that there is no real need for the insertion of IEEE 1149.6.

The second and third most commonly stated problems were that design libraries lack 1149.6 compatible cells and the 1149.6 receiver being too complicated.

Problems with design tools and limited time on schedules were the next most commonly cited issues.

The “insufficient pins in the package” response was much less common for the 1149.6 than for 1149.1. This is most likely due to the device types requiring 1149.6 tending to be in larger packages.

In the “Other” category, the responses were similar to those for the 1149.1 question. In a number of cases, respondents referred to their comments from that section.

3.4.3 Target Applications for Semiconductor Designs

The largest target application for the respondents’ semiconductor devices was consumer and portable products, as shown in Figure 10. This is to be expected since this sector makes up the largest end-user market segment for semiconductors.

What is interesting, however, is that such a price sensitive market, (i.e., the consumer market) seems to have adopted the use of boundary-scan. This is not due to price elasticity in the end product, but is more likely an indicator of the devices containing boundary-scan not having a significant price premium.

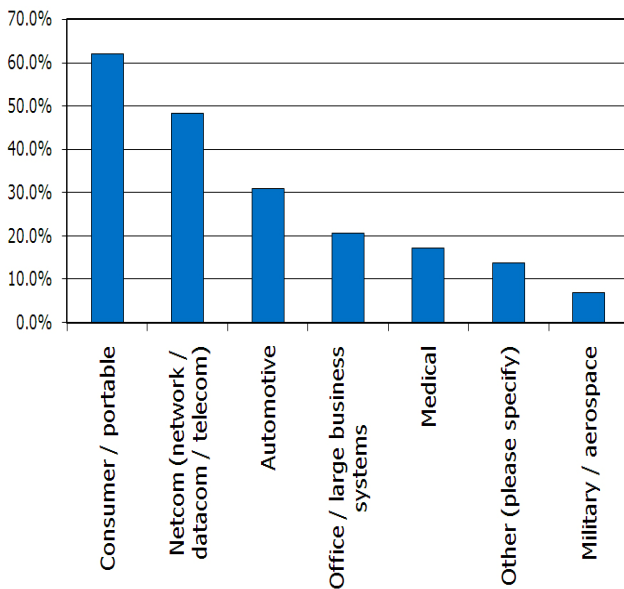


Figure 10 Target Applications for Semiconductor Designs

3.4.4 Boundary-Scan Compliance in Semiconductors

When asked what percentage of devices designed were intended to be 1149.1 compliant, more than half (53.8%) of the Semiconductor Designers replied that it was their intention to include compliant boundary-scan on all of their devices while only 7.7% responded that boundary-scan was not intended to be included. The remaining respondents reported that some percentage of devices designed would receive 1149.1 boundary-scan. The distribution of responses is shown in Figure 11.

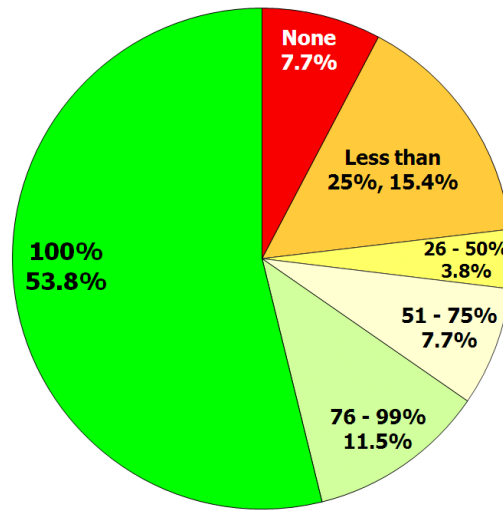


Figure 11 Percentage of Devices Designed Intended to be IEEE 1149.1 Compliant

Semiconductor designers were asked whether their group had ever intentionally developed a non-compliant boundary-scan device. Seventy percent of the respondents said “No”, 29.6% said “Yes”. Several differing reasons were given for non-compliance:

- all aspects of the 1149.x specification cannot be completely supported;
- decisions to add boundary-scan late in the design cycle force trade-offs;
- industry tools need more flexibility;
- using the JTAG interface to configure the device requires TCK to be synchronous to the system clock;
- pin signal type prohibits Boundary-scan implementation.

When asked what actions were taken when devices designed to be 1149.1 compliant were found to be non-compliant (see Figure 12), 40.7% of the respondents said they had not experienced that issue.

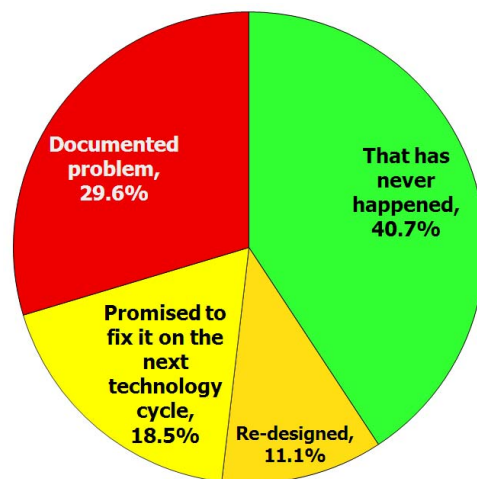


Figure 12 Actions Taken to Resolve Non-Compliant 1149.1 Devices

When problems were found with compliance, the most common solution was to provide documentation of the problem. In many cases, this documentation includes a work-around. In others, it simply states that the 1149.1 boundary-scan does not work.

Approximately 30% of the respondents said they committed to repair the issue in a future revision of the device or redesigned the device to fix the issue.

Designers indicated that their intention to develop semiconductors supporting the *IEEE 1149.6 Standard for Boundary-Scan Testing of Advanced Digital Networks*, also known as “AC Boundary-Scan.” was much lower than their intention to support the IEEE 1149.1 standard. Forty percent responded that they did not have a current requirement or expect one in the future. Thirty-three percent replied that they are currently using 1149.6. As shown in Figure 13, the remainder intends to support 1149.6 in the next six months to three years.

The 1149.6 standard is newer than the other and may be considered more difficult to implement from the perspective of available tools [5].

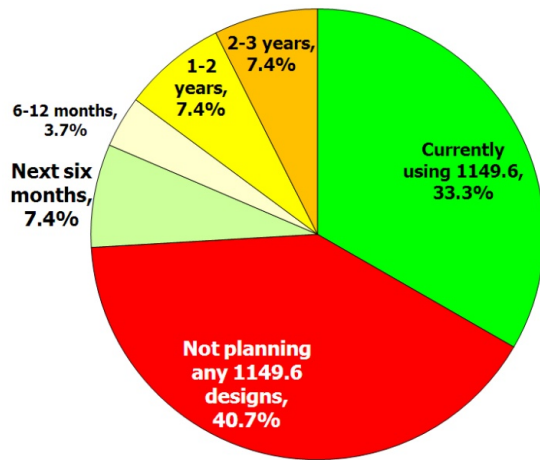


Figure 13 Current/Future Plans to Produce 1149.6 Designs

3.4.5 Boundary-Scan Verification in Semiconductors

Semiconductor Engineers were asked how boundary-scan implementation is verified before device release. All replied that they use simulation and 41% said they additionally do hardware verification.

More than half (53.8%) of the Semiconductor Engineers verify compliance of their device post-tapeout. This finds most of the problems not considered in the simulation phase.

Semiconductor Engineers were asked if their companies use synthesis and/or simulation tools for 1149.1 implementation. The results are shown in Table 7.

Answer Options	Response
Use both	70.4%
Simulation only	25.9%
Use neither	3.7%
Synthesis only	0.0%

Table 7 Use of Synthesis or Simulation Tools in 1149.1 Implementation

Respondents listed a number of commercially available simulation tools they use to verify boundary-scan insertion. These tools were the only method used by many of the designers.

When asked whether 1149.6 boundary-scan design logic was verified with verification tools, only 41.7% of those responding said “Yes”. The implementation design, simulation, and verification processes and the issues associated with them tend to be less developed with the IEEE 1149.6 standard. This standard is far newer and is earlier in its adoption cycle.

3.4.6 Availability and Use of Extended Test Functions in Semiconductors

The addition of on-chip instrumentation along with other types of built-in self-test was indicated as becoming common in semiconductors, as shown in Table 8. Possible confusion existed in this question, since it was intended by the survey creators to refer to printed circuit assembly structural test rather than that of the semiconductor device, which would be the view point of the Semiconductor Engineer.

Answer Options	Response
On-chip instrumentation	60.0%
Logic BIST	36.0%
Memory BIST	92.0%
Power management	16.0%
Other (please specify)	20.0%

Table 8 Features Beyond Basic Boundary-Scan Structural Test

In the “Other” category, respondents mentioned ARM JTAG [6] debug control, all test mode control, scan test compression, PRBS control, FLASH memory programming and on-chip debug.

Respondents were then asked if they provide customer access to boundary-scan features beyond basic structural test capability. Their responses are shown in Table 9.

Answer Options	Response
Yes	48.0%
No	40.0%
Not now but plan to in the future	8.0%
Not applicable (do not provide additional capabilities)	4.0%

Table 9 Access to Features Beyond Basic Boundary-Scan Structural Test

Even though most devices have functions such as Built-in Self-test installed, only about one-half of the Semiconductor Engineers provide either documentation or command access to those functions for use with loaded circuit board or system test.

3.4.7 BSDL Files and Confidentiality

Almost one-fifth (19.2%) of the semiconductor survey respondents said their companies considered the boundary-scan description language (BSDL) file to be a confidential document. In some cases the engineers did not know what the process was for obtaining the BSDL files. In most cases, the files were available under a non-disclosure agreement with their customer.

4. Conclusions

Clearly, boundary-scan is a very important semiconductor feature to Board/System Test Engineers. 98% of the respondents use boundary-scan and 79% rated boundary-scan as highly or mod-

erately important to their production goals. It is widely used in circuit board test and debug.

Semiconductor engineers have a good working knowledge of the released boundary-scan standards and the semiconductor industry in general supports the released standards. Based on the input of the Board/System Engineers, what can the semiconductor industry do to make things better?

First, the semiconductor industry should make a greater effort to produce correct and compliant BSDs. The number one boundary-scan issue reported by Board/System Engineers was incorrect or non-compliant BSD files.

Second, BSDs need to be easier to obtain. Almost 45% of the Board/System Engineers voiced this need.

Third, a better job needs to be done in verifying JTAG hardware compliance. Currently, many Board/System Engineers find non-compliance when they generate a test and try to implement it. This is far too late in the cycle to discover the issue!

Fourth, get involved with the P1581 working group and implement the standard in future memory devices. This will greatly assist the 80% of test engineers who today struggle to test these devices with no on-chip testability.

Finally, semiconductor industry involvement in other proposed boundary-scan standard working groups and early adoption of those standards is very important and will help fix the significant

number of issues encountered when trying to implement tests for non-boundary-scan parts.

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