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iNEMI HFR-Free Portfolio

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IMPACT, Taipei
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Outline

- Consortial Development Programs
- “Low Halogen” Definition – iNEMI Position Statement
- Overview of iNEMI HFR-Free Activities
- iNEMI HFR-Free Leadership Program
- Summary

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Consortial Development Programs

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Drivers for Halogen Free

Driver	Global Environmental Responsibility • **Bio-accumulation** • **Toxicity of flame retardants & vinyl chloride** • **Dioxins released during EOL burning** Threat of legislations Non-Governmental Organization (NGO) pressure to address environmental issues
Materials Involved	All Brominated Flame Retardants (TBBA is main FR in substrate & PCB Materials) All Chlorinated Flame Retardants and PVC
Standards **(PCB Material Only)**	IEC 61249-2-21 JPCA-ES-01-1999 IPC - 4101B

Based on current specs: Halogen free does not mean “zero halogens”

Fluorine, Iodine, and Astatine (Group VIIA halogens) are not restricted in the industry definition of “halogen-free”

Industry BFR/PVC-Free Projects

Project Title	Project Chair	Key Objectives	Expected Completion
HDPUG – Reliability of BFR/PVC-Free Notebook PWBs	Dell Wistron ITRI	Supply chain assessment of 100% BFR/PVC-Free Notebook PWBs (board + components) and reliability assessment	Results expected in late 2009
HDPUG – BFR/PVC-Free Cables	Dell	Assess a broad range of BFR/PVC-Free materials for different cable and wire applications.	Publication expected by early 2010
IPC/JEDEC – Halogen-Free Subcommittee (JP 709)	Intel Dell	Develop a new BFR/PVC-Free standard (define maximum concentration values for halogens across a variety of applications, not just PCBs)	Re-ballot failed in Q3'09
US EPA - Flame Retardants in Printed Circuit Boards	EPA	Identify and evaluate commercially available flame retardants in FR-4 printed circuit boards and their environmental, human health and safety and environmental fate aspects.	Finalize report and publicize results in late 2009
iNEMI - HFR-Free PCB Material Evaluation	Intel	Identify technology readiness, supply capability and standards development opportunities for "halogen-free" alternatives to conventional printed wiring board materials	Project completed in 2008 and presented at SMTAI
iNEMI Position paper on Low-Halogen Electronics	Dell, Intel HP, Cisco Lenovo	Provide a working definition in place of an IPC standard	Released July 1, 2009

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iNEMI Definition of “Low Halogen”

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“Low Halogen” (“BFR/CFR/PVC-Free”) - iNEMI Position Statement

- **All printed board and substrate laminates shall meet Br and Cl requirements for low halogen as defined in IEC 61249-2-21 and IPC-4101B**

  The maximum total halogens contained in the resin plus reinforcement matrix is 1500 ppm with maximum chlorine of 900 ppm and maximum bromine being 900 ppm.

- **For components other than printed board and substrate laminates: Each plastic within the component contains < 1000 ppm (0.1%) of bromine [if the Br source is from BFRs] and < 1000 ppm (0.1%) of chlorine [if the Cl source is from CFRs or PVC or PVC copolymers].**

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Overview of iNEMI HFR-Free Activities

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HFR-Free Project Portfolio

Completed projects

- HFR-Free PCB Material Evaluation

Active projects

- HFR-Free High Reliability PCB
- HFR-Free Leadership Program
  - HFR-Free PCB Materials
  - HFR-Free Signal Integrity

New initiative

- PVC Alternative Initiative

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HFR-Free PCB Material Evaluation: Completed

Project Leader
Steve Tisdale,
Intel Corporation

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HFR-Free PCB Material Evaluation

Purpose: **Identify technology readiness, supply capability and standards development opportunities for "halogen-free" alternatives to conventional printed wiring board materials**

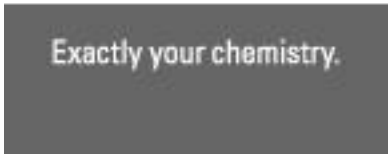
Goals of the Project:

- **Identify commercially viable materials**
- **Benchmark past work and identify critical knowledge gaps**
- **Design test vehicles and test methodologies**
- **Leveraging prior investigations, carry out the necessary testing to characterize viable materials**
- **Analyze results**
- **Publish recommendations**

Results and Benefits:

- **Determined the critical tests for evaluating halogen-free laminate materials**
- **Showed industry the general benefits and limitations of non-bromine based flame retardant laminates**
- **Participants obtained detailed knowledge of each laminate**

HFR-Free PCB Material Evaluation
Project Members



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HFR-Free High Reliability Project: In Process

Project Leader

Steve Tisdale,

Intel Corporation

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HFR-Free High Reliability Project

Purpose: **Identify technology readiness, supply capability and reliability characteristics for "HFR-free" alternatives to conventional printed wiring board materials and printed wiring board assemblies, based on the high-reliability market segment requirements (large, thick boards).**

Goals of the Project:

- **Identify commercially viable materials**
- **Benchmark past work and identify critical knowledge gaps**
- **Build on industry knowledge and capability, including the iNEMI BFR-Free PCB Material Evaluation Project**
- **Design test vehicles and test methodologies**
- **Leveraging prior investigations, carry out the necessary testing to characterize viable materials**
- **Analyze results**
- **Publish recommendations**

Status:

- **Currently in the TV build / testing phase**
- **Completion of Project in Q1 2010**

HFR-Free High Reliability Project Members

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PVC Alternatives Project

Chair:

Scott O'Connell, Dell Inc.

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Thrust Area: Environment	PVC Alternatives Project	Oct-09
TIG: ECE		

Goal: Perform an Life Cycle Assessment of the electrical and mechanical properties, and safety aspects of PVC alternatives for Power Cord Sets

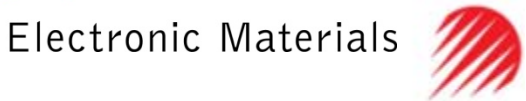
Strategy	Issues	Graphics
• Phase 1 - Develop environmental (LCA) comparing PVC with PVC-free compounds for detachable desktop US power cord sets • Phase 2 - Develop and conduct a test to gain a better understanding of the electrical, mechanical and safety aspects of PVC-free alternatives	• Industry migration to "PVC-free" materials • LCA studies can be costly and it remains to be seen if there will be a critical mass of companies who want to share the cost of performing a full LCA on various materials used in US Power Cord Sets.	
Project Lead: Scott O'Connell, Dell Inc. **Project Co-Lead:**		

Tactics	Milestones and/or Deliverables	Plan	Actual
• Phase I conduct a cradle-to-grave Life Cycle Assessment (LCA) on PVC and PVC-free Alternatives for detachable US desktop power cord sets	Research Project Information – Define and Collect Data	Month 3	
	Provide Information to LCA Consultants for formal quotes	Month 3	
	Go / No-Go Decision on LCA Study	Month 4	
	Model LCI Data	Month 5	
• Phase 2 Conduct performance testing of different PVC-free alternatives	LCA Analysis	Month 7	
	Project Reporting and Participant Training	Month 10	

Project open for sign-up by December 2, 2009.

PVC Alternatives Initiative

Formation Team Participation / Interest



Non-Member Participants	
AlphaGary	Kraiburg TPE
BASF	Lexmark
BizLink	NorthWire
Cordmaster Engineering	PE International
EarthShift	SABIC
Exxon Mobil	Teknor Apex
Hueson Wire	Underwriters Laboratories
Huntsman	Vinyl Institute
	Volex

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HFR-Free Leadership Program: In Process

Program Leader
Steve Tisdale,
Intel Corporation

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iNEMI HFR-Free Leadership Program

Consortium Objectives

1. **Identify technology readiness, supply chain capability, and reliability characteristics for "HFR-free" alternatives to conventional printed circuit board materials and assemblies**
   - **Spans electrical and mechanical properties**
   - **Includes assessing if board/system design modifications can overcome material property limitations**

2. **Define technology limits for HFR-free materials across all market segments**
   - **Initial focus is on client platforms (desktop, notebook)**
   - **Goal is to drive laminate supplier slash sheet content**

HFR-free Technology Leadership Project

Stephen Tisdale, Intel – Chair
HFR-Free Leadership Program

HFR-Free PCB Materials
(Chair: John Davignon – Intel)

HFR-Free Signal Integrity
(Chair: Stephen Hall - Intel
Co-Chair: David Senk - Cisco)

Identify key thermo-mechanical performance characteristics and determine if they are in the critical path for the HFR-free PCB material transition.

Ensure there is no degradation of electrical signals in HFR-free PCB materials, base on investigation of permittivity and loss as well as how they are impacted by moisture absorption in new HFR-free materials.

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HFR-Free Leadership Program

HFR-Free PCB Materials Project

Program Manager:

Stephen Tisdale, Intel

Chair:

John Davignon, Intel;

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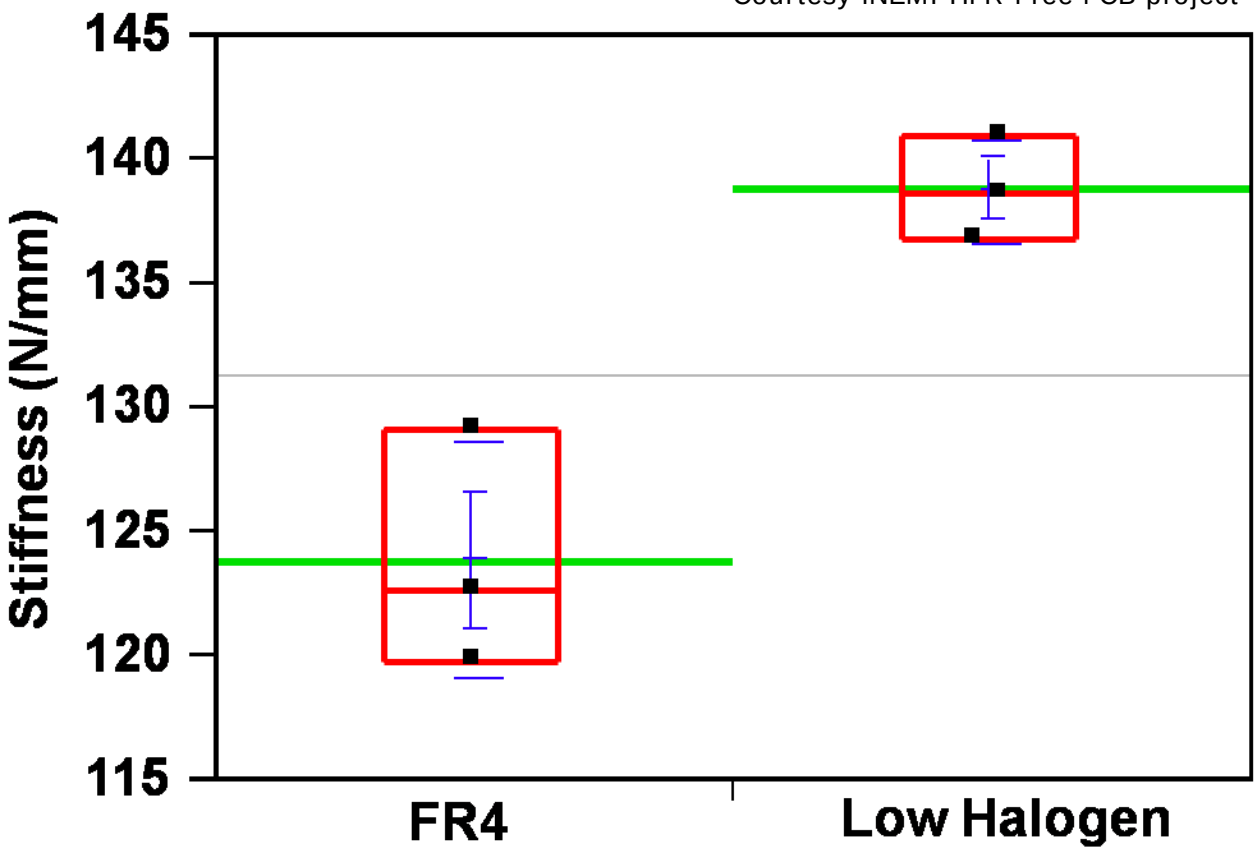
HFR-Free PCB Materials

Electronic Materials

Solder Joint Reliability

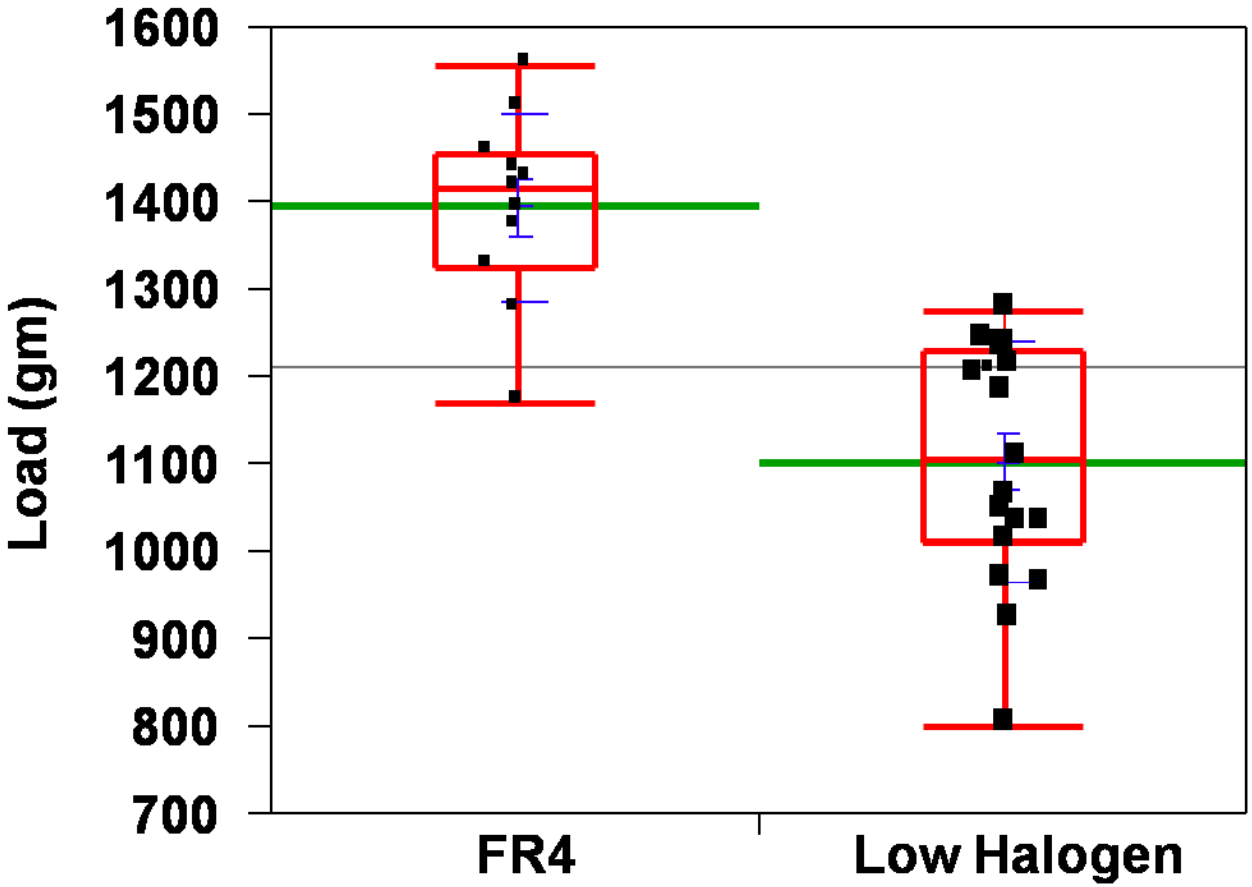
Courtesy iNEMI HFR-Free PCB project



HF is ~10% stiffer
(8 layer .062" board)

Lower mech stress limits
(higher SJR risk)

Pad Crater Performance



HF has ~20% worse cold ball pull performance

Increase pad cratering (higher rework risk)

Some parameters will have less margin!

Technical Concerns: Material Selection Summary

Mat'l	Dk	Df	H_2O Absorb	Tg	CTE	Flex	Td	T260/ Cu	T288/ Cu	Peel Strength	IST	CAF	UL94 V0	Shock	Vibe	Temp Cycle	Cold Ball Pull
A																	
B																	
C																	
D																	
E																	
F																	
G																	
H																	
I																	
J																	
K																	

Color Code

- *Equal to or better than FR4 (No issue)*
- *Marginal vs. FR4 (Issue not clear)*
- *Worse than FR4 (Clear Issue)*
- *No Data*

Derived from iNEMI WG data

Material selection can matter!

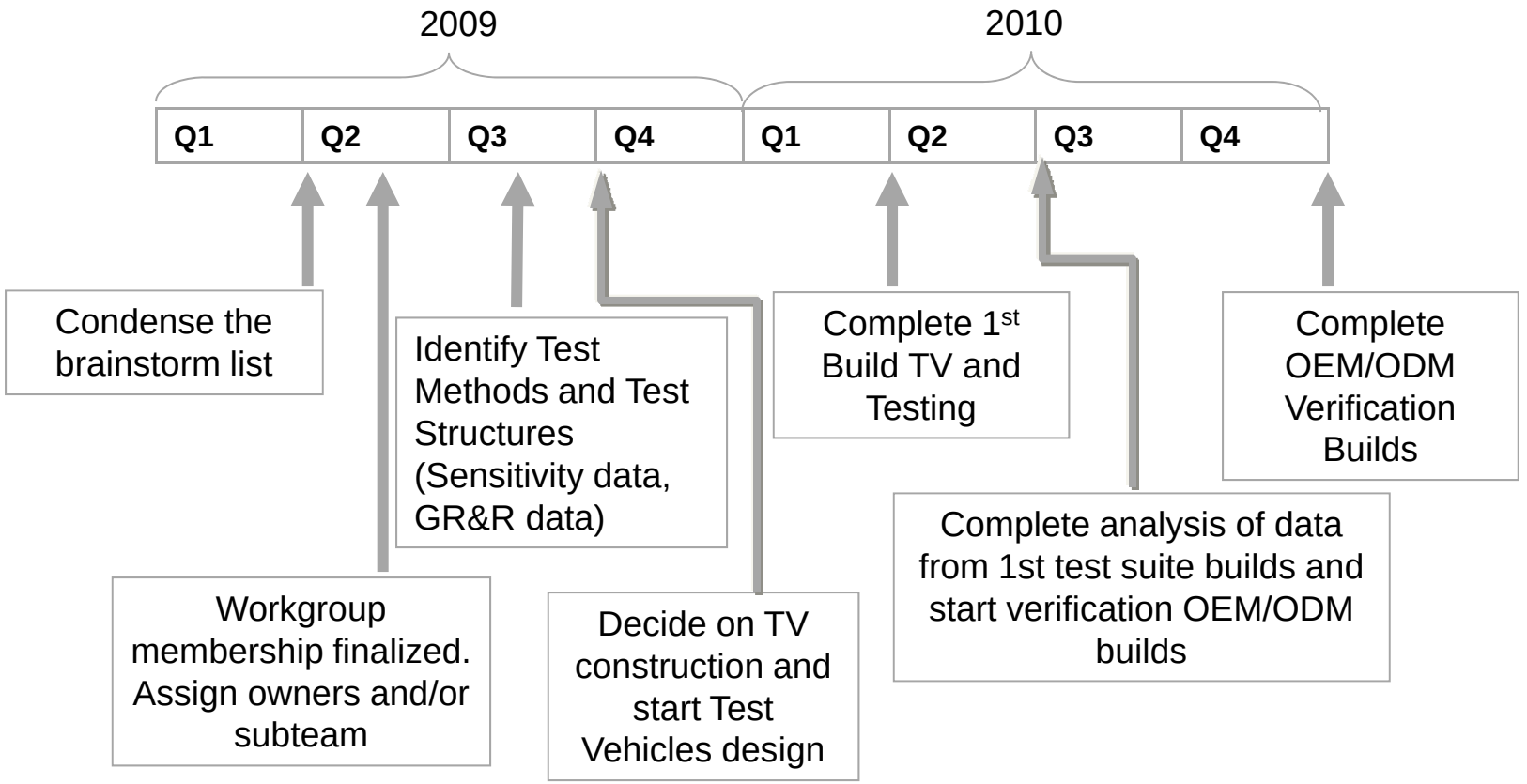
iNEMI HF PCB Materials WG Status

- **27 Areas of Concern have been defined and ranked according to a Risk or Priority of Concern**
- **Subteams have been formed to evaluated the Test Methods (TM) required to give quantifiable data on the 17 down selected areas of concern**
- **Test Methods are being finalized and all modification to existing TM documented.**
- **Two Test Vehicle constructions for the Test Suite have been ratified (.062” 6 layer for DT & .040” 10 layer for NB)**

PCB Materials Industry 27 Areas of Concerns

	Basic Materials Properties	Rating
1	Micro and macro hardness	1.7
2	Glass transition temperature (Tg)	2.2
3	Decomposition temperature (Td)	2.5
4	Moisture absorption	2.7
5	Fracture Toughness of Resin / Resin Cohesive Strenght	2.3
6	Stiffness	1.7
7	Dk & Df	2.9
8	Coefficient of thermal expansion (z-axis and x-, y-axes)	2.7
9	Flexural strength	1.9
	Thermo-Mechanical Performance	
10	Pad Cratering (brittle fracture)	2.6
11	Shock & Vibe and Drop test data	2.4
12	Transient Bend	2.1
13	Copper Pad Adhesion (CBP/Hot Pin Pull/ Shear/Tensile)	2.5
14	CAF resistance	2.8
15	Long term life prediction, such as IST or thermal shock	2.8
16	Plastic and elastic deformation characteristics	1.8
17	Co-Planarity Warpage characteristics	2.1
18	Delamination characteristics (Thermo-mech stress)	2.8
	Process/Manufacturing	
19	PCB fabrication , drill wear, lamination & desmear cycle	2.5
20	Punchability/Scoring/Breakoff Performance	1.6
	Assembly Process	
21	Lead Free Reflow Test	2.7
22	Rework (Pad Peeling)	2.6
	Other Concerns	
23	Resin system dependency/hardening/curing agents	1.8
24	Affect of Fillers	2.0
25	UL Fire ratings (V0-V1)	2.7
26	Electrical Properties (UL CTI rating)	1.5
27	MOT Maximum Operating Temperature	2.2

Proposed Timeline



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HFR-Free Leadership Program

HFR-Free Signal Integrity Project

Program Manager:
Stephen Tisdale, Intel

Chair:
Stephen Hall, Intel;

Co-Chair:
David Senk, Cisco

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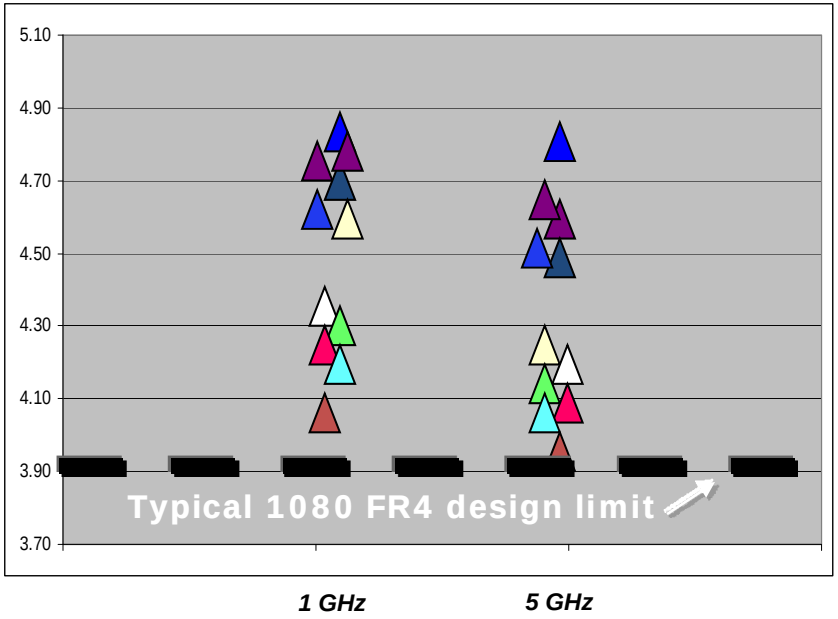
HFR-Free Signal Integrity Project

Electronic Materials

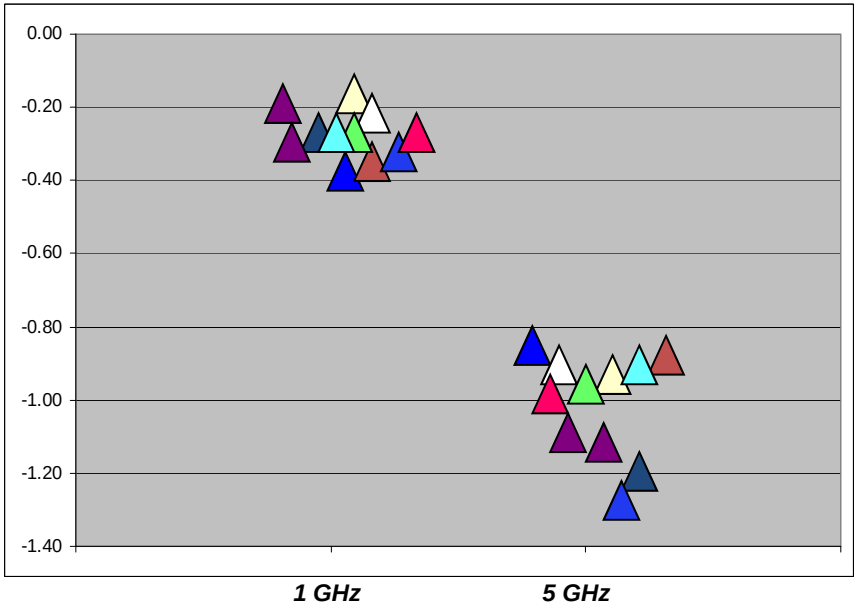
Technical Concern: HF Electrical Results

Electrical Performance

Permittivity (Dk)



Total Loss



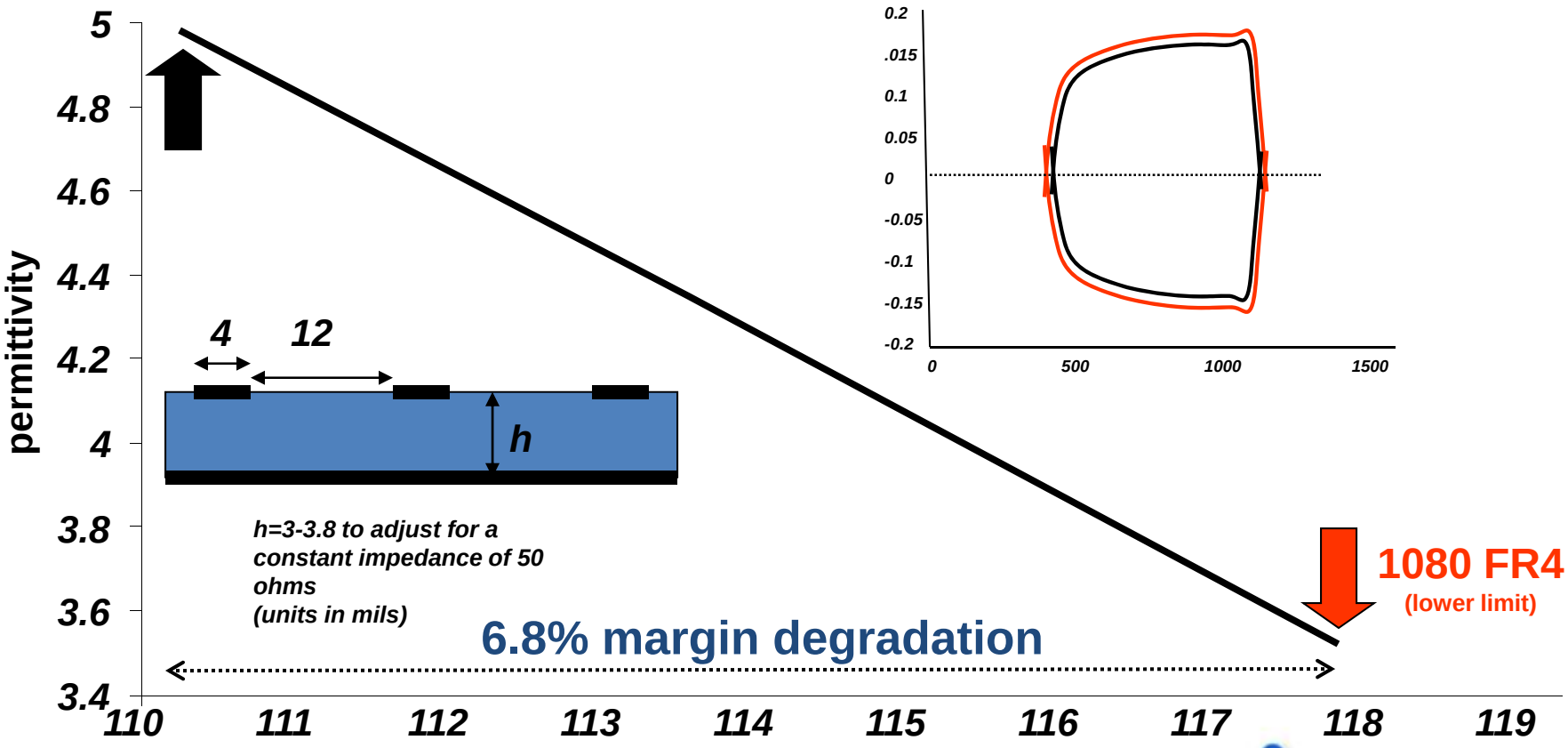
The Dk for the HF materials is generally equivalent to or higher than the control Material

The total loss for the HF materials is generally equivalent to or lower than the control material

Critical Electrical Parameters: Permittivity

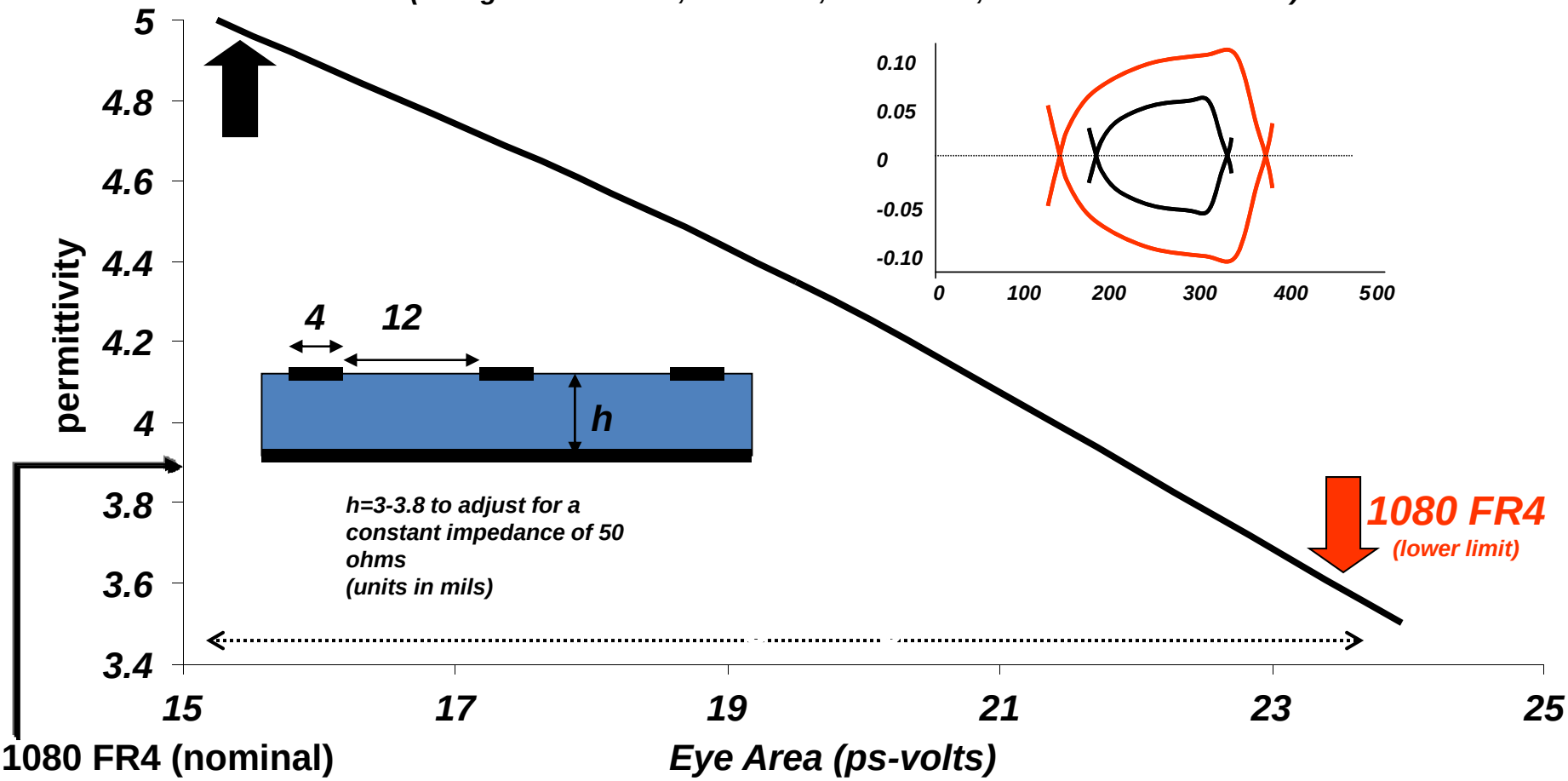
Eye area as a function of permittivity for a constant impedance transmission line at 0.667 Gbits/sec

(3 single ended lines; 10 inches; 4 mil width; 12 mils between traces)



Eye area as a function of permittivity for a constant impedance transmission line at 2 Gbits/sec

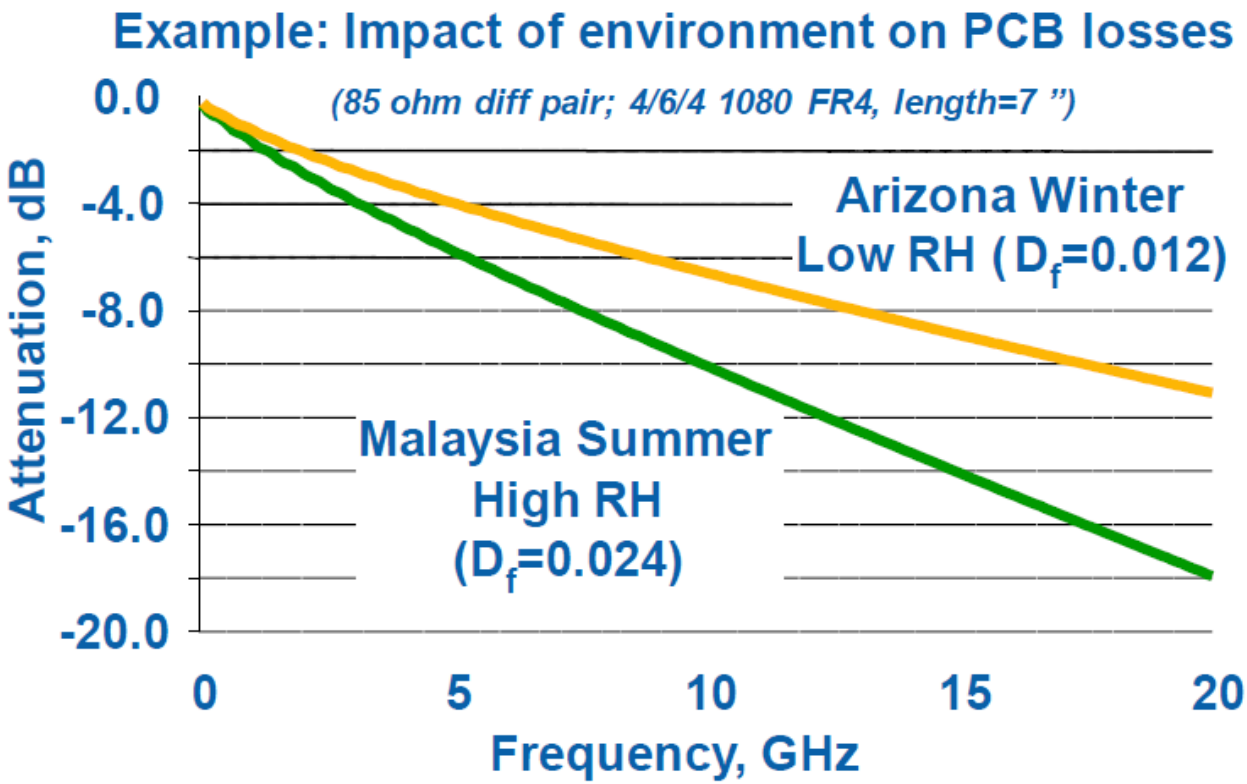
(3 single ended lines; 10 inches; 4 mil width; 12 mils between traces)



Impact of HF PCBs on bus design:

- *Increased crosstalk*
- *Reduced bus performance*
- *Increased performance degradation with bus speed*
- *More expensive designs (more layers to compensate for crosstalk)*

Critical Electrical Parameters: Loss Tangent



The loss tangent needs to be assessed at dry and humid environmental conditions to account for moisture

Goals:

- ✓ ***Assess Df limits to ensure suitability for high-speed bus design***
- ✓ ***Ensure water absorption does not increase Df more than typical halogenated materials***

Critical Electrical Parameters for high-speed deign

- ✓ **Permittivity (also known as Dk, Ɛr, or dielectric constant) dictates …**
  - Impedance
  - Crosstalk
  - Propagation velocity
- ✓ **Loss Tangent (also known as Df or tand) dictates Signal attenuation**
  - Dissipates energy as heat
- ✓ **Moisture Absorption (Specifically, how it changes Dk and Df)**
  - Significantly increases the loss tangent and the permittivity

***Problem:* Dk of widely available halogen-free dielectrics is too high**

- ***Typical FR4 w/ 1080 glass: ~3.6<Dk<3.9***
- ***HF FR4 w/ 1080 glass: ~4.0<Dk<5.2 (iNEMI data)***

Other concerns:

- Tand for HF materials must be equal to or better than FR4
- Moisture absorption must not inordinately increase Dk or Df
- Frequency response must be predictable and continuous
- New formulations may exhibit non-standard behavior

HFR-Free Signal Integrity Project Status

- **Identify:** Identify the critical electrical parameters of HFR-Free dielectric materials, set limits on those parameters ensuring suitability for high-speed digital designs

  Status: The critical electrical parameters of the dielectrics have been identified.

  - ✓ Dielectric permittivity (Dk)
  - ✓ Loss tangent (Df)
  - ✓ Moisture absorption (specifically how it affects Dk and Df)

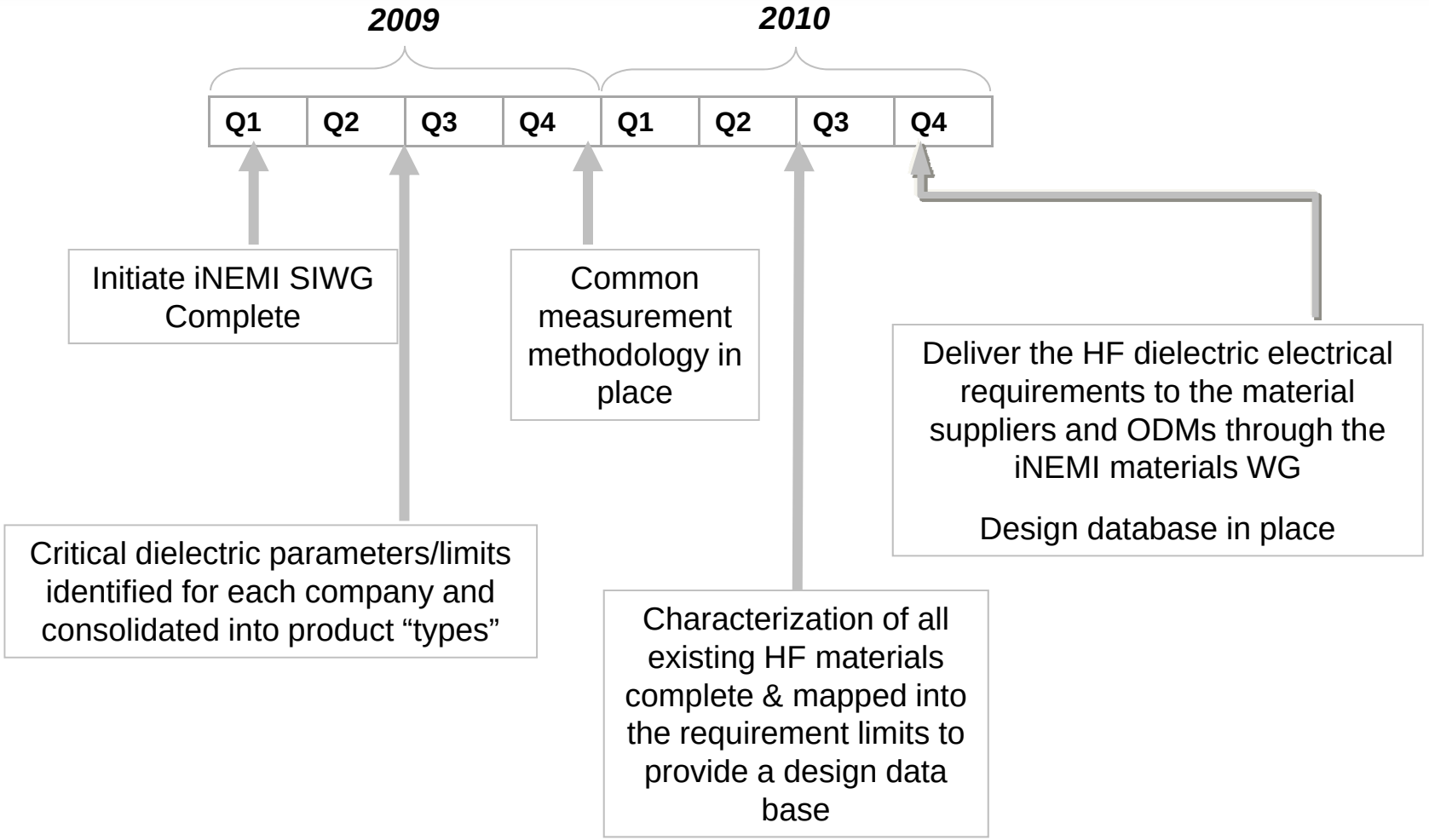
- **Characterize/Limit:** Develop a common measurement methodology that will ensure consistent and accurate evaluation of the electrical parameters of the dielectric and allow apples-apples comparison of the industries HFR-Free materials and map the properties into the performance envelopes to create a design database

  Status: The measurement methodology for comparing the electrical dielectric properties has been developed by Cisco. Validation of the method is currently underway. The material suppliers have agreed to use this method for benchmarking the permittivity and loss tangents reported on the datasheets.

- **Communicate:** Develop and communicate the HF dielectric requirements to the PCB material suppliers to drive volume up and cost down

  Status: Working with HF PCB Materials Team to communicate with Suppliers

Timeline



Emerging buses are more sensitive!
Timeline 2011-2012

Summary: Technology Challenges of HFR-Free

- **Mechanical Properties**
  - **HF materials are ~10% stiffer (8 layer .062” board)**
  - **Lower mechanical stress limits (higher SJR risk)**
    - **HF has ~20% worse cold ball pull performance**
    - **Increased tendency for pad cratering**
    - **Higher rework risk**

- **Electrical Properties**
  - **HF materials have broader range of Permittivity (Dk) values**
    - **Reduced margins for high speed busses**
    - **Especially critical for next generation (e.g. DDR3)**

Closing Thoughts

- **Conversion to Pb-Free Solders has demonstrated:**
  - **The need to select and develop the technology and verify its reliability**
  - **The need for the entire supply chain to be involved**
    - Segments driving the change
    - Segments that may be impacted by the change
  - **The need to develop a conversion time line for each class of products**
- **The Voluntary adoption of HFR-Free Technology will require:**
  - **All of the above**
  - **Verifying the design and electrical performance**
  - **Each Class of Products working with its supply chain to insure successful planning and execution of the conversion**

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