HFR-Free Leadership Program

Program Manager:

Stephen Tisdale, Intel

HFR-Free Signal Integrity

Chair: Stephen Hall, Intel
Co-chair: David Senk, Cisco

HFR-Free PCB Materials

Chair: John Davignon, Intel

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IMPACT, Taipei

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Agenda

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- *PCB Material WG*
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  - *Areas of Concern / Methodology*
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  - *Areas of Concern*
- *Summary*
  - *Project Status / Timeline*

Problem Statement

- **Many of the HF laminates on the market have shown a reduction in performance margin from the FR-4 laminates being used today**
- **This margin loss is in both the thermo-mechanical and electrical performance**
- **The critical electrical properties of available HFR-free dielectrics make high-speed bus design problematic without increasing the cost of the system**
- **The flame retardants currently used vary among manufacturers, resulting in wider fluctuation of vendor to vendor PCB electrical performance compared to FR4 designs**

iNEMI HFR-Free Leadership Program

Consortium Objectives

1. Identify technology readiness, supply chain capability, and reliability characteristics for "HFR-free" alternatives to conventional printed circuit board materials and assemblies
   - Spans electrical and mechanical properties
   - Includes assessing if board/system design modifications can overcome material property limitations

2. Define technology limits for HFR-free materials across all market segments
   - Initial focus is on client platforms (desktop, notebook)
   - Goal is to drive laminate supplier slash sheet content

HFR-free Technology Leadership Project

Stephen Tisdale, Intel – Chair
HFR-Free Leadership Program

HFR-Free PCB Materials
(Chair: John Davignon – Intel)

Identify key thermo-mechanical performance characteristics and determine if they are in the critical path for the HFR-free PCB material transition.

HFR-Free Signal Integrity
(Chair: Stephen Hall - Intel
Co-Chair: David Senk - Cisco)

Ensure there is no degradation of electrical signals in HFR-free PCB materials, base on investigation of permittivity and loss as well as how they are impacted by moisture absorption in new HFR-free materials.

iNEMI HF PCB Materials

Chair: John Davignon, Intel

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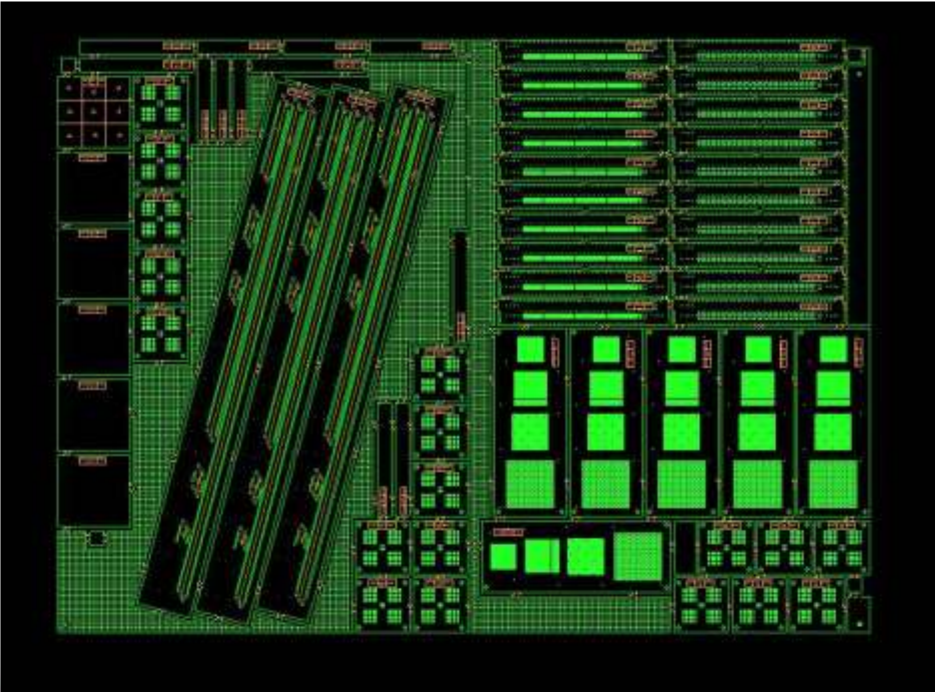
iNEMI HF PCB Materials WG Strategy

- Define and implement quantifiable data into the HF Laminate Suppliers Datasheets that will assist in material selection by users.
- Define a "Test Suite Methodology" which meets the quality and reliability requirements of the chosen market segments
- Ensure the Industry Laminate Suppliers have the capability and capacity to support the industry HF laminate requirements

Test Suite Methodology

Test Methods Under Evaluation		
Glass Transition Temperature (Tg)		Stiffness/Flexural Strength
Decomposition Temperature (Td)		Pad Adhesion (CBP/Hot Pin Pull)
Coefficient of Thermal Expansion (x,y,z)		Interconnect Stress Test (IST)
Moisture absorption		Conductive Anodic Filament (CAF)
Rework (Pad Peeling)		Lead Free Reflow Test: Delamination
Permittivity (Dk)		Charpy Impact Test
Total Loss (Df)		Simulated Reflow Test



10 Layer Mobile Stack-up

	Description	Layer Type	Thickness	
Layer 1	Plated 1/2 oz Cu		1.6	mils
	Prepreg		3	mils - 1 ply 1080
Layer 2	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 3	Unplated 1 oz Cu		1.3	mils
	Prepreg		4.2	mils - 1 ply 2116
Layer 4	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 5	Unplated 1 oz Cu		1.3	mils
	Prepreg		4.2	mils - 1 ply 2116
Layer 6	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 7	Unplated 1 oz Cu		1.3	mils
	Prepreg		4.2	mils - 1 ply 2116
Layer 8	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 9	Unplated 1 oz Cu		1.3	mils
	Prepreg		3	mils - 1 ply 1080
Layer 10	Plated 1/2 oz Cu		1.6	mils
			48.2	

Benefits of the Consortia

- We are changing the way that data is reported on the Laminate datasheets.
  - The test methods will be precisely defined
  - The test methods will be performed on a "product like" construction for more relevant data
- The data reported will enable:
  - A true comparison of material properties and responses between laminates
  - OEM/ODM's to set envelopes for the material properties based on the market/BU sector that mitigate risk factors for that sector
  - PCB Designers to pick cost effective laminate materials that are suitable to their products/market segment
  - Method of directing Laminate Suppliers how to improve laminates by specific properties or responses

iNEMI HF Signal Integrity WG

Chair: Stephen Hall, Intel
Co-Chair: David Senk, Cisco

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iNEMI HF Signal Integrity WG Strategy

Identify HFR-free electrical “envelopes” required by each company in the consortium

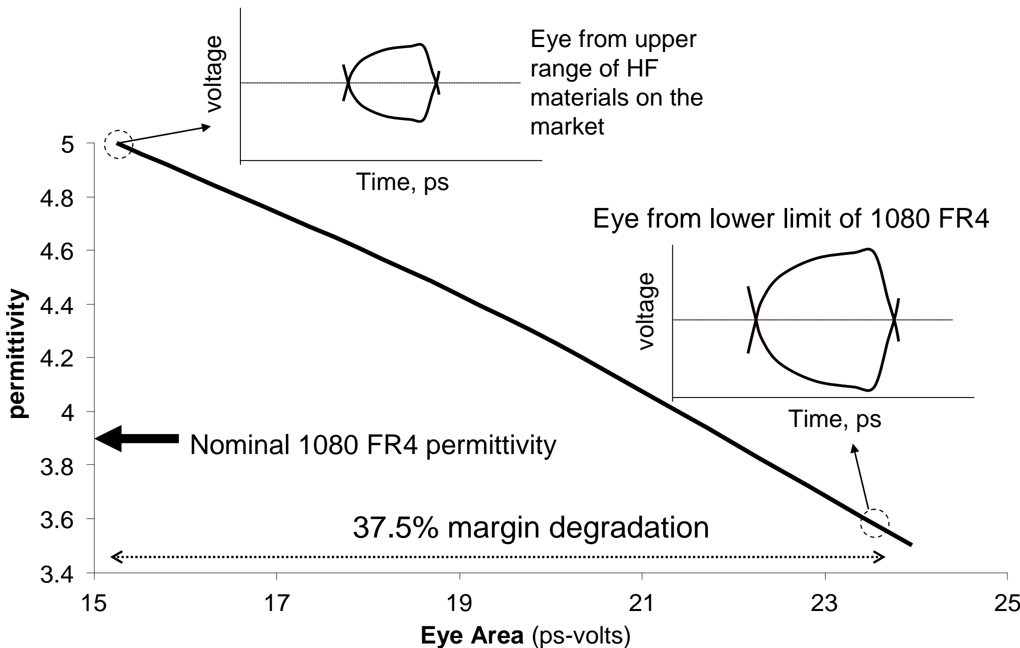
Develop a common measurement methodology

Characterize available HF dielectrics & map into requirements

Communicate requirements to the material vendors so they know what the industry wants

Performance of HF PCB vs. FR4

- ✓ **HFR-free PCB materials on the market tend to have higher permittivity (Dk) values than FR4**
  - ✓ HFR-free Dk ~ 4.2 – 5.0 (1080)
  - ✓ FR4 Dk ~ 3.6-3.9 (1080)

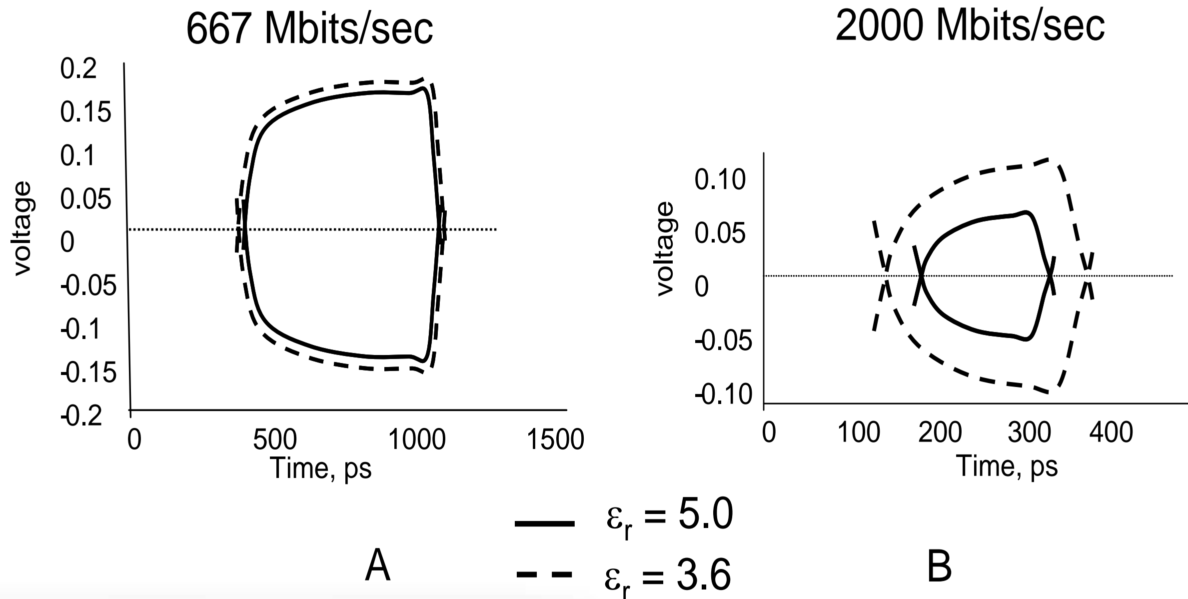


Simulation of three coupled 10" 50Ω microstrip lines; dielectric thickness varied to maintain Z_o; layout rules similar to DDR buses (W/S/W=4/12/4)

- ✓ **Higher permittivity (Dk) reduces bus performance**
  - Thicker layers for same Z_0 increases crosstalk
  - High crosstalk drives increased trace separation & more layers (increased cost)
- ✓ **HFR-free losses tend to be better than FR4 & help compensate for crosstalk for some buses**

Scaling HFR-free bus speeds

✓ **Margin reductions gets *worse* for faster buses**
- HFR-free materials with high permittivity may be adequate for lower speed buses, but can be problematic at higher speeds
- FR4 also places limitations on high-speed buses, but HFR-free exacerbates problems on crosstalk dominated buses like DDR
- HFR-free PCBs can make it more difficult for buses to scale with Moore's Law



Simulation of three coupled 10" 50Ω microstrip lines with layout rules similar to DDR buses (WSW=4/12/4)

Critical Electrical Parameters

✓ **In addition to Permittivity, other critical electrical parameters of HFR-free materials must be assessed**

- Each new formulation of flame retardants will have unique electrical parameters → non-standard electrical behavior
- Must ensure all critical electrical parameters remain within acceptable bounds

Parameter	Other names	Design influences
Permittivity	**Dk, ε_r, dielectric constant**	**Characteristic impedance, Propagation velocity, crosstalk**
Loss tangent	**Df, tanδ, dissipation factor**	**Signal attenuation**
Moisture absorption	**Environmental effects, humidity**	**When dielectric materials absorb water, Dk & Df increase.**

iNEMI HFR-free Leadership Project

Summary

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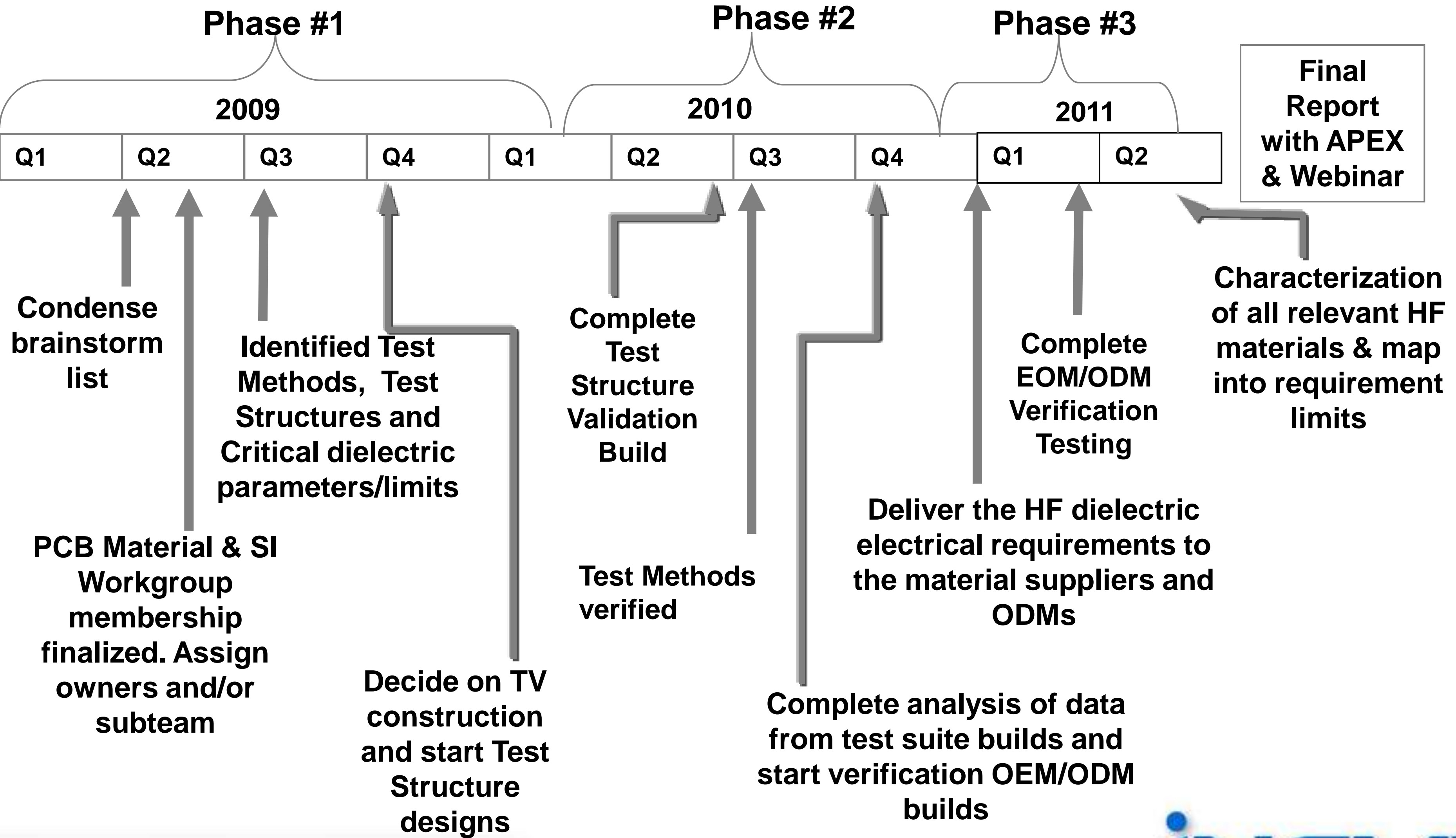
iNEMI HF-Free Leadership Consortia Status

- The initial Test Methods, Test Structures designs, Test Vehicle lay out and construction for the Test Suite Methodology have been completed and in the process of being validated
- Nine different Laminate materials have been chosen for the evaluation (6 HF and 3 FR-4 baseline)
- The Proof of Concept Test Suite validation builds completed
- Common measurement method developed by CISCO to characterize the critical parameters (S3 method)
- Analysis of data underway to validate Test Methods and associated Test Structures, including repeatability and reproducibility at 3 test houses
- Plans in place to complete Phase #2 TV builds, test and data analysis by the end of Q4'10
- Validation of the S3 method currently under way
  - S3 measurements compared to split post resonator measurements (SPR assumed to be the golden standard for accuracy)
  - Initial results show adequate accuracy for Dk, Df evaluation ongoing
- Round robin initiated to get Lab-Lab variation, 7 companies to act as "test houses" for the evaluation of the HFR-free materials

Proposed Timeline



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Summary

- **HFR-free dielectric materials on the market today have higher permittivity than FR4**
- **HFR-free PCBs come at a cost**
  - Reduced bus margins (especially on DDR)
  - Increased difficultly in speed scaling
  - Possibly increased layer count leading to more $$$$
- **Limits can be placed on the permittivity so that FR4 and HFR-free PCBs are interchangeable for a single design**
- **The HFSIWG is currently evaluating many HFR-free materials on the market to create a data-base for member companies to design with**

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Discussion