Built In Self Test (BIST) Survey - An Industry Snapshot of HVM Component BIST usage at Board and System Test

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Abstract

With board and component technology and integration rapidly increasing and becoming more complex, the testing of boards standalone and in a system is becoming more difficult, time consuming and costly. This paper addresses integrated circuit (IC) Built In Self Test (BIST) usage at the board and system test levels to provide increased test coverage, reduced test time and cost.

This paper presents the results of an IC BIST usage survey developed by the International Electronics Manufacturing Initiative (iNEMI). The survey was intended to gauge the current adoption rate of IC BIST for board and system test, identify any impediments to widespread use, and select areas for future research.

1. iNEMI BIST Project

The 2009 iNEMI Roadmap gap analysis [2] determined that one of the greatest risks to High Volume Manufacturing (HVM) board test was the continuous erosion of testpoint access due to increasing bus speeds, higher densities and shrinking form factors. Ultimately, the In-Circuit Tester (ICT) will not deliver the necessary defect coverage required, despite the complementary efforts of Boundary Scan [1]. Integrated Circuit (IC) BIST could be an alternate solution to ICT and provide the necessary defect coverage and diagnostics, independent of test point access. Running IC BIST at the board level, also gives added coverage and reduced test and debug time. Accordingly, the iNEMI BIST project [3] was launched to look at the feasability of running IC BIST at board and system test, how well existing standards support it and whether recommendations should be made for new standards.

The first phase of the iNEMI BIST project was to create and deploy a survey to the electronics industry to gauge the current use of IC BIST in HVM board and system level testing. The objective was to understand existing IC BIST availability, how much it is used at the board and system levels and the current challenges. The survey also covered whether the industry thinks there is a future in running IC BIST at board and system test, and what would enable its wider adoption and ease of use.

Follow on phases of the project are planned to address the issues identified by the survey and promote the adoption of BIST at board and system test.

2. The iNEMI BIST Survey

2.1. Survey Objectives

The objectives of the BIST survey were as follows:

- Find out what types of component BIST are used and what is available to run at the board and system levels.
- Determine whether component BIST tests are proprietary to the company that designed them.
- Understand how component BIST tests are accessed at the chip and board/system levels.
- Gather feedback on how effective component BIST tests are at catching defects at the board level.
- Find out how many component BIST tests are currently used in board and system level test and whether there are any roadblocks to their use at these test steps.
- Obtain data on how much the industry is relying on BIST as a future test technique and what coverage is expected.
- Finally, gather data the extent on which current test standards are being used or will be used.

2.2. Survey Methodology

The BIST survey was developed by the iNEMI BIST working group members and was sent out to several industry mailer lists from December 2009 to January 2010.

2.2.1. Survey Recipients

It was determined that the survey should focus on two primary job function areas. The first group's job function was the 'End Users' (EU) of BIST, which includes application development engineers for system-level BIST. The second group's job function was that of Integrated Circuit (IC) BIST provider and BIST test development. Each group brings it own unique perspective to designing and implementing component BIST.

The 'End Users' of BIST included the following functions:

- Printed Circuit Board (PCB) circuit designer, layout and routing engineers.
- PCB Design for Testability (DFT) engineer doing PCB design to manufacturing testability.
- PCB Test Engineer responsible for the design, implementation and maintenance of tests used in the manufacturing process for PCBs.
- System Architect who defines the basic structure and core design features of a system.
- System-level Application Engineer, who defines, evaluates and integrates system-level concepts.
- Manufacturing Test Engineer who writes board/system manufacturing tests and runs production testing.
- Field Service Engineer who installs, repairs and performs preventative maintenance at customer sites.
- Service and Support Engineer at a service center or repair depot.

- Test Equipment Provider working for a company that designs and sells test equipment for systems test.

IC BIST providers and test development included:

- ASIC designers responsible for IC design.
- FPGA/DSP chip designers and application engineers.
- BIST IP solution provider of BIST solutions as IP for ASICs to enable testability.
- IC test engineer who develops IC test program for verification and manufacturing test.
- Test equipment provider of IC ATE for IC verification and manufacturing test.
- EDA software tool provider of CAD software tools for IC design, verification and test generation.

2.2.2. Survey Content

The survey was structured into three sections. The first section consisted of general information. This was the company's primary business, company's annual sales, product sector where the respondents have BIST experience and respondent's primary area of responsibility (BIST End User , IC BIST Provider or IC Test Engineer.)

All respondents were asked to answer the questions in the general information section. Depending on their job area the respondent was then directed to either the End User section or the IC section.

The second section for IC BIST poviders and test engineers comprised twenty questions. The second section for End Users had the same twenty questions as for the IC section, plus three more specific to the End Users job function. The 'IC' and 'EU' replies were split out to be able to look for trends in the data per job type. The questions in the second section covered the following topics:

- Types of IC BIST used, and whether they can be run at the board level.
- Details of who provides IC BIST to the respondent's company.
- Whether the BIST tests are proprietary.
- The access method of the BIST tests at the component and board/system levels.
- The percentage of PCBs having IC BIST that can be used at the board level.
- The reasons why IC BIST is currently used for the board and system level testing, and what IC BIST might be used for in future testing.
- The types of IC BIST that are currently used at the board and system levels and how effective those tests are.
- Test steps where IC BIST is used.

The third section of the survey looked at the future usage of IC BIST at board and system test and whether respondents see it as critical for future test coverage. Infomation around the use of exsiting standards and future standard requirements was also gathered, to help set the direction for Phase 2 of the iNEMI BIST project. This section's questions covered:

- IC BIST's criticality for future coverage and fault isolation.
- Whether IC BIST along with boundary scan, is seen as replacing some of the diminishing test point access of in-circuit testing of assembly defects.
- Problem areas encountered in running IC BIST at the board and system levels.
- Adoption of current standards such as IEEE 1149.7 [5] and P1687[4].
- Whether standardization is needed for IC BIST and its application at the board level.

3. BIST Survey Results

3.1. Respondent Statistics

A total of 210 people responded to the survey. The demographics of the respondents are presented in this section.

Figure 1 shows the primary business of the respondents' companies, with over half coming from the network/datacom and consumer industries.

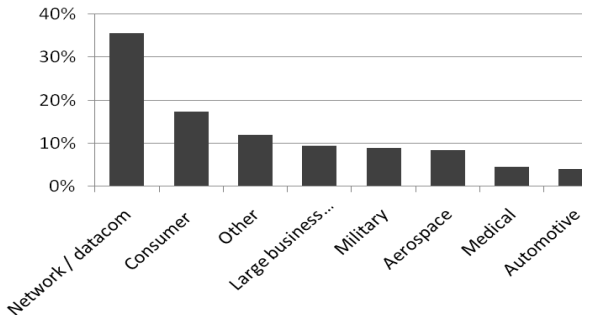

Figure 1 Primary business of the respondents' companies

Figure 2 shows the overall industry sector breakdown. The majority of respondents came from OEMs (Original Equipment Manufacturers).

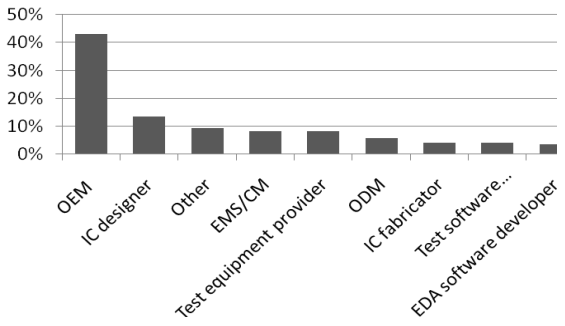

Figure 2 Industry sector breakdown of respondents

The companies' sizes in annual sales broke down as:

- 67% were greater than $500 million
- 11% were in the $100-$500 million range
- 9% were in the $10-100 million range and
- 13% were less than $10 million.

The job function breakdown for all respondents is shown in Table 1. The majority (72%) were BIST End Users.

Table 1 Respondent Job Functions

Job function	Response
BIST End User (EU)	72%
IC BIST provider and test (IC)	28%

3.2. Results for BIST availability and Access

The first questions in the survey were to find out which types of IC BIST were most commonly used and available to run at the board level. Questions then asked whether the IC BIST tests were proprietary to the company and what was the primary access method for these tests. Answers to these questions were needed to get a general idea of how much BIST is available to be run at the board level and if there are any 'show-stoppers' to IC BIST being run there.

Figure 3 shows the responses from both groups (EU and IC) regarding the types of IC BIST available at the component level. Internal memory BIST, logic BIST, high-speed IO/SERDES BIST and chip ID were most commonly cited as being available for IC test.

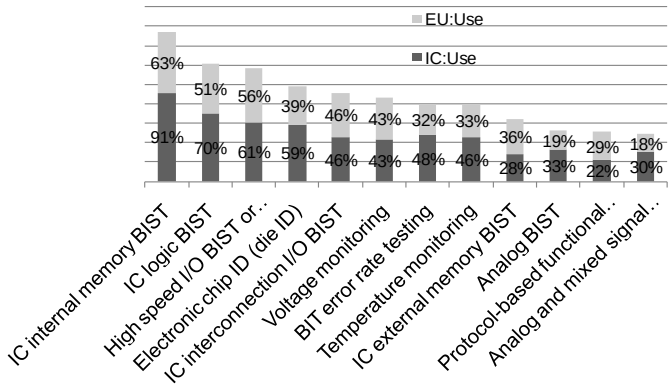

Figure 3 IC BIST availability at the component level

A follow-on question asked which types of BIST were available to run at the board level. The respondents' replies (Figure 4) indicate there is good availability, with the End Users being more optimistic about running BIST at the board level than the IC respondents. The questions represented in Figures 3 and 4 assume component-level stuck-at-fault, transition fault and path delay tests are run at component test and will not be run at the board level.

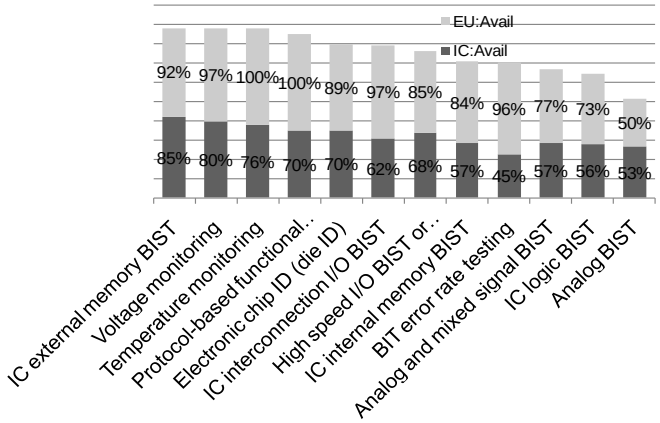

Figure 4 IC BIST tests available at the board level

It is important to understand who the IC BIST providers are so that if any changes in standards relating to protocol are necessary, the target audience that needs to be informed is known. As shown in Figure 5, most BIST is designed in-house, with 'third party IP providers' and 'commercial IC providers' being the second and third BIST providers respectively.

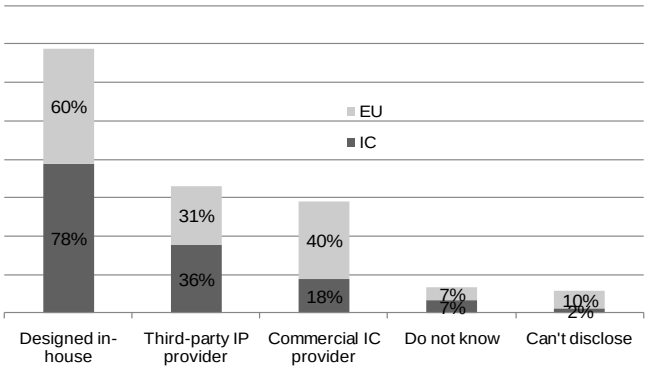

Figure 5 BIST IP providers to the respondent's company

Often companies IC BIST tests are their own IP (Intellectual Property) and as such may be proprietary. If this is the case, it could impede IC BIST adoption at board and system test. The responses to the question "Are BIST tests proprietary?" are given in Figure 6. This shows that the majority of BIST tests are proprietary and therefore any new tools and use models to allow BIST to be run at the board level will need to protect the IP.

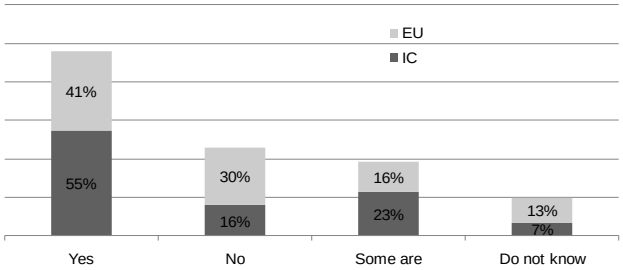

Figure 6 Are component BIST tests (IP) proprietary?

Another possible issue slowing the adoption of BIST at the board level could be the consistency of IC BIST design and implementation across products within a company. Figure 7 shows there is a major difference of opinion between the 'IC' and 'End User' respondent answers. The 'IC' believe there is consistency, however the 'End Users' see inconsistencies from the board level point of view.

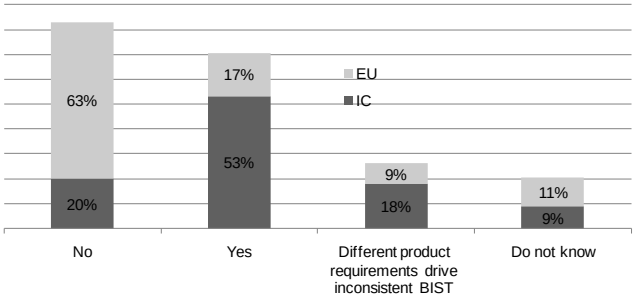

Figure 7 Is IC BIST design and implementation consistent across products?

A third impediment to BIST running at the board level could be how it is accessed. The question "How is BIST accessed at the board level?" was asked to assess whether access might be standardized. Figure 8 shows the majority are accessible by IEEE 1149.1 Test Access Port (TAP) [8]. This is good as most BIST is already following an existing standard.

The BIST is also accessed in other ways, such as POST (Power On Self Test), as part of the application, etc.

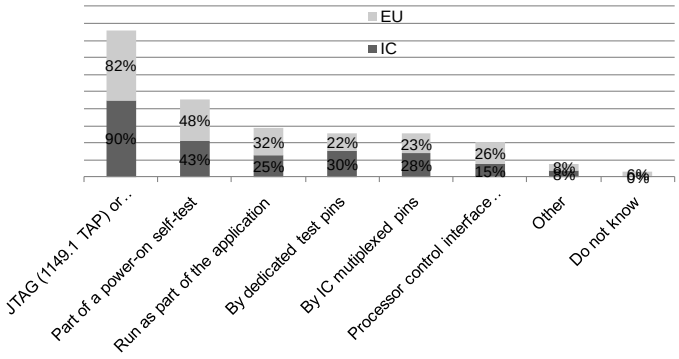

Figure 8 How is BIST accessed at the board level?

In order to drive standardization across component and board level test, the question "If BIST is able to run at the board level, is the access the same for IC and board level test?" was asked. The majority replied that it is the same, (Figure 9) although some different access mechanisms will be required at the board level, as shown by the responses in Figure 8.

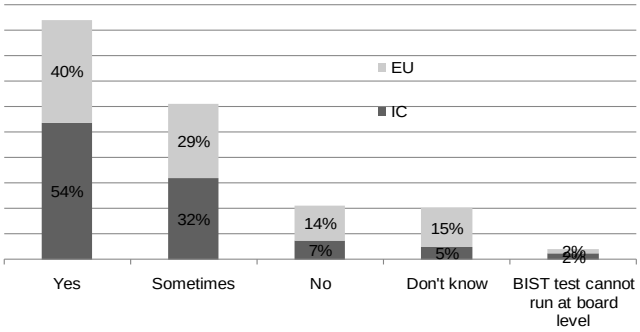

Figure 9 if BIST is able to run at the board level, is the access the same for IC and board level test?

The final question in this section "Are Board designers requesting access to IC BIST?", showed that 63% of board designers are requesting it, with internal memory BIST, logic BIST and Pseudo Random Binary Sequence (PRBS) / Input/Output BIST (IOBIST) being the most requested. The reason why some board designers are not requesting it is because they are not familiar with it, DFT is not their primary responsibility, or they have other test solutions available.

3.3. Results for BIST usage in Board and System Test

This next section looks at how much and which types of BIST are currently used at the board and system test levels. Questions also asked about the reasons for using BIST, how effective BIST is seen to be and any problems encountered running it. Data on the estimated coverage is also presented.

The first question was on the estimated number of PCBAs (Printed Circuit Board Assemblies) within the respondent's company that used board level IC BIST. The majority of End Users requesting IC BIST (see the final question in section 3.2 above) say that greater than 60% of their boards used IC BIST, as shown in Figure 9. The majority of End Users not requesting IC BIST either did not know how many boards use IC BIST or estimated only 5% to 20% use it. The replies from the IC respondents were also optimistic, with the majority stating that greater than 60% of PCBAs use component level BIST.

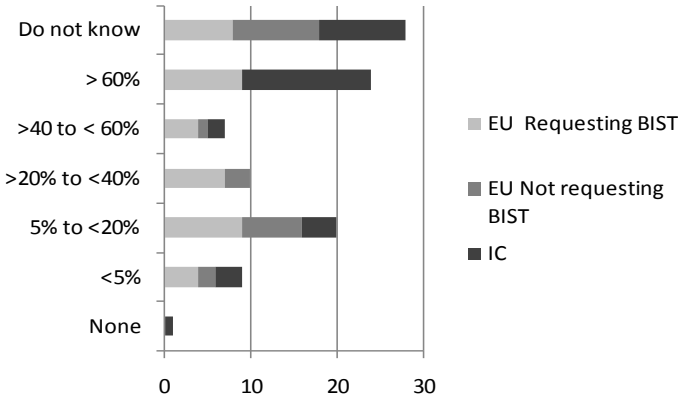

Figure 9 Percentage of PCBAs estimated to have IC BIST that is used at the board level.

The next question asked why IC BIST is currently run at the board/system levels and the reasons for its use in the future. The top reasons for it currently run were:

- Reduces manufacturing test time and cost
- Simplifies the test environment
- Provides at speed testing
- Design validation
- Resolves test access issues for high density PCBAs,

Respondents also would like to use BIST more in these areas:

- Programming it to meet various test requirements
- More coverage for board and system defects
- Debugging defects more effectively
- Yield improvement.

In the future, respondents said they would like to use it in these areas:

- Reuse in the field for maintenance and debug
- To resolve problems of signal integrity
- To measure performance

Reuse in the field shows the value of component BIST can be extended throughout its product life cycle.

The types of IC BIST actually run at the board level (compare to Figure 4 that shows component BIST available but not necessarily run at the board level) are given in Figure 10 below. This shows many types of BIST are run at the board level, with internal memory and IOBIST being the most common.

Having established the types of BIST being run at the board/system levels, the next question was "At which test steps is it used?" The replies in order of 'most used' test steps to 'least used' were:

1. IC prototype test
2. PCBA functional test
3. Product development debug
4. Product System test
5. PCBA ICT
6. PCBA repair test
7. In-field maintenance and diagnostic test
8. Product environmental test

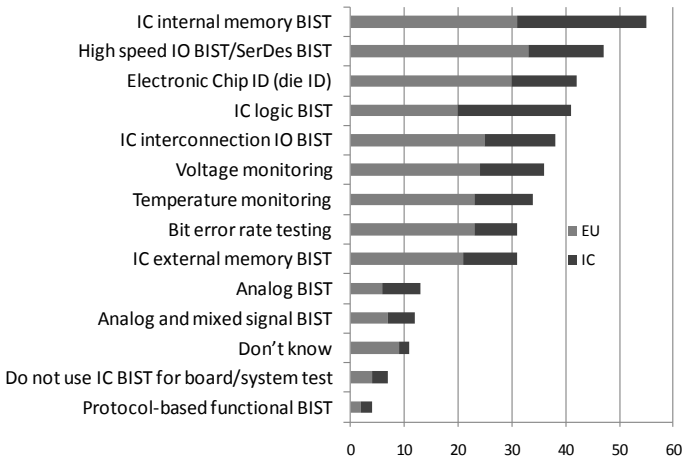

Figure 10 Types of IC BIST run at the board/system.

Respondents also replied they would like to use IC BIST more at the in-field maintenance and PCBA repair steps as well.

The respondents' opinions on the effectiveness of BIST in detecting defects at the board level are also important to gauge the future usage of BIST at the board test. By far the majority of IC and End User respondents said BIST is good at catching defects in the areas of internal memory, IC interconnect, high speed IOs, logic and external memory cells.

The survey results so far look positive for IC BIST usage for board and system level testing. In order to assess any further roadblocks to its ability to run at these test steps the question was asked, "What problems have you encountered running IC BIST at the board and system levels?" The respondents' replies in order of 'most problems' to 'least' were:

1. BIST tests are not supported by a standard
2. Few ICs support BIST function
3. Commercial IC suppliers do not provide the BIST function to board users
4. Lack of access to BIST when IC is mounted on board
5. Poor board DFT (hardware and software).
6. BIST tests designed for IC test do not meet board and system test requirements.
7. PCBA testing does not support IC BIST application.
8. BIST does not meet the diagnostic requirement
9. Current investment (such as for test equipment) hinders the application
10. Test coverage of BIST is lower than other tests

The final question in this section asked respondents "to estimate the defect coverage at board test steps where BIST is currently used". Please note the survey gave no specified definition of what 'coverage' meant. This was left up to each respondent to interpret. The majority of replies were that it is estimated currently that IC BIST has less than 20% coverage, but in future it would ideally be at greater than 80%.

This section's questions provided a good snapshot of where the industry is at today in terms of running IC BIST at board and system test. IC BIST tests are able to run there, with most being accessible via the 1149.1 TAP, however, many BIST tests are the design companies own IP and an NDA is needed for the application at the board and system level. End Users of BIST are requesting IC BIST and it is seen to be effective at board and system level test.

3.4 Results for the Future of BIST

This section gives data on the industry expectations for the future of IC BIST at board and system testing, in terms of whether the industry is trending up in its usage and understanding if IC BIST running at these test steps is useful. To meet this section's objective, the first question was "How critical is board and system level IC BIST access for future coverage and fault isolation?" The response was very positive as shown in table II:

Table II Criticalness of board and system level IC BIST access for future coverage and fault isolation

Very critical	60%
Somewhat critical	31%
Not critical	3%
Do not know	6%

The next question was "Do respondents see IC BIST coupled with boundary scan replacing some of the diminishing test point access of in-circuit testing for assembly defects?" Again, the clear majority was "yes", as shown in Table III.

Table III Respondents who see IC BIST coupled with boundary scan replacing some of the diminishing test point access of in-circuit testing for assembly defect

Yes	80%
No	11%
In some cases	3%
Do not know	6%

Table IV show the replies to the question "In the next 2-5 years, what role will IC BIST play in your company's product test?" Again, the majority of respondents said it would increase and none said it would decrease.

Table IV The role BIST will play in respondents' companies' test in the next 2-5 years

It will increase	85%
It will decrease	0%
It will not change	7%
Do not know	8%

The final part of this section looked at plans to use any existing related DFT standards and solicited feedback on how respondents thought BIST test could be further standardized to improve usability at board and system test. The majority of respondents (74% of IC people and 59% of End Users) said they plan to adopt or are actively considering adopting standards. Figure 11 shows specifically which standards.

Both IEEE 1149.7 [5] and IEEE P1687 [4] have equal interest from both respondent groups. There is also some interest in the IEEE P1581 [6] standard as well. Some respondents also replied they are interested in SJTAG [7], new enhancements to IEEE 1149.1 [8], IEEE 1149.6 [9], IEEE1500 [10] and IEEE 1149.8.1 [11].

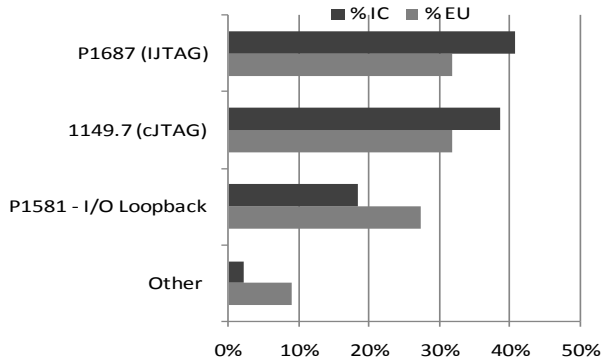

Figure 11 Standards being looked at by respondents

Figure 12 below shows the replies to the question "If standards are established on IC BIST design and its application in board and system level test, what do you think should be standardized?"

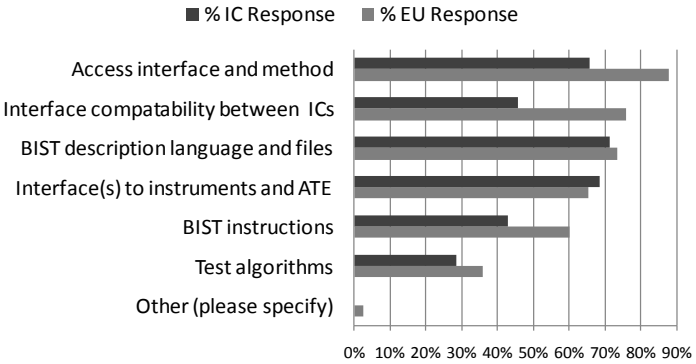

Figure 12 What respondents think should be standardized if standards are established for IC BIST at board and system test.

Both respondent groups have the highest concern about the BIST interface and access method, BIST description language and files, the interfacing to ATE and instruments, and the compatibility of interfaces between ICs. Some areas where the two respondent groups differed are EUs (88%) are more concerned about access interface and method than ICs (66%).

EUs (76%) are also more concerned about interface compatibility between chips than ICs (46%) and EUs (60%) are somewhat more concerned about BIST instructions than ICs (43%). When respondents were asked how they thought BIST tests should be standardized, some respondents replied that existing standards could be leveraged (particularly 1149.1 and 1149.7) and that new standards should be compliant to these existing standards. Many respondents also felt that the new IEEE P1687 standard would address many of the requirements for running IC BIST at board and system test.

4. Conclusions

The survey data showed that many IC BIST tests are available and currently run at the board level, with the most common being internal and external memory testing, voltage and temperature monitoring, IOBIST, and Logic BIST. More than 60% of board designers are requesting access to IC BIST to run at the board level, which shows good adoption already of IC BIST at the board level. The access method to the IC BIST is predominantly via the 1149.1 TAP, and hence is very suitable for board. The majority of BIST tests are proprietary, which could present a roadblock to wider adoption and implementation at the board test level.

BIST run at the board/system levels was seen to be good at catching defects in the areas of internal memory cells, IO interconnects, high speed IO and logic BIST.

It is currently run at many different board and system test steps, and a future use is to run more BIST during in-field maintenance and diagnostics and PCBA repair test.

There are however still some problems encountered in that few ICs support BIST function, commercial IC suppliers do not give the BIST function to the board users, there can still be a lack of access to the BIST when the IC is mounted on the board and BIST is not supported by a standard.

Looking to the future, IC BIST is seen as critical for future fault isolation and respondents would like to see BIST coverage at greater than 80% at board level testing. More than 75% of respondents see IC BIST coupled with boundary-scan replacing some of the diminishing test point access of in-circuit testing for assembly defects, Well over 50% of respondents have definite plans to adopt current standards or are actively involved and considering adopting them.

4.1. iNEMI BIST Project Phase 2 Next Steps

While there is good adoption , the usefulness of IC BIST at board and system test can continue to be promoted.

The team needs to look at how existing standards can help with BIST standardization and implementation and promote the standards to that effect. Any gaps found in the existing standards will be presented to the respective standards committee with recommendations on how the standard could be changed to support IC BIST at board and system test.

The standardization of description languages and interfaces will also be investigated. The use of IC BIST to help with lack of ICT test point coverage needs further research as well.

Acknowledgments

The authors would like to acknowledge the iNEMI BIST project team (from many companies) and the iNEMI staff who derived questions for the survey and compiled the results.

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5. IEEE 1149.7 http://grouper.ieee.org/groups/1149/7/. **
6. IEEE P1581 http://grouper.ieee.org/groups/1581/. **
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8. IEEE 1149.1 http://grouper.ieee.org/groups/1149/1/. **
9. IEEE 1149.6 http://grouper.ieee.org/groups/1149/6/. **
10. IEEE 1500 http://grouper.ieee.org/groups/1500/. **
11. IEEE P1149.8.1 http://grouper.ieee.org/groups/1149/atoggle/. **

Note: * iNEMI membership required for access.
** IEEE membership may be required for access.