NEMI Project on Cost-Performance Modeling of High Speed Backplanes, Copper vs. Optical

Presented on Behalf of the Project Members
by Peter Arrowsmith
05-04-2004
Industry Collaboration

Benefits of Participation
NEMI Mission – North American Based Consortium

Assure Leadership of the Global Electronics Manufacturing Supply Chain for the benefit of members and the industry

NEMI Scope

Collaborative Design
Components
Materials
Materials Transformation
Equipment
Build to Order
Software Solutions
Life Cycle Solutions

Supply Chain Management
Information Technology
Logistics
Communications
Business Practices

Marketing ➔ Design ➔ Manufacturing ➔ Order Fulfillment ➔ Customer

Connect with and Strengthen your Supply Chain
NEMI Roadmap Cycle

NEMI Implementation Cycle
Connect with and Strengthen your Supply Chain
What Does NEMI Do?

**Leverage the combined Power of Member Companies to Provide Industry Leadership**

- NEMI Roadmaps the Global Needs of the Electronics Industry
  - Evolution of existing technologies
  - Predictions on emerging/innovative technologies
- NEMI Identifies Gaps (both business & technical) in the electronics Infrastructure
- NEMI Stimulates R&D Projects to fill these Gaps
- NEMI Establishes Regional Implementation Projects to Eliminate these Gaps
- NEMI Stimulates World-wide Standards to speed the Introduction of New Technology & Business Practices
- NEMI works with other organizations to insure that North American government policy recommendations are aligned with NEMI mission.

*Connect with and Strengthen your Supply Chain*
Industry Leaders belong to NEMI – OEM/EMS

Connect with and Strengthen your Supply Chain
Connect with and Strengthen your Supply Chain

Industry Leaders belong to NEMI - Suppliers
Connect with and Strengthen your Supply Chain

Industry Leaders – Consultants, Government, Organizations, and Universities

- AEA
- AMR Research
- EIA
- IPC
- CMAP
- Centre for Microelectronics Assembly and Packaging
- IEEC
- METAGROUP
- Georgia Institute of Technology
- MIT
- NCMS
- NIST
- Québec
- Virginia’s Center for Innovative Technology
www.nemi.org

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Optoelectronics Substrates Project

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OE Trends & Drivers

- Starting to see OE equipment revenue growth, e.g. access & FTTP, PONs
- Traffic continues to grow 50-100% pa, triple play (data, VoIP, video), retail, file swapping...
- Distributed systems (1000s servers) require high speed interconnects
- Copper can support up to 10G over 1m, 40G in some cases, at increased cost: mtrls, line spacing, signal conditioning...
- Emerging OE technologies: reconfigurable/active systems, polymer waveguides & substrates, Si optical emission & modulation (Intel), optical band gap mtrls...
- Although fiber interconnects will be continue to be used. Optical functions, initially transmission, will co-exist with electrical in the printed wiring board
- COST reduction of pkg, assembly & test, remains significant driver
Current Interconnect Board-Board Bottleneck

• Increasing chip-performance leads to problems with conventional electrical intrasystem interconnection technologies (Siemens SBS C-LAB, 2002):
  – Increasing electromagnetic radiation
  – Limited bandwidth due to high frequency skin effect
  – High pin-count through limited bandwidth
  – Increasing signal integrity and timing problems
  – Increased data rate leads to disproportional increased costs and power consumption

• Transmission speeds reach their physical limits when power consumption is increased and there is no obvious increase in the propagation speed (for some architectures)

• It is the ability of optical interconnections to operate at high data rates (>2.5 GHz) with superior signal integrity that makes them an exploitable alternative
## JIEP Optical Packaging Roadmap

<table>
<thead>
<tr>
<th>Sub-System Packaging</th>
<th>~ 1998</th>
<th>2000</th>
<th>2005</th>
<th>2010</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sub-System</td>
<td>~ 500 Gbps</td>
<td>500-1000 Gbps (&lt;Tbps)</td>
<td>&gt; Tbps</td>
<td></td>
</tr>
<tr>
<td>Optical Connection</td>
<td>Flexible fiber board</td>
<td>Board edge optical connector</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Board Packaging</td>
<td>Optical printed board</td>
<td>Module on optical printed board</td>
<td>2-D Connectors</td>
<td></td>
</tr>
<tr>
<td>Optical Connection</td>
<td>Direct connection between optical waveguides</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Module Packaging

<table>
<thead>
<tr>
<th>Package</th>
<th>Wiring Board</th>
<th>Optical Connection</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pigtail fibers</td>
<td>PLC Platform</td>
<td>Mechanical alignment</td>
<td>End Type</td>
</tr>
<tr>
<td>Multi-channel using recepticals</td>
<td>Optical path conversion technology</td>
<td>Mode field matching</td>
<td>LD PD AWG</td>
</tr>
<tr>
<td>~ 1.5 Gbps</td>
<td>Optical path conversion waveguide</td>
<td>Optical path conversion technology</td>
<td>32ch</td>
</tr>
<tr>
<td>~ 10 channels</td>
<td>mode coupling</td>
<td>connection between multi-layer optical wiring</td>
<td>64 ch</td>
</tr>
<tr>
<td>~ 2.5 Gbps</td>
<td></td>
<td></td>
<td>100ch</td>
</tr>
<tr>
<td>~ 32 channels</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>~ 2.5-10 Gbps</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>~ 100 channels</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Source: Japan Institute of Electronics Packaging & SEMI

Connect with and Strengthen your Supply Chain
Optoelectronics Substrates Project

Original Purpose Statements:

• This purpose of this group is to addresses the implementation of optical and optoelectronic technologies in printed wiring boards (PWB’s) used for packaging, or for other applications.

The areas to be addressed include:

• An understanding of the drivers and the constraints of producing optoelectronic PWB’s including cost analysis and tradeoffs.
• Design considerations for materials used for PWB fabrication and assembly, including material properties
• Manufacturability of waveguides and the integration of waveguides in PWB’s
• Component mounting and interconnecting structures
• Performance and testing of waveguides and connector attachments
Current Statement:

• Initial investigation (2002) indicated that the OEM’s were not planning to use optoelectronics in their next generation machines

• The OEM’s were all working on internal analyses of optoelectronic solutions and were all interested in participating in a NEMI technology analysis activity

• There are numerous estimates of how far copper can be pushed to increase data rates. The estimates range from 2.5 Gb/s to 40 Gb/s per channel.

• It was decided to do a business analysis of copper vs. optoelectronics

• The product to be analyzed will be a communications industry backplane, e.g. Terabit router
Cost-performance is the key driver; we need an industry metric to compare optical vs. Cu-based, e.g. $/(Gb/s/channel/m)

Crossover zone:
changeover will not be immediate, but will range depending on issues including cost sensitivity, reliability, and design limitations
Optoelectronics Substrates Project

• Project Objectives:
  – Develop cost models, including assembly and test, of a high performance “product” (black box emulator)
  – Copper and optical backplane versions
  – Run cost models for various speeds and system configurations, using appropriate sets of components and technologies

• Project Benefits:
  – Information exchange between suppliers (component, technology..), assemblers and system OEMs
  – Define industry relevant cost-performance metric(s)
  – Identify technology gaps and barriers to implementation
  – Roadmaps and cost models will be available for industry use

• Meeting Objectives:
  – Report work-in-progress
  – Promote awareness, attract new participants
Optoelectronics Substrates Project: Status

- Project started in June 2003, in open/forming stage
- Bi-weekly telecons
- Very good participation
  - Several OEM’s, PCB fabricators, CMs, material suppliers
- First pass output of PCB fab cost model run and validated by 3 fabricators
- Starting to add connector choices to the model
- Draft electrical technology roadmap, 1-10(40) Gbps, includes connectors, signal conditioning, chip-sets and high performance substrates
- Discussing the optoelectronic technology alternatives
  - Fiber, Waveguide, Polymer
- Developing list of optical attributes and performance issues
- Optical cost model not yet started… looking for input
Cost Modeling Method

• Based on Technical Cost Modeling, as developed by IBIS Associates / MIT
• Activities Based Costing, plus engineering relationships
  – Assembly cycle time = f(design, mtrls, equipment)
Electrical Backplane Cost Model

Context
- North American facility
- Equipment assumes max 24 inch width conveyors
- Yields reflective of 8 mil line / space
- Drilling reflects 20 mil minimum diameter
- Medium throughput (350 Ksqft/yr top surface)

Product
- 32 metal layers, no buried vias
- FR-4, 24x20 inch panel, 20x18 inch finished board
- 5,000 drilled holes per board
- ~1-3 Gbps performance
## Back Plane Cost Model

### DESIGN ISSUES

<table>
<thead>
<tr>
<th>Product Name</th>
<th>Cu backplane</th>
<th>PROD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Annual Production Volume</td>
<td>117 (000) board per year</td>
<td>VOL</td>
</tr>
<tr>
<td>Other assumptions:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Panel Length</td>
<td>24 inch</td>
<td>PLEN</td>
</tr>
<tr>
<td>Panel Width</td>
<td>20 inch</td>
<td>PWID</td>
</tr>
<tr>
<td>Minimum Panel Edge Margin</td>
<td>0.8 inch</td>
<td>PMARGIN</td>
</tr>
<tr>
<td>Minimum Space Between Boards</td>
<td>0.1 inch</td>
<td>BMARGIN</td>
</tr>
<tr>
<td>Boards Per Panel</td>
<td>1</td>
<td>BPPAN</td>
</tr>
<tr>
<td>Number of Drilled Through-Holes</td>
<td>5,000 per board</td>
<td>NHOLES</td>
</tr>
<tr>
<td>Number of Innerlayer Pairs - FR-4</td>
<td>15</td>
<td>FR-4</td>
</tr>
<tr>
<td>Number of Innerlayer Pairs - Type 1</td>
<td>0</td>
<td>Type 1</td>
</tr>
<tr>
<td>Number of Innerlayer Pairs - Type 2</td>
<td>0</td>
<td>Type 2</td>
</tr>
<tr>
<td>Number of Innerlayer Pairs - Type 3</td>
<td>0</td>
<td>Type 3</td>
</tr>
<tr>
<td>Number of Innerlayer Pairs - Type 4</td>
<td>0</td>
<td>Type 4</td>
</tr>
<tr>
<td>Number of Innerlayer Pairs - Type 5</td>
<td>0</td>
<td>Type 5</td>
</tr>
<tr>
<td>Number of Innerlayer Pairs - Type 6</td>
<td>0</td>
<td>Type 6</td>
</tr>
<tr>
<td>Number of Innerlayer Pairs - Type 7</td>
<td>0</td>
<td>Type 7</td>
</tr>
<tr>
<td>Number of Innerlayer Pairs - Type 8</td>
<td>0</td>
<td>Type 8</td>
</tr>
<tr>
<td>Number of Innerlayer Pairs / Avg Price</td>
<td>15 NIP</td>
<td>$2.17</td>
</tr>
</tbody>
</table>

**Yield of Innerlayer Pairs**: 94.0%

**Yield of Boards, Post-Lamination**: 99.2% | number of innerlayer pairs

**Yield of Boards, Post-Lamination**: 88.0%

### PROCESSING ISSUES

<table>
<thead>
<tr>
<th>Sequence of Operations</th>
<th>Product Description</th>
<th>Facility Description</th>
<th>Operation Database</th>
<th>Cost Summary</th>
<th>Co</th>
</tr>
</thead>
<tbody>
<tr>
<td>NUM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Strategy for System Cost Models

• Seek input from relevant experts:
  – technology and hardware selection, identify gaps (white paper)
  – issues & concerns, e.g. manufacturing yield, reliability
  – requirements for performance, application, future system (IP, confidentiality issues)
• Define detailed sets of attributes, electrical & optical
• Draft roadmaps: understand which and how the attributes change with performance
• Define 1st generation black box system (top down approach)
• Choose logical set(s) of the key attributes (80/20)
• Obtain cost data, build initial cost model
• Verify and improve model with actual costs, expert input
• Run what if sensitivities: speed, no. lines, hardware variation, yields, …
• Repeat for 2nd generation system

Connect with and Strengthen your Supply Chain
Electrical Backplane Attributes 1-40G (Partial)

- Receiver/Transmitter signal conditioning chip set:
  - Bus type: multipoint, point-to-point
  - Signaling: single-ended, differential, CML NRZ, PAM4, duobinary
  - Equalization: pre/post emphasis, filtering, DFE
  - Encoding: 8b/10b, 64b/66b, FEC codes...

- PCB Technology:
  - Materials: FR4, Getek, PPO/CE, FR4013, BT/APPE, PTFE… LCP
  - Loss: \( D_f = 0.02 - 0.002 \)
  - Processes: standard, backdrilling, dual density drilling
  - Transmission line: single-ended, differential pairs, broadside
  - Distance: up to 1 m
  - Via/connector launch: PTH, pad in via, micro, buried, differential anti-pad

- Connector Technology: Several vendor types
## Electrical Bandwidth Technology Roadmap

<table>
<thead>
<tr>
<th>Signaling Bandwidth</th>
<th>Application</th>
<th>Receiver/Transmitter Signal Conditioning Chip Set</th>
<th>SerDes Technology</th>
<th>Distance</th>
<th>Size Design</th>
<th>Connector, Launch, Repair</th>
</tr>
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<tr>
<td>1G</td>
<td>DIMM</td>
<td>Multipoint, Point to point</td>
<td>FR-4</td>
<td>1m</td>
<td>200 mm</td>
<td>HDM, ERmet</td>
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<tr>
<td>2.5G / 3.125G</td>
<td>Chip to chip, Legacy, Point to point</td>
<td>FR-4, FR4013</td>
<td>PPO-GE, FR4013</td>
<td>0.8 – 1.0</td>
<td>250 mm</td>
<td>HDM-L, Z-Pack HM-2D</td>
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**Notes:**
- FR-4: FR-4, FR4013
- PPO-GE: PPO-GE, FR4013
- HDM: HDM, HDM-L
- ERmet: ERmet, ERmet-ZD
- airMax: airMax 15
- Z-Pack: Z-Pack HM-2D
- MultiGig: MultiGig RT-3
- FCI: Matrel 2000
- FCI: Matrel 4000
- Foilure: FCI 251200a
- Melox: Melox L, Melox S
- SIP: SIP-1000 I platform

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**Electrical Bandwidth Technology Roadmap**

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Optical Backplane Attributes 1-40G (Partial)

- **Receiver/Transmitter:**
  - Link loss budget: 8 dB per channel @ 850 nm
  - Source/modulation: <10G VCSEL, 10G F-P, >20G DFB
  - Channel density: single channel transceivers, VCSEL / PD arrays
  - Multiplex: serial (TDM), parallel (12-72 channels), CWDM

- **Light coupling:**
  - Type: butt coupled, index matched, lens, mirror/grating, free-space

- **Optical carrier technology:**
  - Fiber: single, ribbon, flex/laminated (shuffle), MM or SM
  - Waveguide: surface, embedded, organic, silica, PLC
  - Impact on PCB design rules, electrical layer reduction

- **Connector:**
  - Coupling losses: tolerance, cleanliness (contamination has critical impact on yield & costs, but hard to quantify)

- **Assembly & Test**

*Connect with and Strengthen your Supply Chain*
Black Box 1st Generation Optical System (Proposed)

- Based on COTS hardware
- Point-to-point, defined, fixed physical path
- Fiber based, MM ribbon
- 1x12 array connectors, VCSELs & PDs in transceiver packages
- 2.5 Gbps per channel, unidirectional Tx→Rx
- Electrical switching, central hub, star switch fabric

Connect with and Strengthen your Supply Chain
Optoelectronics Circuits

3rd Generation Optical Circuits
2nd Generation Hybrid Fiber Cables
1st Generation Discrete Fiber Interconnect

Courtesy: JW Watson, 3M Optical Comm Tech Center
Rochester Institute of Technology (RIT)
Board-to-Board Optical Interconnects

- Daughterboard
- Optical and Electronic Interconnects
- Backplane
- Optical Transmitter, Receiver or Transceiver Modules
- Optical Waveguide and Electrical Conductors
- Blind-Mating Optical Backplane Connectors
- Motherboard

Rochester Institute of Technology (RIT)
**OECB Technology Challenges**

- **n x 4 flipchip VCSEL array**
- **Optical underfill**
- **Optical layer, with embedded MM waveguides**
- **Optical via**
- **45° mirror**
- **Multi-layer FR4 board**
- **Optical edge connector**

- Choice of Glass or Polymer optical layers
- Choice of embedded or overlaid waveguides
- Choice of assembled or integrated mirrors

*Connect with and Strengthen your Supply Chain*
Coupling Challenge

- **Assembled Mirror**?
  - Several research avenues involving the insertion of mirrors or carriers.
  - Large alignment tolerance stack-up.
  - High cost issues due to small parts, and tight alignment tolerances.

- **Integrated Mirror**?
  - Ideal process route is to combine mirror into board during PCB fabrication, for direct active component attach.
  - Limited alignment tolerance stack-up.
  - Low cost assembly achievable.

*Source: Siemens SBS C-Labs*
Optical Backplane Global Forecast

$2.565 billion by 2008

Source: ElectroniCast
Next Steps

• Run multiple copper sensitivities
  – Materials, via qty. and types,
  – Layers counts, etc.
• Develop connector data base
  – Cost, type, application
• Add signal conditioning, bus chip-sets, ASICs
  – May need resource assistance
• Complete optical attributes and optical technology roadmap
• Determine the copper / opto architectures to be modeled for high performance
  – Difficult because it is often proprietary information
Conclusions

• Performance of copper backplanes will continue to improve, at increased cost to achieve signal integrity
• Benefits of optical outweigh cost for critical applications, e.g. avionics, clock distribution in high perf systems
• Future generation, high bandwidth telecom/office systems likely to have optical distribution
• The problems of assembling and handling fiber/connectors are drivers for integrating optical waveguides in the PWB
• Improved coupling and light-turning technologies are required
• The initial choices of optical technology and components have major impact on costs. Have we chosen the right combination?
• Cost-performance models of emulator systems are useful way to understand the (relative) costs, test different choices
• Immediate need for practical cost-performance metric(s), e.g. $/bit, $/(Gbps/m/channel)

Connect with and Strengthen your Supply Chain
Contacts

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Your Participation is Welcome!
Optoelectronics Substrates Project