



HFR-Free Material Dk/Df Test Method Proposal



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OUTLINE

- I. Driver for Cisco Interest
- II. HFR-Free Materials – Dk/Dk Testing
- III. Towards a New Dk/Df Test Method

I. Driver for Cisco Interest

From Cisco's 2008 Materials Roadmap:

Top-Level Goal for Pb-Free Linecards

Direct replacement of

HIGH-LOSS PHENOLICS

with reduced / lower-loss

HALOGEN-FREE MAT'LS

(...at minimal cost impact...of course!)

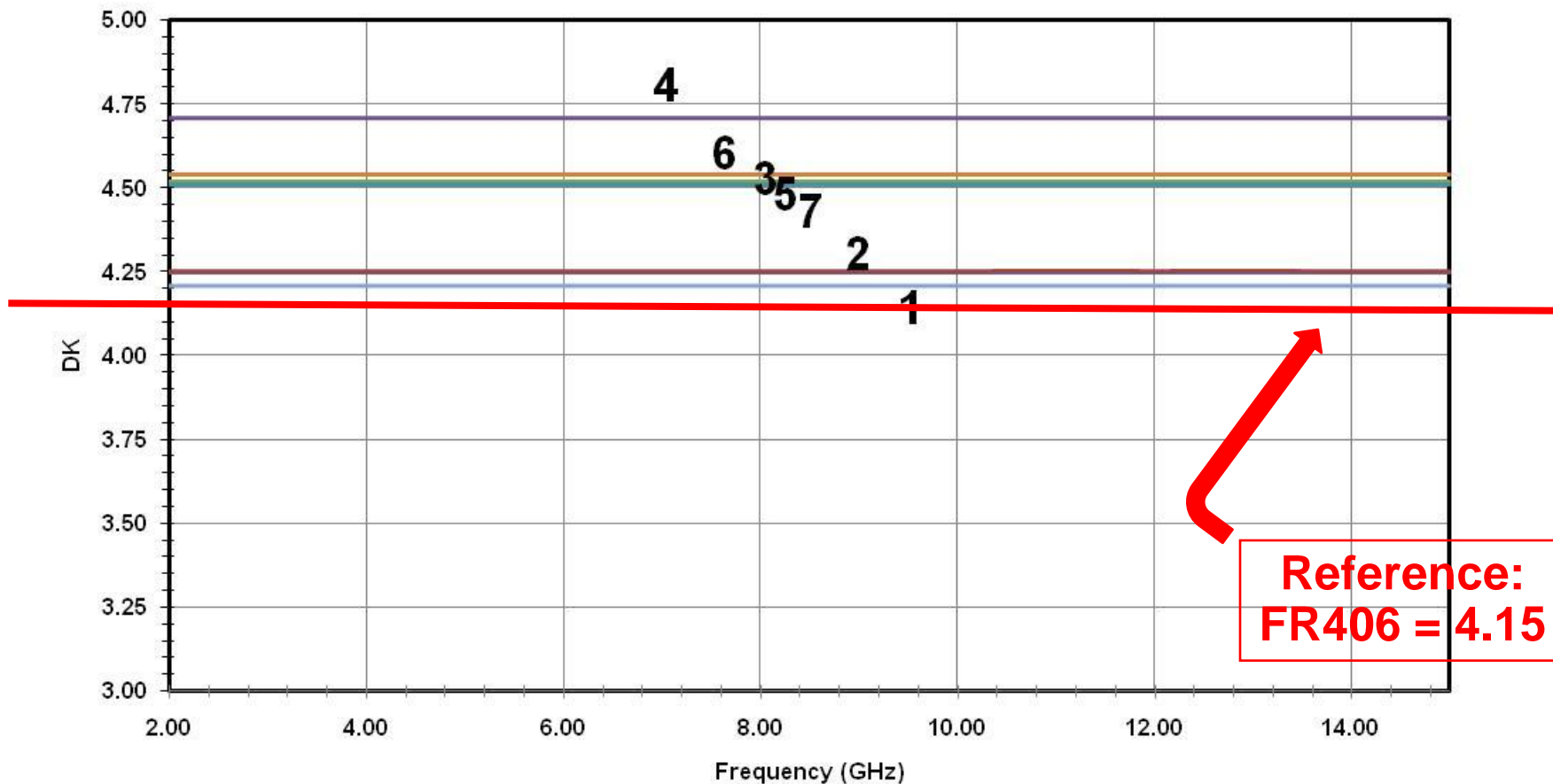
II. Dk/Df Testing

Halogen-Free

Materials

HFR-free material Dk test results

Dielectric Constant -- With Resin 50%

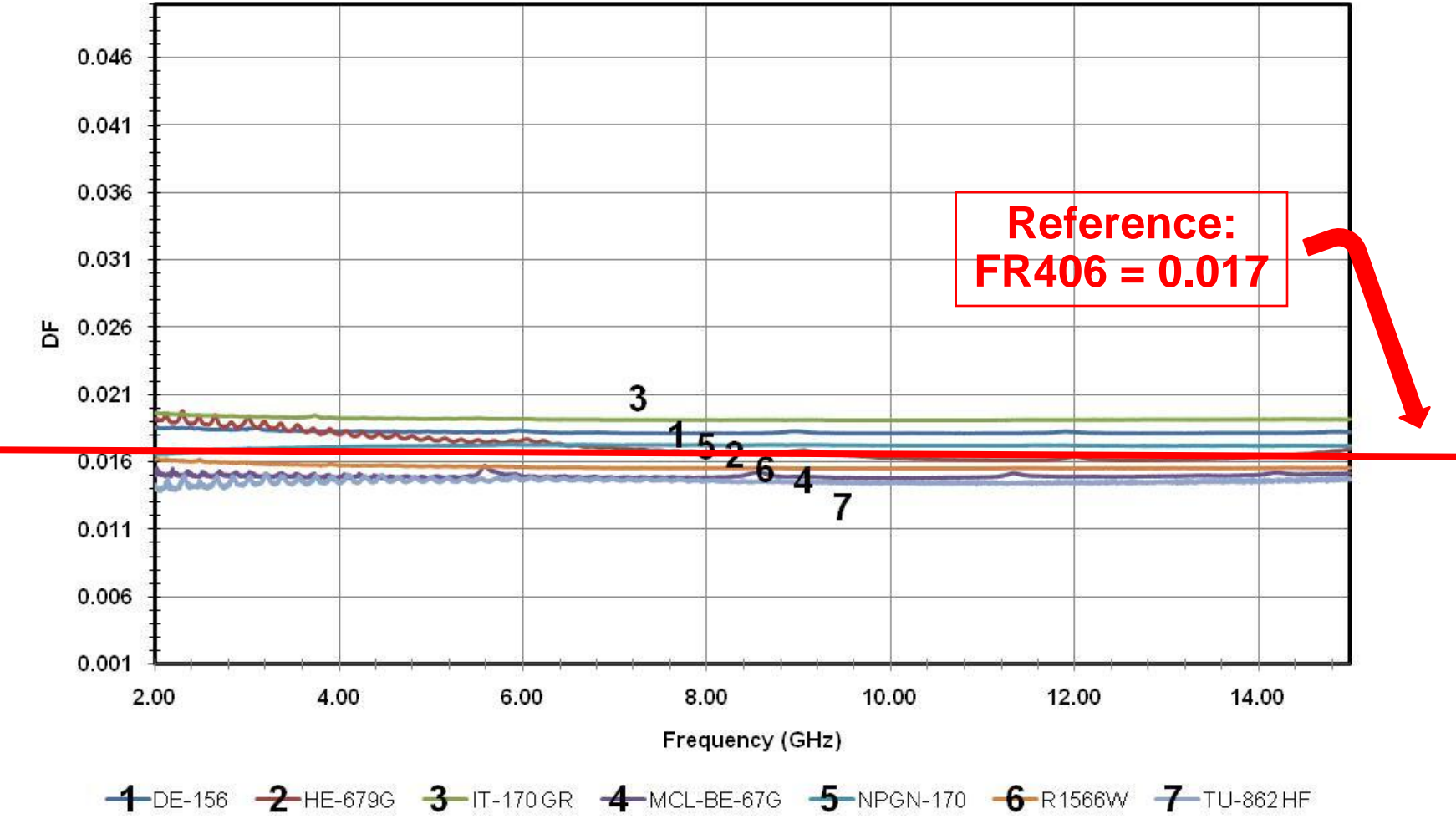


Reference:
FR406 = 4.15

- 1 DE-156
- 2 HE-679G
- 3 IT-170 GR
- 4 MCL-BE-67G
- 5 NPGN-170
- 6 R1566W
- 7 TU-862 HF

HFR-free material Df test results

Loss Tangent (Dissipation Factor)



HFR-free: New materials planned

FY'10 Test Plan

- **Hitachi BE-67G(R) or G(S)**
- **EMC EM-285 or 280(H)**
- **Ventec VT-447**
- **(?) Panasonic R-1577***

** Release date-dependent*

III. Towards a New Dk/Df Test Method

Top-Level Goal

Gain acceptance of our Dk/Df test method as an official IPC Industry Standard in TM-650

START: SUMMER 2009

WHY...?

- ... No industry consensus on methods**
- ... Existing methods: single data points**
- ... Apples/oranges between datasheets**

General challenges around Dk/Df

- No NIST-traceable “gold standard” for Dk/Df
 - RESULT: No way to know that a given Dk/Df measurement is “correct”
 - RESULT: No way to know that a modeled Dk/Df is “correct”
- No industry consensus on test methods
 - IPC: Official in TM-650: 2.5.5.x (total 10 methods)
 - JIS: Tri-plate resonator
 - RESULT: Datasheet Dk/Df values don't correlate across laminate mfr's
- Cisco/MST: Converge better test method & algorithm
 - Test method: No tuned resonators, real-life PCB, many sample points
 - Algorithm: Physics-based; address simplifications in existing models
 - Desired Endpoint 1: Measured Dk/Df curves overlay modeled curves
 - Desired Endpoint 2: Library of apples-apples curves for WW laminates

Current IPC Methods vs. Cisco/MST

- X-band, Stripline “Sandwich”, Split-Cylinder, Bereskin, FSR

All employ tuned resonators -- TV's do not resemble real PCBs

Require TV structures tuned to specific frequencies

Result yielded: Dk/Df at individual freq. points (Loss \rightarrow Df , Phase \rightarrow Dk)

Interpolation required between measured points

Dk/Df extraction algorithms are fairly simplistic (Hammerstad, 1975)

Algorithms based on ideal (perfectly smooth Cu) traces

- Cisco / MST test method: For 2+ GHz

“Real PCB” stripline TV – Not a tuned resonator

Calibration structures built into the board itself (TRL calibration)

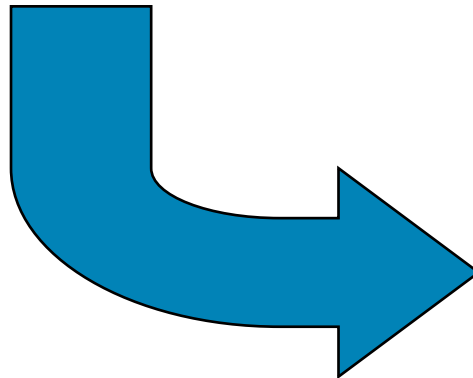
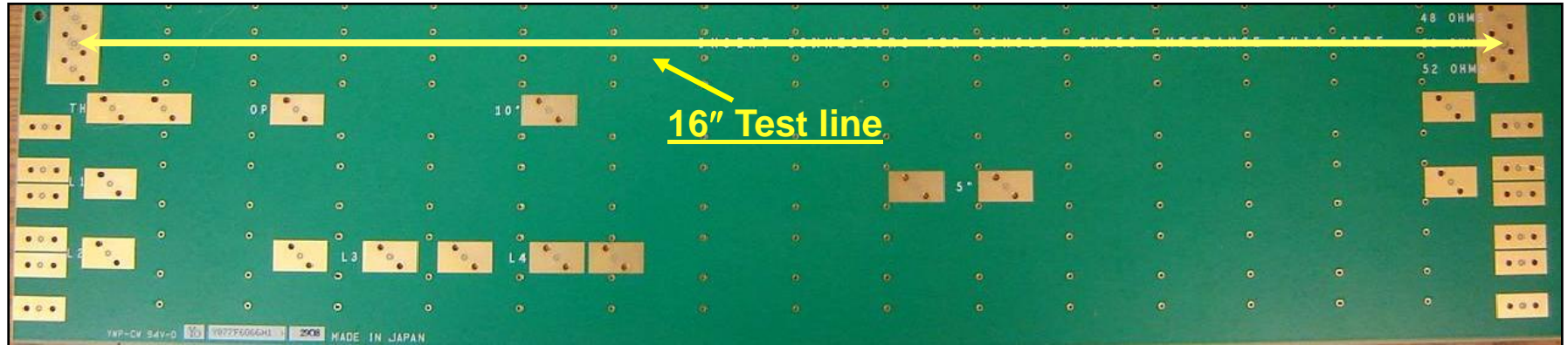
Thousands of discrete measurements (at ~5 MHz intervals)

Result yielded: (Effectively) continuous Dk/Df curves; no interpolation

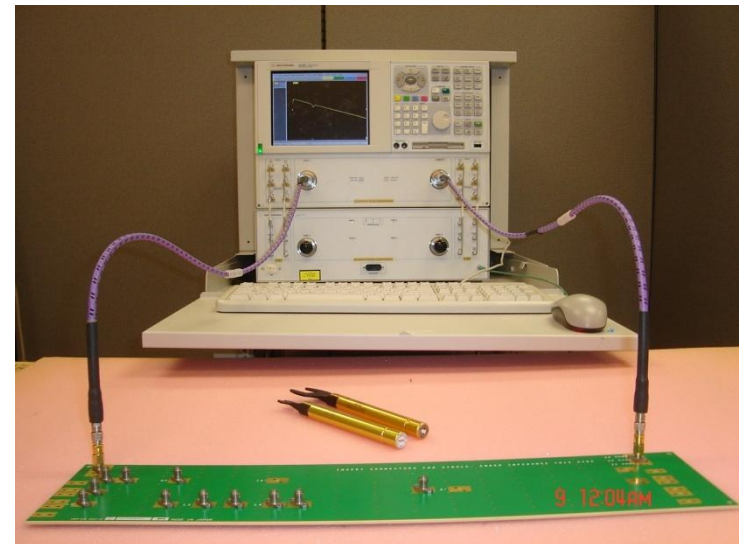
Dk/Df extraction algorithms updated to account for Cu roughness

Structure of test vehicle

Top view of Cisco / MST Stripline Test Vehicle

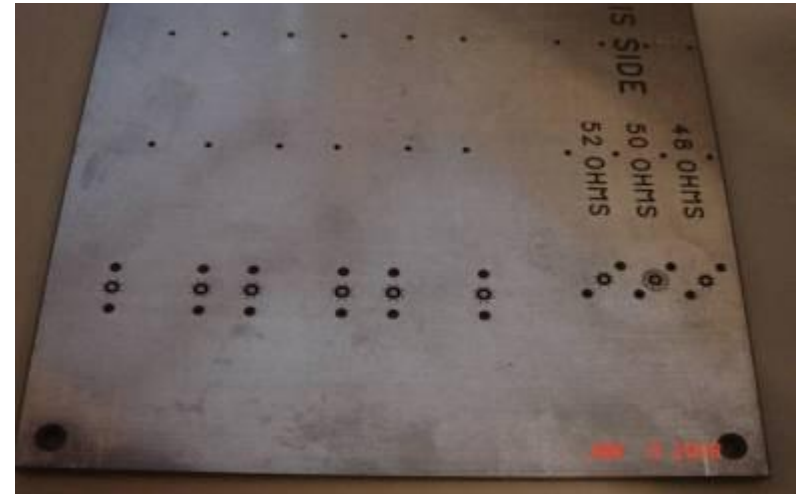


***Agilent E8364B PNA-series
Vector Network Analyzer***



Stripline TV Structure

The Stripline TV includes both 50Ω SE and 100Ω diff pairs and accepts SMA connectors.



The Molex SMA connectors are of the compression-mount style. (Molex P/N 73251-1850)

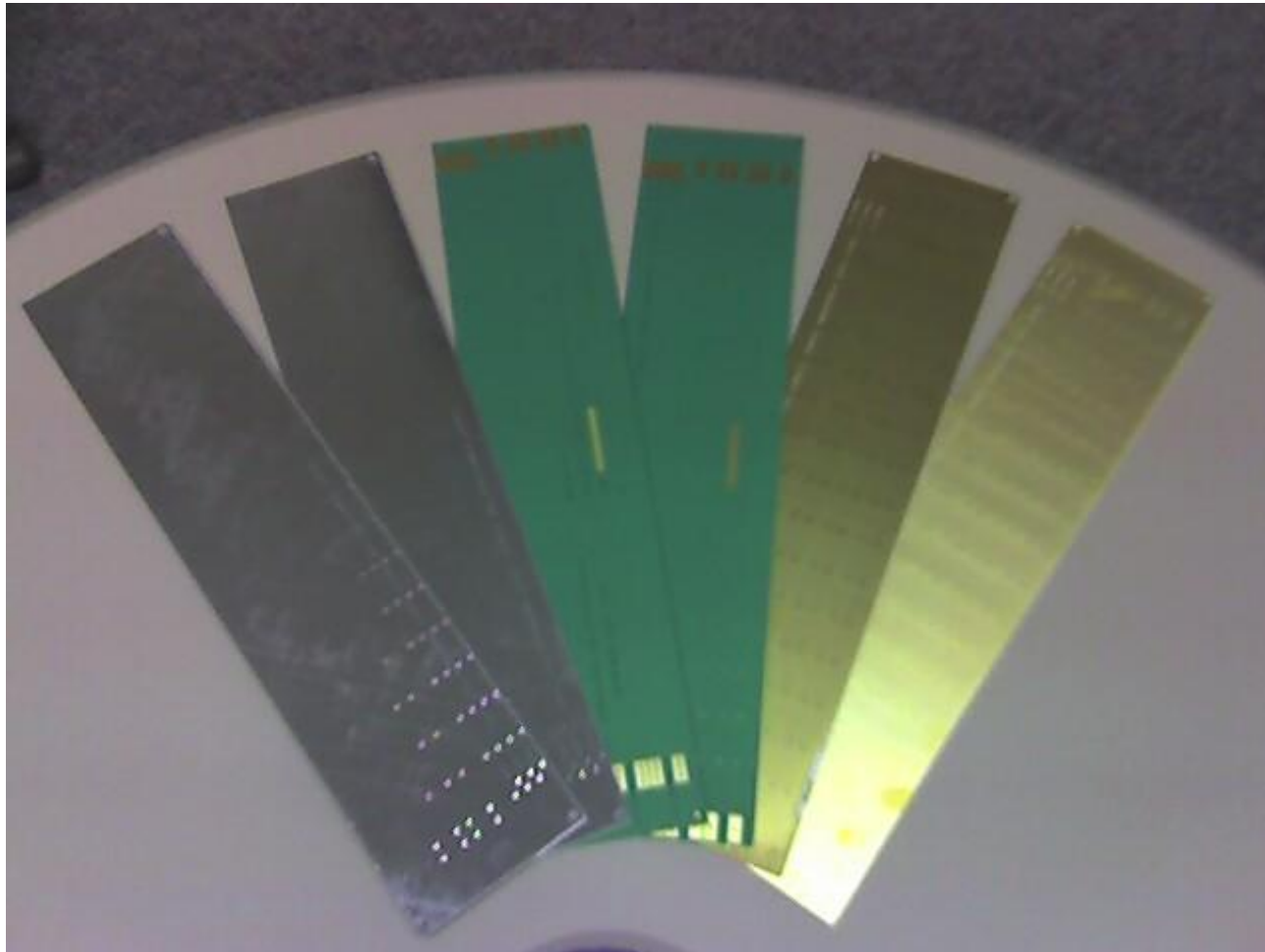
Trace length 16" (406mm)

Stripline TV Stackup

- Six-layer PCB, 17.5" x 4" x .093"
- Two 3-layer, balanced stripline structures
 - ~0.010 dielectric on both sides
 - Target 50% RC (usually 2x2116)
- Layer 2 is 50Ω SE and Layer 5 is 100Ω Diff pairs
- Layers 1, 3, 4, 6 are GND reference
- Dummy material between Layers 3 and 4
- Three adjacent SE/Diff pairs, to allow best match
 - SE = 48, 50, 52 ohms
 - Diff = 96, 100, 104 ohms
- SMA mounted on far side → via stubs .012" nominal
 - No backdrilling (for this iteration)
 - Stub length variation from BD is undesirable

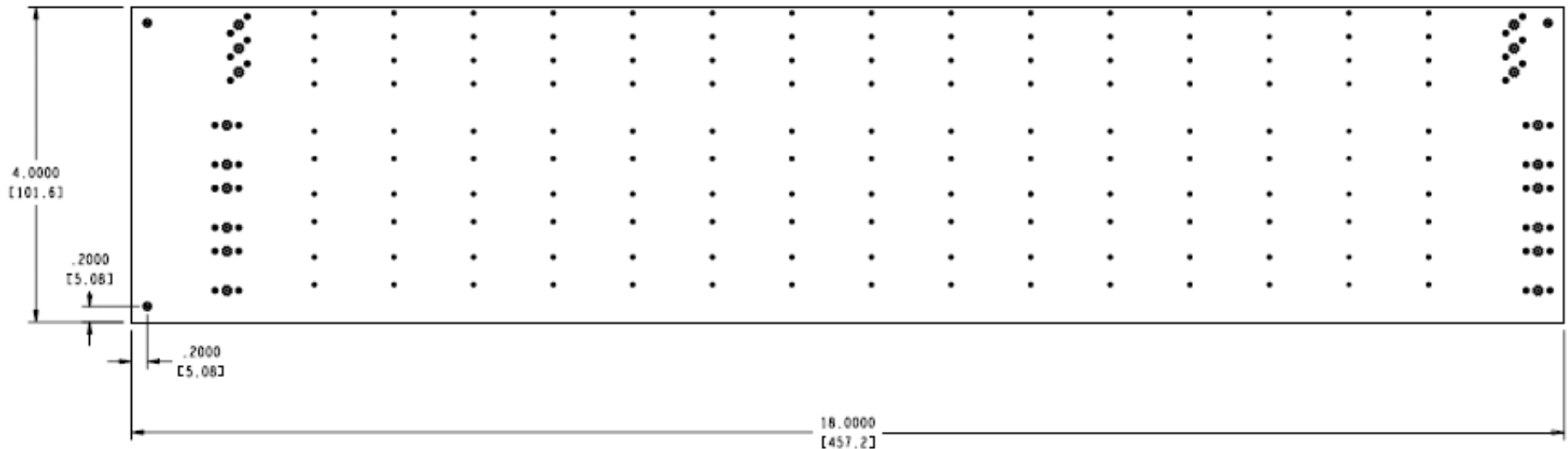
Test Program Details

EXISTING TV SET: ~ 40 MATERIALS



Test Program Details

GERBER DATA FOR TV AVAILABLE



... for those who want to replicate, or add new materials to the S-parameter and Dk/Df database!

Test Program Details

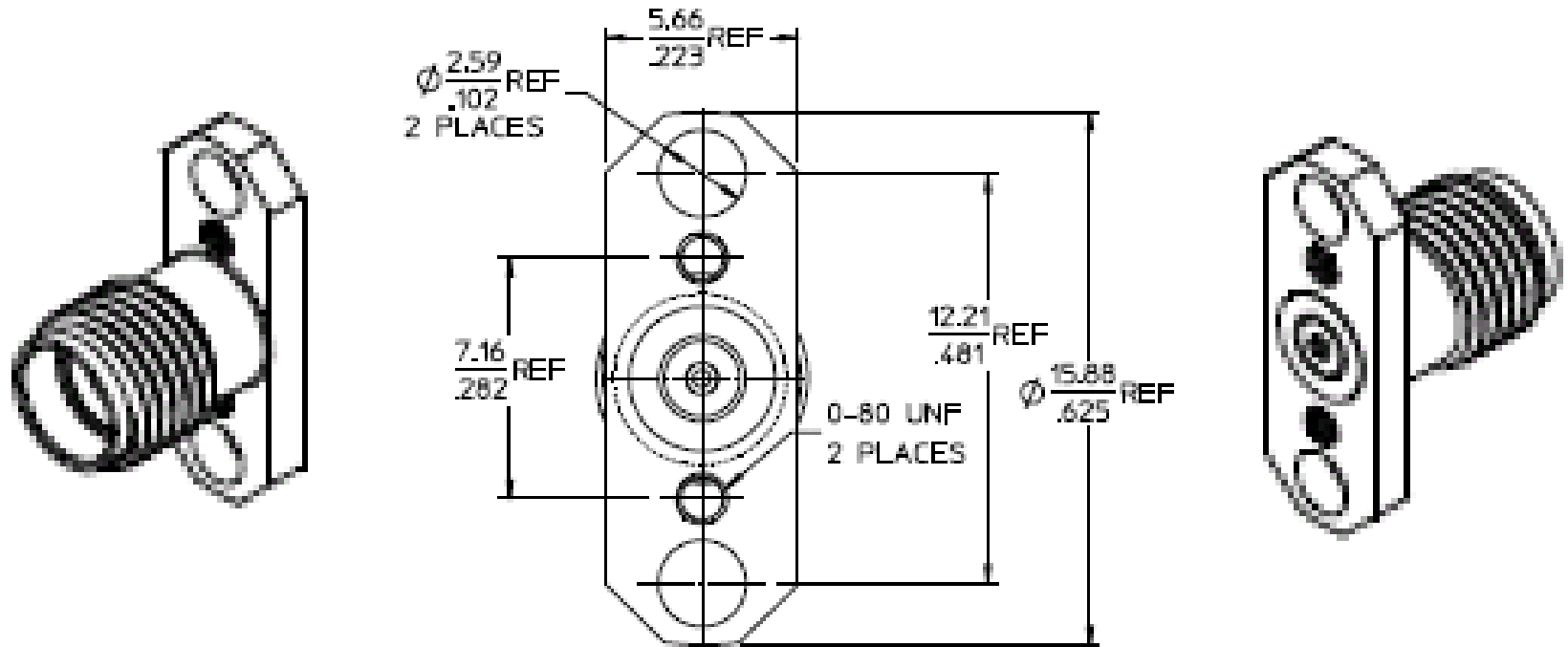
VNA CAPABILITY MUST BE VALIDATED



**30GHz, 2- OR 4-PORT VNA WITH
LOW-LOSS CABLES...**

Test Program Details

STANDARDIZED CABLES & SMA...



FLANGE-MOUNT SMA TYPE MOLEX P/N 73251-1850

Test Program Details

STANDARDIZED VNA CALIBRATION PROCEDURE...

Time Domain Reflectometry (TDR) calibration and benchmark board [2L32 see page 20] test procedure.

1.0 Purpose:
The purpose of this test is to calibrate the VNA and to verify the accuracy of the measurements.

1.0 Scope:
This procedure applies to the VNA and the benchmark board.

3.0 Required Tools:
VNA, Benchmark Board

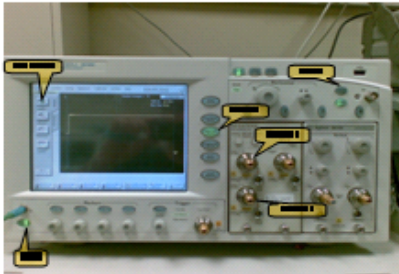
4.0 Special Definitions:

4.1 **Calibration**
The process of adjusting the VNA to measure the unknown.

4.2 **Accuracy**
The degree of closeness of measurements to the true value.

5.0 Calibration steps:

5.1 **Setup:**
Set up the VNA and the benchmark board (BB) by using the "Power" and other DDC settings approximately 18 minutes before starting the test.



5.2 **Connect the calibration board to the DDC connector of the benchmark board as shown in the diagram. Leave the board open.**

5.3 **Open the benchmark board as shown in the diagram.**

5.4 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.5 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.6 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.7 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.8 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.9 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.10 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.11 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.12 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.13 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.14 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.15 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

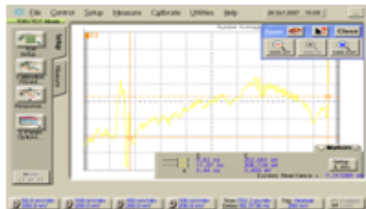
5.16 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.17 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.18 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.19 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**

5.20 **Connect the probe of the benchmark board to the DDC connector of the benchmark board.**



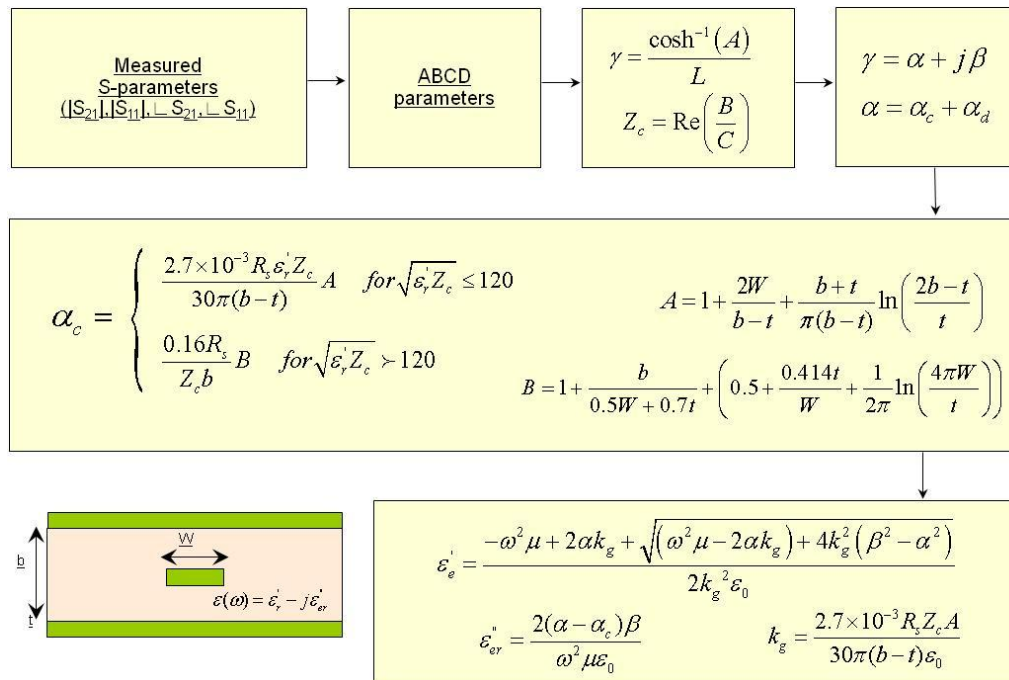
Test Program Details

S2P (OUTPUT) FILES OF OUR ACTUAL S-PARAMS AVAILABLE AS REFERENCE

```
!Agilent Technologies,E8364B,MY43040876,A.07.50.23
!Agilent E8364B: A.07.50.23
!Date: Saturday, February 23, 2008 18:57:00
!Correction: S11(Full 2 Port(1,2))
!S21(Full 2 Port(1,2))
!S12(Full 2 Port(1,2))
!S22(Full 2 Port(1,2))
!S2P File: Measurements: S11, S21, S12, S22:
# Hz S dB R 50
10000000 -2.378200e+001 5.673628e+001 -2.584631e-001 -1.376380e+001 -3.022304e-001 -1.376806e+001 -2.340713e+001
6.027135e+001
19368750 -2.642289e+001 3.853881e+001 -2.925846e-001 -2.174982e+001 -3.004267e-001 -2.168536e+001 -2.623681e+001
3.703846e+001
28737500 -2.745473e+001 1.856262e+001 -3.267293e-001 -3.080593e+001 -3.389186e-001 -3.078322e+001 -2.754905e+001
1.993869e+001
38106250 -2.797746e+001 2.983054e+000 -3.553250e-001 -3.985679e+001 -3.524945e-001 -3.985023e+001 -2.856044e+001
6.122039e+000
47475000 -2.863589e+001 -1.382138e+001 -3.932017e-001 -4.905007e+001 -3.875628e-001 -4.905552e+001 -2.902165e+001 -
8.903451e+000
56843750 -2.882035e+001 -2.572735e+001 -3.992082e-001 -5.837532e+001 -4.042186e-001 -5.839590e+001 -2.906086e+001 -
1.948173e+001
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5.532522e+001
94318750 -2.973300e+001 -7.703996e+001 -5.914595e-001 -9.588406e+001 -5.671583e-001 -9.575095e+001 -3.244051e+001 -
6.958324e+001
103687500 -3.051751e+001 -9.705671e+001 -6.107419e-001 -1.050000e+002 -5.979300e-001 -1.050000e+002 -3.372701e+001 -
```

Test Program Details

DRIVE S-PARAMS THRU CISCO/MST Dk/Df EXTRACTION ALGORITHM...



...TO GET Dk/Df SWEEP CURVES

How we'll get there...

1. Identify suppliers with VNA capability
2. Distribute test procedure and algorithm
3. Validate capability at sites (4-5 preferred)
4. Select materials with wide range of Dk / Df
5. Round-robin testing at participating sites
6. Find causes of variation; debug procedure
7. Calculate R&R, and if acceptable...
8. **Submit to IPC D-24 test methods committee**

Q and A

