Report on iNEMI Boundary-Scan Adoption Project Results and Future Plans

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Abstract

The increase in circuit densities and speeds are driving the reduction of electrical test point access for printed circuit assembly test. Boundary-scan technology (JTAG/IEEE 1149.x) will allow continued testability of printed circuit assemblies, but it requires that it is designed into semiconductor devices. Currently not all semiconductor vendors support boundary-scan. Wider availability of complying devices is necessary to enable cost efficient and effective board test for future designs. A project analyzing boundary-scan adoption by the industry was undertaken by the International Electronics Manufacturing Initiative (iNEMI) in 2009. Its objective was to assess the present status and ultimately motivate wider adoption of boundary-scan throughout the industry. To this end, the project group surveyed users of boundary-scan devices and board test development tools to identify the current levels of boundary-scan implementation in the industry today and projected short term future use. This paper presents the summarized results of the project's industry survey including the implementation status and the gaps identified to adoption of this technology by the industry. It also discusses the iNEMI follow on project plans which will leverage learning from this project in the subsequent work which will result in broader and potentially more focused usage of boundary-scan test.

Introduction

The iNEMI Boundary-Scan Adoption Project aimed to promote wider adoption of boundary-scan (JTAG/IEEE 1149.x) throughout the electronics industry, to encourage semiconductor suppliers to include the technology in their products, and to promote the development of tools by ATE (automated test equipment) suppliers to support boundary-scan based board test. The first phase of this project was to conduct an industry survey to determine how boundary-scan is currently being used, identify what issues boundary-scan users encounter, and how those issues impact results. The project team developed a detailed online questionnaire and solicited participation from the iNEMI membership and contacts, and promoted the survey through trade publications and the iNEMI website. An extended summary of the highlights of the survey is given elsewhere [1]. Results and conclusions from some of these key questions in the survey leading to the future work are given below.

The iNEMI Boundary-Scan Survey

The survey had five main objectives:

- gauge the penetration of IEEE 1149.x boundary-scan implementation in several industry sectors;
- identify familiarity with existing, new, and proposed boundary-scan standards;
- identify issues encountered by survey respondents while implementing boundary-scan;
- identify reasons why boundary-scan currently is not used;
- identify research areas for future iNEMI projects.

Survey Methodology

The survey focused on responses from two groups: Board/System Engineering and Semiconductor Engineering. Each group contributes its own unique perspective to designing and implementing boundary-scan. The initial, common section of the survey consisted of general information, such as name, company name and primary business sector, company's annual sales, and respondent's primary area of responsibility (Board/System Engineering or Semiconductor Engineering). Depending on the answers to the latter questions, the respondents were then directed to either the Board/System Engineering section or the Semiconductor Engineering section.

The Board/System Engineering section consisted of 51 questions addressing the following areas:

- industry (product) sector the respondent works in;
- knowledge level of assorted released and proposed 1149.x and related standards;
- importance of boundary-scan to design or production goals;
- current implementation level of boundary-scan based processes in product development and production test;
- frequency and impact of issues encountered in implementing boundary-scan;
- advantages/disadvantages of boundary-scan;
- plans for future implementation of boundary-scan in board/system level design and production test processes;
- types of devices for which the respondents would like to see boundary-scan offered in the near future.

Based on "Boundary-Scan Adoption - An Industry Snapshot with Emphasis on the Semiconductor Industry", by P. B. Geiger & S. Butkovich, which appeared in the Proceedings of the 2009 International Test Conference. © 2009 IEEE.

The Semiconductor Engineering section consisted of 23 questions that covered:

- knowledge of released and proposed 1149.x and related standards;
- current and planned support for boundary-scan standards;
- issues that have or could hinder successful implementation of boundary-scan in IC designs;
- target applications for the respondents' designs;
- boundary-scan design, simulation, and verification processes and associated issues;
- plans for future implementation of boundary-scan in IC designs.

Boundary-Scan Survey Results

Respondent Statistics

A total of 240 people, from 131 companies and 27 countries responded to the survey. Of the respondents, 86% classified themselves as Board/System Test Engineering and 14% classified themselves as Semiconductor Engineering.

In terms of company size (denoted by annual sales), the breakdown for the Board/System Test engineering respondents is given in Figure 1.

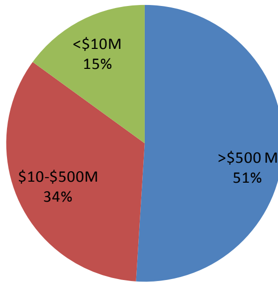

Figure 1 Company Size Break-down for Board/System Test Respondents

The majority of the Board/System Test Engineering respondents were Test Engineers. The overall job function breakdown for the Board/System Engineering respondents is given in Table 1.

Job Function	Response
Test Engineer	44.3%
Development/Test Engineering Manager	17.2%
Test Equipment Provider	9.9%
Designer	9.4%
DFT Consultant	8.9%
Manufacturing Manager	5.4%
System Architect	1.5%
Service and Support	1%
System-Level Applications	1%
Other	0.9%
Field Service Engineer	0.5%

Table 1 Board /System Test Respondent Job Functions

The Board/System Test respondents were drawn from across the electronics industry, as can be seen in Table 2. The majority (27.7%) were in the Netcom industry sector (telecom, datacom, and networking), followed by Test Equipment/Services Providers (17.3%) and Military/Aerospace (11.4%).

Industry Sector	Response
Netcom	27.7%
Test Equipment/Services	17.3%
Military/Aerospace	11.4%
Office/Large Business Systems	10.9%
Consumer/Portable	9.9%
Other	8.4%
EMS/Contract Manufacturer	5.9%
Medical	5.4%
Automotive	3.0%

Table 2 Industry Sector Break-down for Board/System Test Respondents

For the semiconductor engineering respondents, the majority of respondents were employed in $500 million + companies. Figure 2 shows the company size (in annual sales) for Semiconductor Engineering respondents.

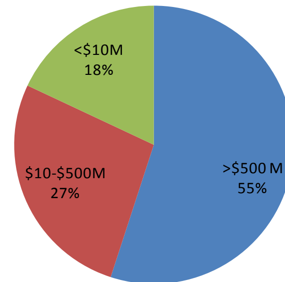

Figure 2 Company Size Break-down for Semiconductor Respondents

Table 3 shows the overall job function break-down for the Semiconductor Engineering respondents. The majority were described as IC DFT/Test Engineer (34.4%) and IC Logic Designer (25%).

Job Function	Response
IC DFT/Test Engineer	34.4%
IC Logic Designer	25.0%
IC Engineering Manager	18.1%
IC Architect	12.5%
IC Floorplan Designer	3.1%
IC I/O Designer	3.1%
Other	0%

Table 3 Semiconductor Respondent Job Functions

In terms of their company business profile, the majority of Semiconductor Engineering respondents defined their company's business as "IC designer" (51.5%); the rest were divided into IC fabricator (15.2%) and "Other" (15.2%). The majority of "Other" responses were third-party semiconductor services companies. OEMs and test equipment providers (6.1% each).

IEEE Std	Revision	Test Type	Application
1149.1-2001 (BSDL added 1994)	Update (1st Release 1990)	Digital BSCAN	Connectivity (DC)
1149.4-1999	1st Release 1999	Analog BSCAN	Connectivity (Mixed signal)
1149.6-2003	1st Release 2003	Advanced I/O BSCAN	Connectivity (AC-coupled) Differential, Serial Bus, High-Speed I/O, SerDes.
P1149.7 (cJTAG) Initiative	In Review. Vote expected in CY2009. (Superset of 1149.1)	Compact JTAG. BSCAN with reduced TAP pin count (2 rather than 4 pins) total.	Extended functionality of device integration, power management, application debug, and device programming. SoC and SiP test.
1500-2005	1st Release 2005	Embedded Core BSCAN	Multi-core ASIC Test
1532-2002	1st Release 2002	In-System Configuration BSCAN	In-system access & configuration of Programmable Devices. FPGA, ePLD, FlashRAM, etc.
P1581 Initiative	In Review. Draft to IEEE expected in CY2009	I/O Loopback (w/o adding pins to device). Augments 1149.1	Non-BSCAN Memory Device Test (DDR,SRAM,FLASH)
P1687 (iJTAG) Initiative	In Review. Vote expected in CY2010	Embedded Instrument Gateway access through 1149.1 TAP	Embedded Instrumentation control and access
SJTAG Proposed Initiative (IEEE has not assigned an number yet)	Request to IEEE for PAR in CY2009	Inter-module and Backplane BSCAN	System-based Connectivity (DC)
P1149.8.1 Selective-Toggle Initiative	In Review. Vote expected in CY2009.	Analog-Digital BSCAN.	Connector & Non-BSCAN Device Test. Powered OPENs Test.

Table 4 Boundary-Scan Standards and Initiatives at the time of the survey [1]

Knowledge and Support for Boundary-Scan Standards and Initiative

"Boundary-scan" is a generic term commonly used to describe several IEEE standards released since 1990, with 1149.1 and 1149.6 being the most common. Several initiatives for new standards that enhance or extend the effectiveness of boundary-scan for newer technologies are in process. Table 4 above describes the boundary-scan standards and working group initiatives at the time of the survey.

All respondents were asked questions about their knowledge of and current and future support for these standards and initiatives.

For Board/System Test Engineering: The standards with which respondents had the most working knowledge were the oldest: 1149.1, 1149.6, and 1149.4. Newer proposed standards had the least amount of familiarity: P1687, P1581, and P1149.7.

For Semiconductor Engineering: semiconductor engineers were asked about their familiarity with boundary-scan standards to gauge knowledge of the standards that are commonly used for loaded circuit board test. There was widespread familiarity with the long existent 1149.1 boundary-scan standard, but newer standards such as 1149.7 [2] and P1687 appeared virtually unknown.

Lack of a large number of responses from programmable logic device suppliers may have resulted in the low familiarity rate with the IEEE 1532 standard.

It was noted that several IEEE proposed standards, such as P1581 Static Component Interconnection Protocol [3] and P1687 Methodology for Access to Embedded Test and Debug Features, are still in the development stage and have not been widely promoted to the technical community.

Board/System Engineering Survey Results

The Board/System Engineering section included in depth questions on a broad range of topics related to boundary-scan. The responses highlighted the extent to which boundary-scan is used, its importance in board and system design and development, and the standards that are supported.

How important is Boundary-Scan to Board/System Test Engineers?

As can be seen in Figure 3, 49% of Board/Systems engineers identified boundary-scan as "Highly important," stating that they cannot meet goals if it fails to work, and 30% rated it as "Moderately important," indicating that they could work around most unsolvable boundary-scan issues encountered.

Another 19% said that they only use boundary-scan to fill in test coverage or are "dabbling" in it; and only 2% stated that it is "Not important" and that they do not use it.

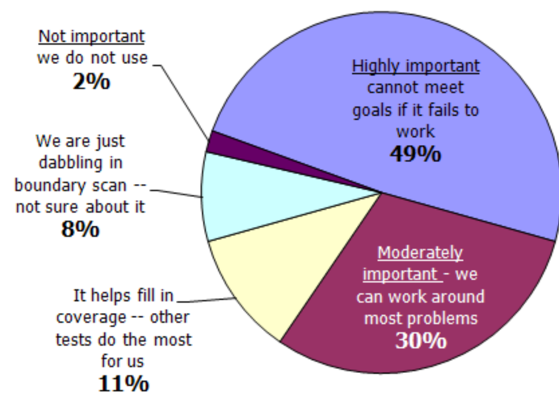

Figure 3 Importance of Boundary-Scan to Production Goals [1]

The survey also showed the significant use of boundary-scan throughout the engineering development and production processes. According to Board/System Engineering respondents, boundary-scan is most often used in production and pre-production circuit board testing (88% and 72%, respectively). In addition, 65% said they use it in circuit board debug and repair; 63% use it on prototypes, and 41% use it in circuit board functional test.

When asked more detailed usage questions the respondents indicated that the top five places boundary-scan is currently used are:

- structural test (opens/shorts, ICT, memory interconnect);
- programming FLASH and programmable logic devices;
- device version verification;
- debug and diagnosis on production and prototype circuit boards;
- nail reduction for ICT fixtures.

60% of the respondents reported that they use boundary-scan in multiple functional areas on the same product.

How Does Boundary-Scan Affect Product Development Time and Cost?

Certain questions asked aimed to ascertain the cost/benefit of the use of Boundary-scan. When asked if boundary-scan had increased or reduced product development costs, 41% of respondents reported cost reductions, 25% were neutral, and 17% reported increased cost. People noted in comments that, although there may be up-front costs, boundary-scan saved money in the long run.

Fifty respondents gave specific examples of how boundary-scan has reduced development costs. These included:

- significantly faster debug of manufacturing defects in prototypes, allowing development engineers to concentrate on design verification;
- faster prototype turn time at no additional cost;
- reduced cost of in-circuit test fixturing and development.

The survey also asked for examples of how boundary-scan had increased development costs. Twenty-three people replied, and their answers can be summarized as:

- Cost of boundary-scan hardware and software;
- Boundary-scan parts more expensive than traditional parts.

When respondents were asked if implementing boundary-scan reduced or increased development time, "Reduced time" and "Neither" were tied at 36%; and 13% reported that boundary-scan increased development time.

Many of the examples provided by the 39 respondents who said boundary-scan decreased development time were similar to those given for decreased development cost:

- faster test and debug of prototype boards, resulting in faster prototype turn time and higher quality prototypes delivered with few, if any, manufacturing defects;
- easier and faster development of in-circuit and functional board test;
- simplified FLASH and PLD part programming process;
- reduced testpoint requirements result in less expensive test tooling.

It was noted that the common theme in the 15 examples submitted for ways that boundary-scan increased cost, was added time for DFT implementation in the designs.

The Board/System Engineers were asked what benefits were derived from boundary-scan other than cost/time improvements. There were 109 responses to this question, many of which were similar to the cost or time responses:

- increased PCBA test coverage at prototype builds;
- higher fault coverage in production than with standard tests with increased fault identification;
- ability to maintain structural test coverage at ICT despite reduction in test point access ;
- easier and faster FLASH and PLD part programming and verification;
- ensures product quality and reliability (at reduced development time and cost).

Use of Boundary-Scan to Test Non-Boundary-Scan Devices

The majority of Board/System Engineers said they use boundary-scan to test non-boundary-scan devices, including:

- simple combinational logic (74%);
- simple sequential logic (66%);
- resistors and resistor networks (65%);
- SRAM/DRAM interconnects (80%);
- FLASH memory interconnects (74%).

Other devices being tested by respondents using boundary-scan included LEDs, I2C/SPI parts, A/D or D/A converters, and connectors/sockets. Significant issues were reported when testing non-boundary-scan devices. SRAM/DRAM interconnects were cited most often for causing problems when tested with boundary-scan (58% said they occasionally encountered problems and 28% said they frequently did), followed by FLASH memory interconnects (62% occasionally and 20% frequently).

Verifying Semiconductor JTAG Compliance

Respondents in the Board/System Test Engineering section were asked if their companies do anything to verify that the devices they receive from semiconductor suppliers are JTAG compliant. 48% of respondents replied "Yes" and 52% replied "No". 70 of the 93 respondents who said "yes" described the methods used to verify compliance. The most common are as follows:

- verify boundary-scan functionality in the silicon during component validation;
- verify the devices by developing production tests that use boundary-scan;
- run a BSDL file syntax check;
- specify compliance in our procurement contracts;
- do DFT and/or verify boundary-scan is in data sheets.

Issues Encountered When Implementing Boundary-Scan

Respondents were also asked what percentage of time they encountered major, minor, or no issues with boundary-scan, based on their experience with new printed circuit boards entering production. The responses were averaged; 44% had no issues, 40% had minor issues, and 16% had major issues. The top 3 major issues reported were:

- problems related to BSDL files (non-compliant, "bad" or "wrong" BSDLs);
- non-compliant devices (devices that stray from IEEE1149.x standards);
- DFT issues.

The most common problem cited was bad BSDL files. Seventy-five percent of respondents said they occasionally had

problems with bad BSDL files, and 18% said they frequently had problems. Other leading sources of problems were board design not being correctly implemented for boundary-scan, compliance issues with ICs and problems with tester or software.

When asked how boundary-scan issues affected them, 60% of the respondents said problems occur but are basically acceptable. Additional resources are required for success according to 25% of the respondents, 20% said they have very few issues, and 10% question the value versus cost of boundary-scan.

The survey also tried to ascertain issues that would prevent Board/System Engineers from using boundary-scan. When asked the majority response was devices that don't support boundary-scan (78%), followed by poor DFT on the board (49%). An additional 44% say they cannot get BSDLs from silicon suppliers and 12% cited concerns about potential security holes in the boundary-scan interface.

Attributes Important to Board/System Engineers When Choosing a Semiconductor Supplier

Board/System test engineers were asked what attributes they considered the most important in influencing the choice of semiconductor suppliers for design-for-test purposes. More than 80% regarded boundary-scan support features as either "Important" or "Very important" in device selection. The factors that were of greatest importance to the Board/System Test Engineers were the availability of boundary-scan cells on a high number of the device signal pins, the accuracy of the device documentation and the availability of BSDL files.

Semiconductor Engineering Survey Results

Current and Planned Support for Boundary-Scan in Semiconductor Devices

The survey results indicated that the general intention of many semiconductor designers is to support boundary-scan. No semiconductor engineers responded that they never support boundary-scan. This is interesting as it is contrary to the perception of many board test engineers that many semiconductor suppliers do not support boundary-scan. There were no respondents that indicated that they never provide a boundary-scan interface when applicable, and more than half indicated that it is always a requirement for their designs.

Respondents were asked what factors determine which pins will have boundary-scan cells attached; 61% indicated that they support all eligible pins and 14% answered they support the most requested pins and ignore the remainder. Silicon real estate is the limiting factor for 11% of the respondents, and 7% cited library cell support.

In most cases there is an attempt to assign a boundary-scan cell to any eligible pin. Note that this does not mean that all of the device pins will receive boundary-scan cells. Other factors, such as operational speed or differential and analog signals were indicated as factors in the ability to place a boundary-scan cell.

Boundary-Scan Compliance in Semiconductors

Figure 4 outlines the response to the question on what percentage of devices designed were intended to be 1149.1 compliant. 53.8% of the Semiconductor Designers replied that it was their intention to include compliant boundary-scan on all of their devices while only 7.7% responded that boundary-scan was not intended to be included. The remaining respondents reported that some percentage of devices designed would receive 1149.1 boundary-scan.

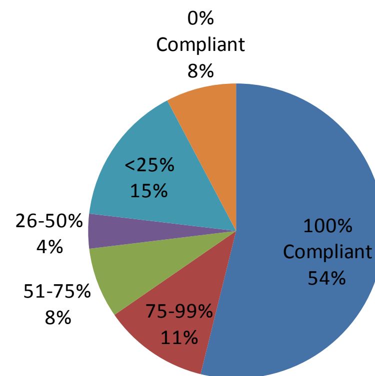

Figure 4 Percentage of Devices Designed Intended to be IEEE 1149.1 Compliant

Semiconductor designers were also asked whether their group had ever intentionally developed a non-compliant boundary-scan device. The majority, 70% of the respondents answered "No", while 29.6% said "Yes". Several differing reasons were given for non-compliance:

- all aspects of the 1149.x specification cannot be completely supported;
- decisions to add boundary-scan late in the design cycle forced trade-offs;
- industry tools need more flexibility;
- using the JTAG interface to configure the device requires TCK to be synchronous to the system clock;
- pin signal type prohibits Boundary-scan implementation.

When asked what actions were taken when devices designed to be 1149.1 compliant were found to be non-compliant, 40.7% of the respondents said they had not experienced that issue. When problems were found with compliance, the most common solution, indicated by 29.6% of the respondents was to provide documentation of the problem which in many cases included a work-around. In others cases, 18.5% of the respondents said they committed to repair the issue in a future revision of the device and 11.1% indicated that they would redesign the device to fix the issue.

Designers indicated that their intention to develop semiconductors supporting the IEEE 1149.6 Standard for Boundary-Scan Testing of Advanced Digital Networks, also known as "AC Boundary-Scan." was much lower than their intention to support the IEEE 1149.1 standard. Forty percent responded that they did not have a current requirement or expect one in the future. Thirty-three percent replied that they are currently using 1149.6. As shown in Figure 5, the remainder intends to support 1149.6 in the next six months to three years. The 1149.6 standard is more recent than the others and may be considered more difficult to implement from the perspective of available tools [4].

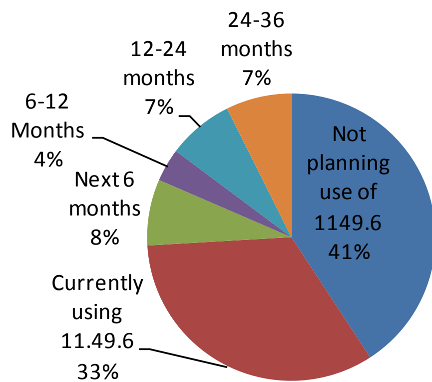

Figure 5 Current/Future Plans to Produce 1149.6 Designs

Conclusions

Clearly, boundary-scan is a very important semiconductor feature to Board/System Test Engineers. 98% of the respondents use boundary-scan and 79% rated boundary-scan as highly or moderately important to their production goals. It is widely used in circuit board test and debug.

Semiconductor engineers have a good working knowledge of the released boundary-scan standards and the semi-conductor industry in general supports the released standards.

Based on the survey, there were a number of recommendations identified:

- The semiconductor industry should make a greater effort to produce correct and compliant BSDLs. The primary issue reported by Board/System Engineers was incorrect or non-compliant BSDL files.
- BSDLs need to be easier to obtain. Almost 45% of the Board/System Engineers voiced this need.
- Improvements are needed in verifying JTAG hardware compliance. Currently, many Board/System Engineers find noncompliance when they generate a test and try to implement it.
- More involvement with the P1581 working group will help implement the standard in future memory devices. This will greatly assist the 80% of test engineers who today struggle to test these devices with no on-chip testability.
- Ssemiconductor industry involvement in other proposed boundary-scan standard working groups and early adoption of those standards is very important and will help address the significant number of issues encountered when trying to implement tests for non-boundary-scan parts.

Description of Boundary Scan Phase 2 Project: Structural Test of External Memory Devices

A major gap identified by the 2009 iNEMI Boundary-Scan survey was that over 80% of board test engineers today struggle to implement boundary-scan based connectivity testing on PCBAs that have soldered down memory devices with no on-chip testability. SRAM/DRAM interconnects were cited most often as having issues.

The primary reasons for the issues are:

- Loss of standard test point access due to circuit density and signal integrity concerns,
- Memory signal/speed timing requirements exceed capability of test equipment,
- No “test mode” designed into memory devices to allow easy, straightforward generation of a structural test.

These issues contribute to significant loss of structural test coverage and are compounded as the memory devices get larger and faster, circuit densities increase, and 3D packaging continues to challenge test access and effective test strategies.

A new project proposal has been defined and approved for start within iNEMI, which will examine and evaluate potential solutions and determine what the current and future best industry practices are [5]. This will include evaluating the following:

- feasibility of P1581 Static Component Interconnection Test Protocol & Architecture to help solve this problem,
- capabilities of standalone boundary-scan test solutions,
- Powered Opens In-Circuit Test solutions
- boundary-scan processor controlled test.
- capabilities and limitations of Built-in Self Test.

The cost benefits and tradeoffs of all of these options will be quantified.

The project goals are to compare the potential solutions, identify technology gaps, and determine industry best practices for structural test of memory devices. An additional goal will be to drive better alignment, predictable results, and ease of use through the adoption of P1581 and P1687.

Business impacts are expected in cost improvements for overall product test development, improvements in time to ramp on new products supported, improved product quality as a result of more effective/efficient test coverage, and reduced cost of test and failure diagnostic. The iNEMI team will work to quantify the business impacts realized.

The timeline of this project is to start up the study during Q3 2010, complete the data collection of various study elements by Q2 2011, analyze results during Q3 2011, and complete the project and publish results during Q4 2011.

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