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International Electronics Manufacturing Initiative

iNEMI HFR-Free Programs

ENFIRO Conference

Stephen Tisdale - Intel

March 15, 2011

Advancing manufacturing technology

Current (Active) Programs

HFR-free High Reliability PCB Project

HFR-free Leadership Project

- PCB Materials WG
- Signal Integrity WG

Other Environmental Projects

PVC Alternatives Project

ECO Impact Evaluator for ICT Equipment

Drivers for Low-Halogen Electronics

Driver	***Global Environmental Responsibility*** *Non-Governmental Organization (NGO) pressure to address environmental issues*
Materials Involved	***All Halogenated Flame Retardants*** *Brominated Flame Retardants (TBBPA is main FR in substrate & PCB Materials)* *All Chlorinated Flame Retardants and PVC*
Standards *(PCB Material Only)*	**IEC 61249-2-21** **JPCA-ES-01-1999** **IPC - 4101B**
Guidelines *(Solid State Devices Only)*	***JEDEC JEP-709*** *(Expanding Scope to Include Passives / Connectors)*

Various Industry Standards / Guidelines are in place

Supply Chain Alignment / Definition Critical

iNEMI's HFR-Free Position

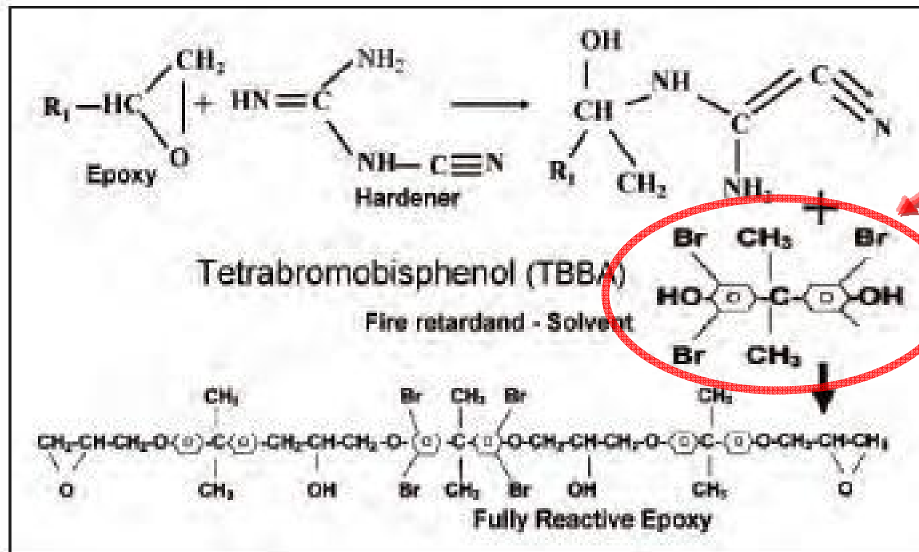
iNEMI supports removal of:
Halogenated Flame Retardants (HFRs)
and Polyvinyl Chloride (PVC)

iNEMI Position Statement Can Be Found Here :
http://thor.inemi.org/webdownload/projects/ese/HFR-Free/Low-Halogen_Def.pdf

Low-Halogen Material Changes

HFR-free - What Changed?

Low-Halogen changes the flame retardant used for epoxy laminate (FR4) materials



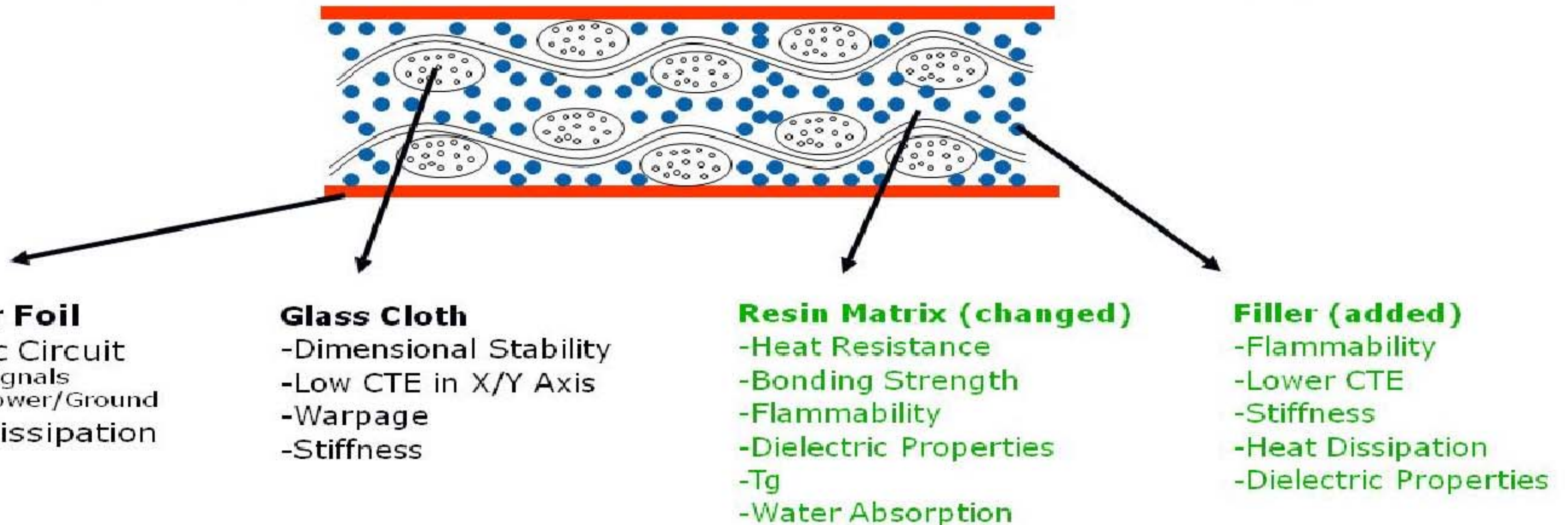
Tetrabromo bisphenol-A (TBBPA) is the current halogenated flame retardant for all laminate epoxy systems

Reactive flame retardant that is incorporated into the epoxy chain and volatilizes at burning temperatures

Halogen-free - What is different in the PCB?

Halogen-free changes the flame retardant used for epoxy laminate (FR4) materials

- Resin epoxy backbone modified – Organo-phosphorous or nitrogen compounds substituted for TBBPA
- Fillers added – SiO_2, metal hydroxides, and/or other compounds



Copper Foil
- Electric Circuit
  - Signals
  - Power/Ground
- Heat Dissipation

Glass Cloth
- Dimensional Stability
- Low CTE in X/Y Axis
- Warpage
- Stiffness

Resin Matrix (changed)
- Heat Resistance
- Bonding Strength
- Flammability
- Dielectric Properties
- Tg
- Water Absorption

Filler (added)
- Flammability
- Lower CTE
- Stiffness
- Heat Dissipation
- Dielectric Properties

Halogen-free changes the fundamental composition of FR4 material with no one choice dominant

Low Halogen (HFR-free) PCB - Challenges

HFR-free PCB Implementation	Potential Impact
Epoxy Backbone Change	– Mechanical degradation of resin strength resulting in lower peel strength & increase material brittleness – Decomposition temperature (Td) of the resin is increased. – Change to Glass Transition Temp (Tg) – **Impact to resin electrical properties (Dk and Df) due to moisture absorption** – Change to resin CTE properties affecting via reliability and assembly compatibility.
Fillers	– **Fillers increase the Dielectric Constant (Dk) of the material impacting impedance targets, crosstalk and other design considerations** – Fillers can lower the CTE and increase the rigidity of the material. – Fillers can lower the peel strength of the laminate. – Fillers can degrade the assembly of the laminate affecting process cost and via reliability.

Problem Statement

- **A potential reduction in performance margin has been observed from the FR-4 laminates being used today**
  - Loss of margin in thermo-mechanical performance
  - Loss of margin in electrical performance
- **High-speed bus designs may be problematic due to electrical properties of these materials**
  - Potential for increasing the cost of the system
- **Wider fluctuation of vendor to vendor PCB electrical performance compared to FR4 designs**
  - Multiple variations of flame retardants in use

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HFR-Free High Reliability Program

Program Manager:

Stephen Tisdale, Intel

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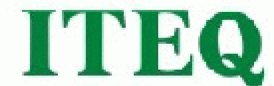
iNEMI HFR-Free High Reliability PCB Project

- **Focus is on Hi-Rel (Server) Market Segment Application Space**
- **PCB and PCBA components are BFR-free**
- **Board Thicknesses are 0.093” & 0.125” (MEB’s) & 0.116” (Agilent)**
- **PCB Material should be LF compatible, low / med loss and HVM capable**
  - 8 BFR-free Materials Identified with 1 Halogenated Material as Control
- **7 of 8 BFR-free TV’s have been completed and are being tested (estimated completion beginning Q2’11)**
  - 1 BFR-free and FR-4 Control TV continues to be built (Completion Mar’11)

	MEB	MEB	Agilent
Layer Count / Thickness	18 Layer / 0.093”	24 Layer / 0.125”	20 Layer / 0.116
Drill Sizes	8mil / 10mil / 12mil	10mil / 12mil / 14 mil	
Pitch	0.8mm / 1.0mm	0.8mm / 1.0mm	
Reflow Temps	245C & 260C	245C	260
# Reflows	6x & 10x	6x & 10x	6x & 10x

All Materials are Phenolic Resin Based

HFR-Free High Reliability Project Members



HFR-Free Leadership Program

Program Manager:

Stephen Tisdale, Intel

HFR-Free Signal Integrity

Chair: Stephen Hall, Intel

Co-chair: David Senk, Cisco

HFR-Free PCB Materials

Chair: John Davignon, Intel

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iNEMI HFR-Free Leadership Program

Consortium Objectives

1. **Identify technology readiness, supply chain capability, and reliability characteristics for “HFR-free” alternatives to conventional printed circuit board materials and assemblies**
   – Spans electrical and mechanical properties

2. **Define technology limits for HFR-free materials across all market segments**
   – Initial focus is on client platforms (desktop, notebook) in 2011 timeframe
   – Goal is to drive laminate supplier slash sheet content

HFR-free Technology Leadership Project

Stephen Tisdale, Intel – Chair
HFR-Free Leadership Program

HFR-Free PCB Materials
Chair: John Davignon – Intel

Identify key thermo-mechanical performance characteristics and determine if they are in the critical path for the HFR-free PCB material transition.

HFR-Free Signal Integrity
Chair: Stephen Hall - Intel
Co-Chair: David Senk - Cisco

Ensure there is no degradation of electrical signals in HFR-free PCB materials, base on investigation of permittivity and loss as well as how they are impacted by moisture absorption in new HFR-free materials.

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iNEMI HFR-free PCB Materials

Chair: John Davignon, Intel

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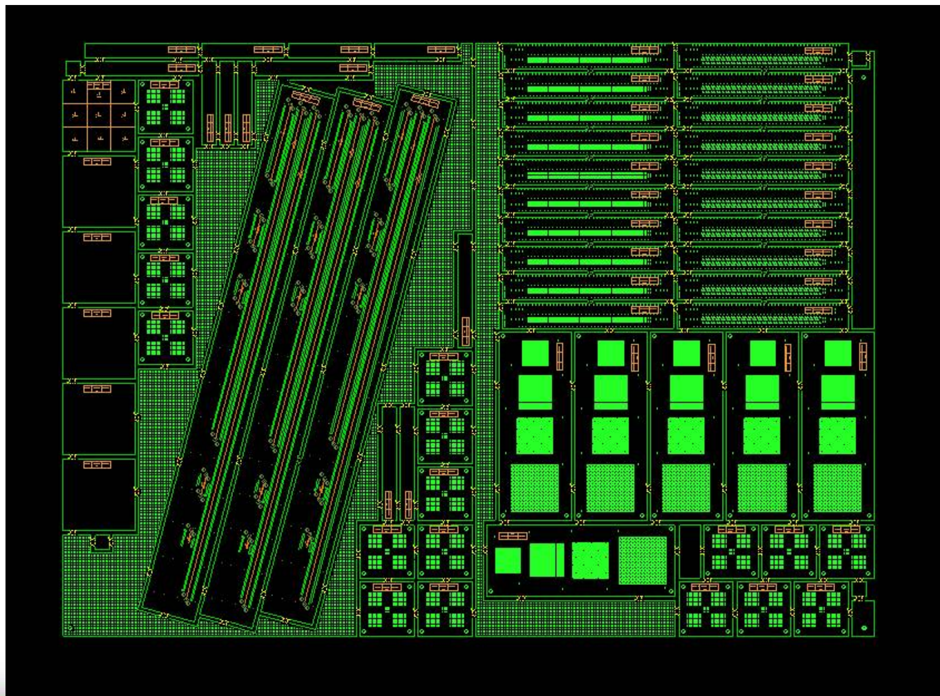
iNEMI HFR-free PCB Materials WG Strategy

- **Define and implement quantifiable data into the HF Laminate Suppliers Datasheets that will assist in material selection by users**
- **Define a "Test Suite Methodology" which meets the quality and reliability requirements of the chosen market segments**
- **Ensure the Industry Laminate Suppliers have the capability and capacity to support the industry HF laminate requirements**

Test Suite Methodology

Test Methods Under Evaluation		
Glass Transition Temperature (Tg)		Stiffness/Flexural Strength
Decomposition Temperature (Td)		Pad Adhesion (CBP/Hot Pin Pull)
Coefficient of Thermal Expansion (x,y,z)		Interconnect Stress Test (IST)
Moisture absorption		Conductive Anodic Filament (CAF)
Rework (Pad Peeling)		Lead Free Reflow Test: Delamination
Permittivity (Dk)		Charpy Impact Test
Total Loss (Df)		Simulated Reflow Test



10 Layer Mobile Stack-up

	Description	Layer Type	Thickness	
Layer 1	Plated 1/2 oz Cu		1.6	mils
	Prepreg		3	mils - 1 ply 1080
Layer 2	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 3	Unplated 1 oz Cu		1.3	mils
	Prepreg		4.2	mils - 1 ply 2116
Layer 4	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 5	Unplated 1 oz Cu		1.3	mils
	Prepreg		4.2	mils - 1 ply 2116
Layer 6	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 7	Unplated 1 oz Cu		1.3	mils
	Prepreg		4.2	mils - 1 ply 2116
Layer 8	Unplated 1 oz Cu		1.3	mils
	Core		4	mil core - 1 ply 2116
Layer 9	Unplated 1 oz Cu		1.3	mils
	Prepreg		3	mils - 1 ply 1080
Layer 10	Plated 1/2 oz Cu		1.6	mils
			48.2	

iNEMI Materials WG - Phase 2 Update

- **Two Proof of Concepts (POC) lots have been built to verify the Test Suite Methodology test vehicle/coupon design and test methods. 80% of Test Methods have been ratified**
  - Focus on determining the repeatability and reproducibility of the test methods across multiple sites
- **Final "Test Suite Methodology" Design completed with all test structures finalized**
  - Test Vehicle design has been finalized and Gerber data loaded to the iNEMI ftp site
- **All laminate builds are completed (6 HFR and 3 FR4 laminates)**
- **Phase 2 Schedule:**
  - 9 laminate builds have been completed
  - Laminate Testing Scheduled Completion Q2'11
  - Final analysis of Phase 2 results Q2'11

PCB Summary - Benefits

- **We are changing the way that data is reported on the Laminate datasheets.**
  - The test methods will be precisely defined
  - The test methods will be performed on a “product like” construction for more relevant data
- **The data reported will enable:**
  - A true comparison of material properties and responses between laminates
  - OEM/ODM’s to set envelopes for the material properties based on the market/BU sector that mitigate risk factors for that sector
  - PCB Designers to pick cost effective laminate materials that are suitable to their products/market segment
  - Method of directing Laminate Suppliers how to improve laminates by specific properties or responses

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iNEMI HFR-free Signal Integrity

Chair: Stephen Hall, Intel
Co-Chair: David Senk, Cisco

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iNEMI HF Signal Integrity WG Strategy

Identify HFR-free electrical "envelopes" required by each company in the consortium

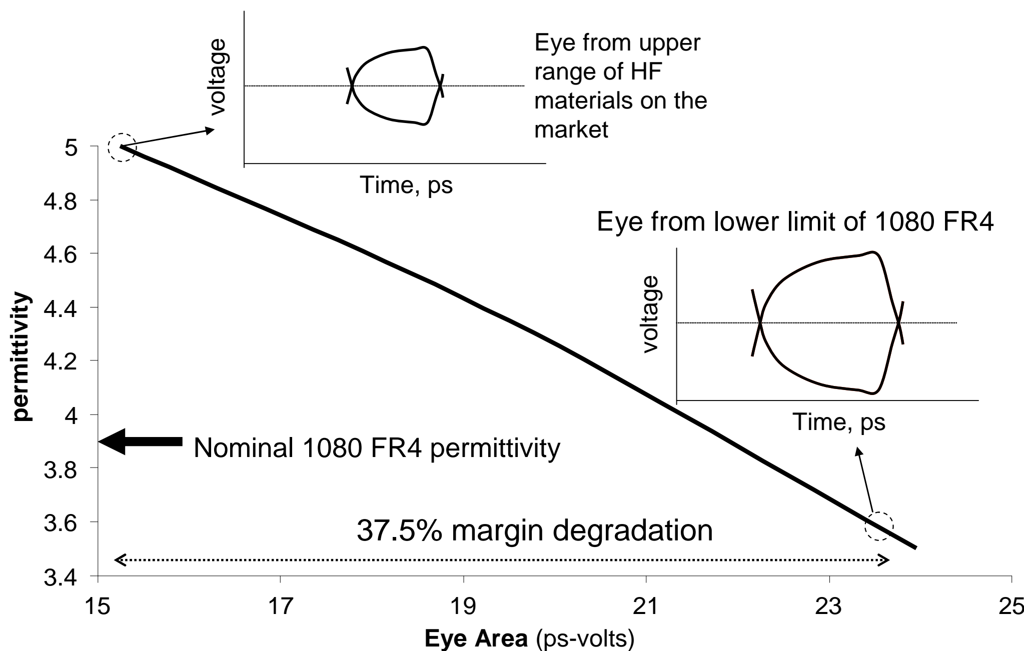
Develop a common measurement methodology

Characterize available HF dielectrics & map into requirements

Communicate requirements to the material vendors so they know what the industry wants

Performance of HF PCB vs. FR4

- ✓ **HFR-free PCB materials on the market tend to have higher permittivity (Dk) values than FR4**
  - ✓ HFR-free Dk ~ 4.2 – 5.0 (1080)
  - ✓ FR4 Dk ~ 3.6-3.9 (1080)



Simulation of three coupled 10" 50Ω microstrip lines; dielectric thickness varied to maintain Z_o; layout rules similar to DDR buses (W/S/W=4/12/4)

- ✓ **Higher permittivity (Dk) reduces bus performance**
  - Thicker layers for same Z_0 increases crosstalk
  - High crosstalk drives increased trace separation & more layers (increased cost)
- ✓ **HFR-free losses tend to be better than FR4 & help compensate for crosstalk for some buses**

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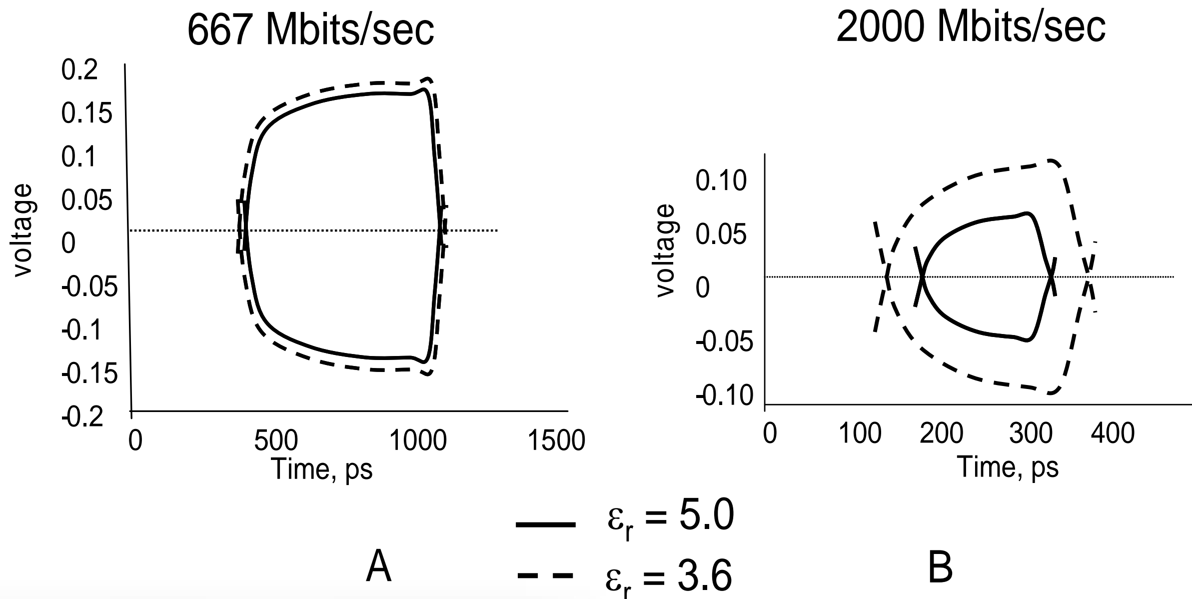
Scaling HFR-free bus speeds

✓ **Margin reductions gets *worse* for faster buses**

- HFR-free materials with high permittivity may be adequate for lower speed buses, but can be problematic at higher speeds
- FR4 also places limitations on high-speed buses, but HFR-free exacerbates problems on crosstalk dominated buses like DDR
- HFR-free PCBs can make it more difficult for buses to scale with Moore's Law



Simulation of three coupled 10" 50Ω microstrip lines with layout rules similar to DDR buses (WSW=4/12/4)

Critical Electrical Parameters

- ✓ **In addition to Permittivity, other critical electrical parameters of HFR-free materials must be assessed**
  - Each new formulation of flame retardants will have unique electrical parameters → non-standard electrical behavior
  - Must ensure all critical electrical parameters remain within acceptable bounds

Parameter	Other names	Design influences
Permittivity	**Dk, ε_r, dielectric constant**	**Characteristic impedance, Propagation velocity, crosstalk**
Loss tangent	**Df, tanδ, dissipation factor**	**Signal attenuation**
Moisture absorption	**Environmental effects, humidity**	**When dielectric materials absorb water, Dk & Df increase.**

iNEMI Signal Integrity WG Status

- **Common measurement method developed by CISCO to characterize the critical parameters (S3 method)**
  - Material vendors (in the WG) agreed to use this method for reporting numbers on the data-sheet
    - S3 measurements compared to split post resonator measurements (SPR assumed to be the golden standard for accuracy)
- **Completed round robin testing phase; proved the reproducibility and repeatability of the S3 test method**
  - Round robin results show excellent reproducibility of measurements across 6 members
    - Lab-Lab variation within 4% for Dk, 5% for Df.
  - Within lab repeatability quantified to be within 1% for Dk, 2% for Df
    - 5 measurements taken over 5 sequential days

Electrical Summary

HFR-Free Laminates have increased permittivity (Dk)

Higher Dk impacts high speed buses; Biggest impact is DDR interface

Limits can be placed on the permittivity so that FR4 and HFR-free PCBs are interchangeable for a single design for 2011 Platforms

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iNEMI HFR-free Leadership Project Schedule

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Proposed Timeline

		Phase #1				Phase #2				Phase #3	
2009				2010				2011			
Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4

- 2009 Q1: Condense brainstorm list
- 2009 Q2: PCB Material & SI Workgroup membership finalized. Assign owners and/or subteam
- 2009 Q3: Identified Test Methods, Test Structures and Critical dielectric parameters/limits
- 2010 Q2: Decide on TV construction and start Test Structure designs
- 2010 Q3: Complete POC Test Structure Validation Build
- 2011 Q1: Test Methods verified, Phase 2 build complete and under test
- 2011 Q2: Complete analysis of data from Phase 2 test suite builds and start verification OEM/ODM builds
- 2011 Q3: Complete EOM/ODM Verification Testing
- 2011 Q3: Deliver the HF dielectric electrical requirements to the material suppliers and ODMs
- 2011 Q4: Final Report with Webinar

Firms Participating in the Program

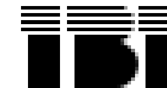
invent

CISCO

FLEXTRONICS

Celestica

QUANTA COMPUTER



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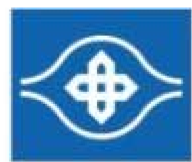

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Discussion