Pb-free Assembly, Rework and Reliability Analysis of IPC Class 2 Assemblies

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Outcome of presentation

Walk away with an understanding of a 3 year iNEMI project and its findings for Pb-free IPC Class 2 processes for assembly, rework and reliability

Outline of today’s presentation

- Background and overview of 3 year project
- Assembly process development & findings
- Rework process development & findings
- Process robustness evaluation
- Top 10 Key Conclusions
- Summary
- Acknowledgements

Background and project overview

- Pb-free project is one of many projects within iNEMI’s Environmentally Conscious Electronics Technical Integration Group setup to meet the EU deadline for RoHS compliant products.
- Pb-free project took three years, and was a consortium of 19 of the 70 iNEMI companies, including one university, formed to develop and test Pb-free manufacturing processes for IPC Class 2 assemblies.

*Definition of IPC Assembly Classes

- **Class 1- General Electronic Products**
  Includes consumer products, some computer and computer peripherals suitable for applications where cosmetic imperfections are not important and the major requirement is function of the complete electronic assembly.

- **Class 2- Dedicated Service Electronic Products**
  Includes communications equipment, sophisticated business machines and instruments where high performance and extended life is required and for which uninterrupted service is desired but not critical. Certain cosmetic imperfections are allowed.

- **Class 3- High Performance Electronic Products**
  Includes the equipment where continued performance or performance-on-demand is critical. Equipment downtime cannot be tolerated and must function when required, such as in life support devices or flight control systems. Assemblies in this class are suitable for applications where high levels of assurance are required, service is essential, or the end-use environment may be uncommonly harsh.

*From IPC-A-610D, March 2005

iNEMI Project Schedule Overview

Project Planning

2/02

Phase I Development

5/02

Phase II Development

2/03

Phase III TQ Build

10/03

Phase III TQ Rework

Reliability Tests & Failure Anal.

12/03

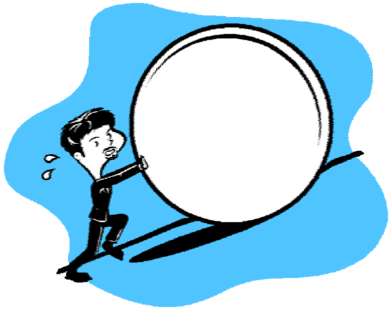
Draft Report

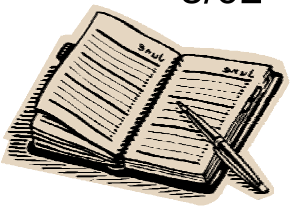
2/04

Final Report

11/04

5/05





The four phases of a real project:

Euphoria!	Sweat!	Panic!	Success!

Assembly Team Strategy

(1) Focus on SMT IPC Class 2 assemblies.

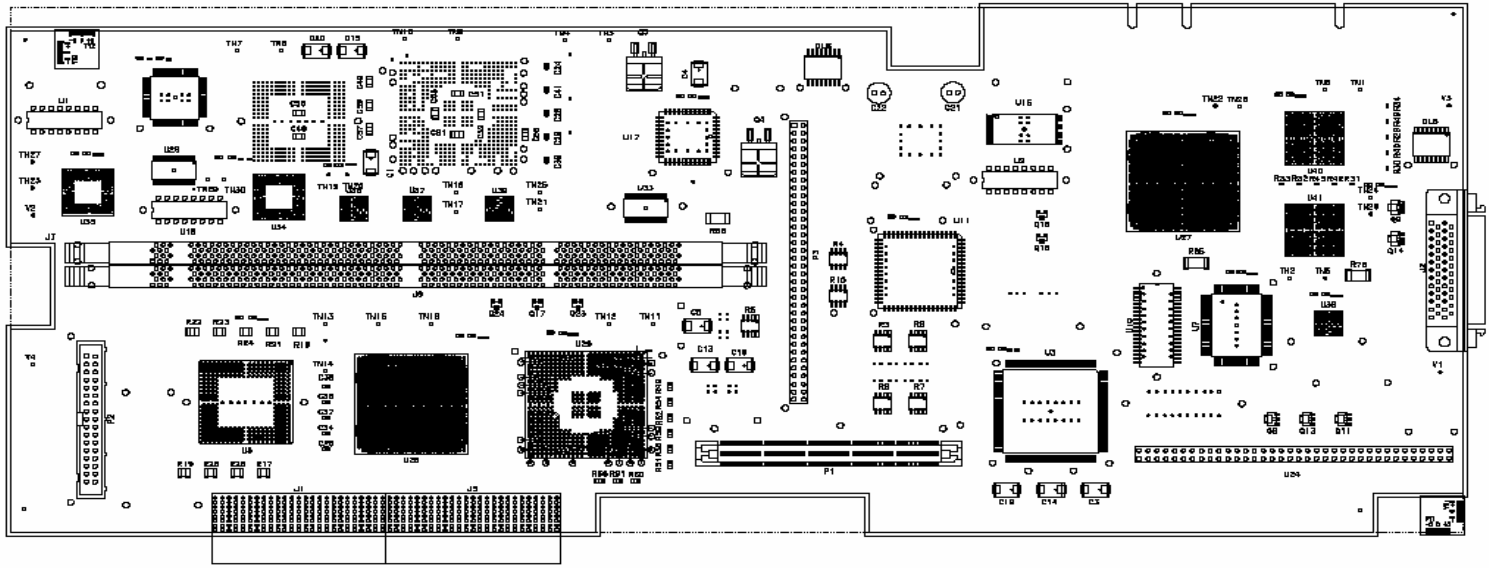
(2) Utilize existing equipment & process flows.

(3) Study, develop, improve, and implement new Pb-free processes (printing, placement, reflow).

(4) Assess PCB laminate survivability throughout entire process.

(5) Begin PTH development studies (> 100mil thick boards).

Design Considerations



PCB:

Class: IPC Class 2
Tg / Td: 170°C / 327°C

Dimensions: 17” x 7.3”
Board thickness: 0.093” and 0.135”

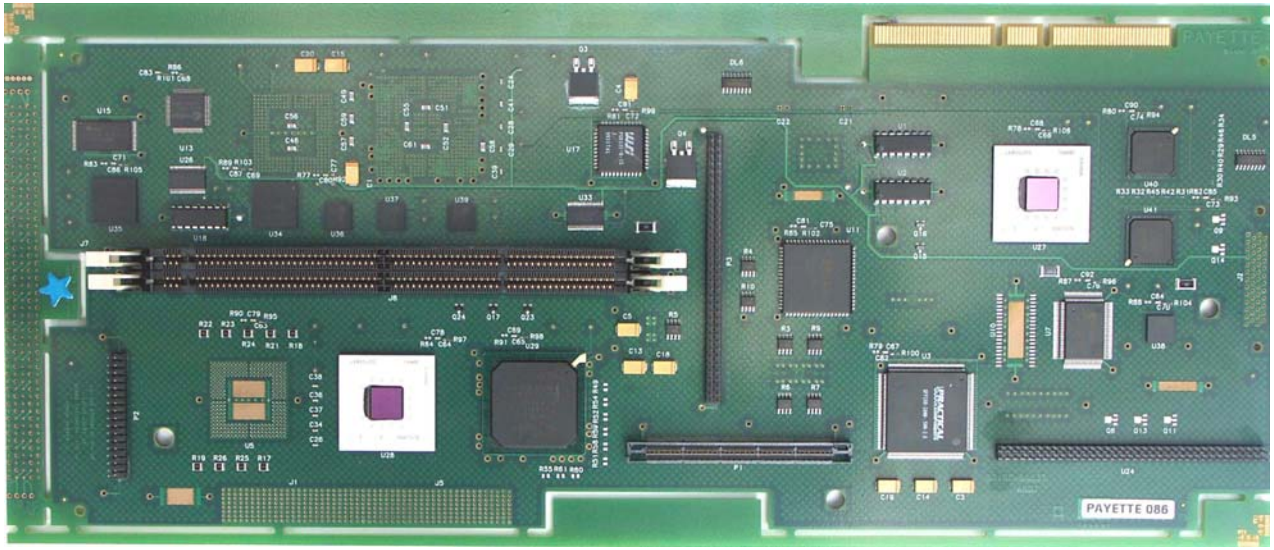
Surface Finish: Electrolytic NiAu and ImmAg
Solder Alloy: iNEMI recommended Sn3.9Ag0.6Cu (no-clean)

COMPONENT TYPES:

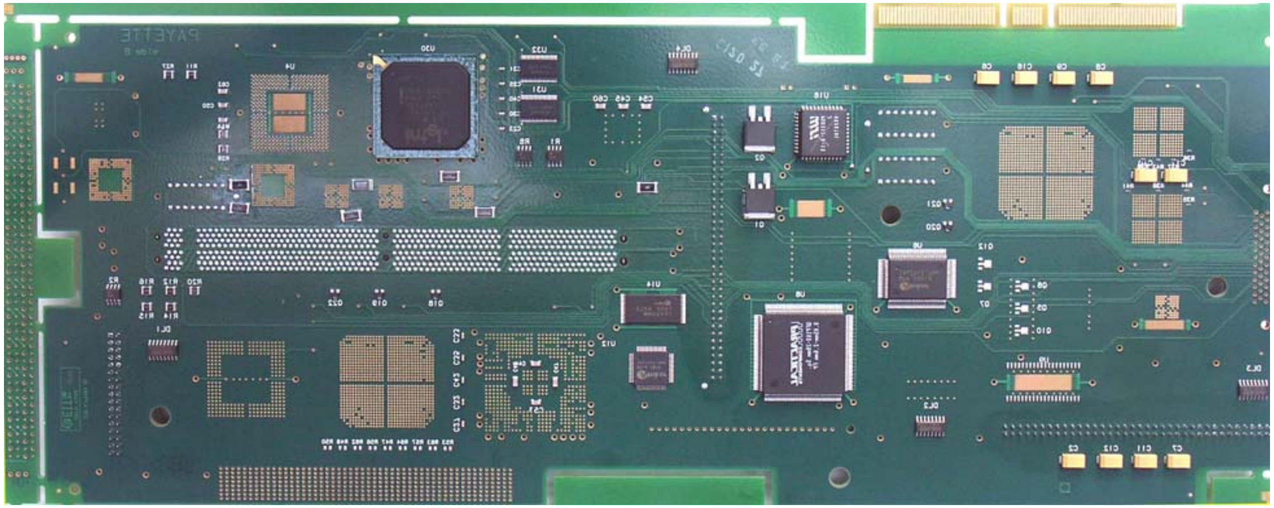
- CBGA, PBGA, CSP, QFP, TQFP, PLCC, TSOP, SOIC, 0603, 0402
- 15 different component families populated

IPC Class 2 “Payette” Test Vehicle

Side A (top)
14 Cu layers, 0.093” and 0.135” thick, Electrolytic Au and Imm Ag



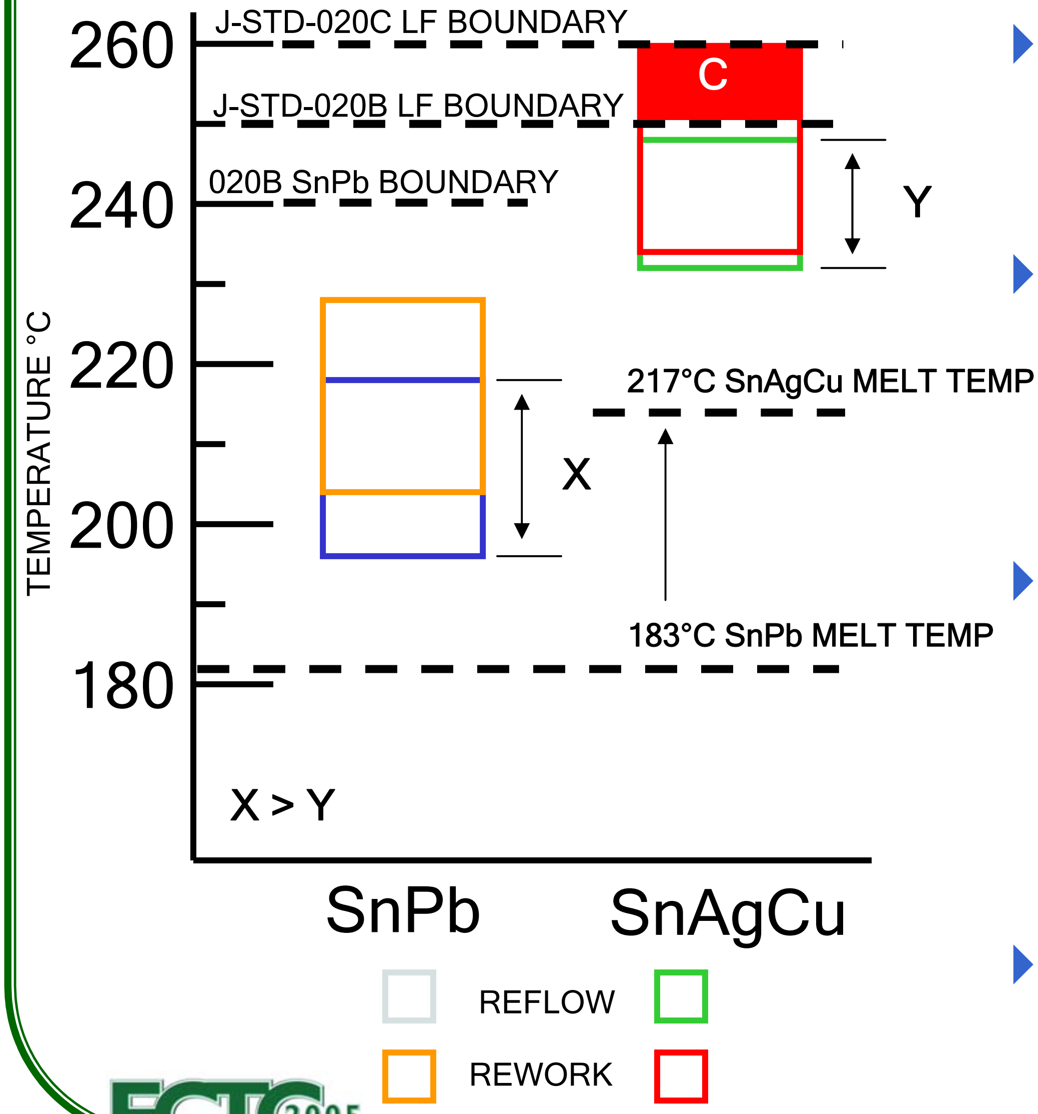
Side B (bottom)
(SMT + Wave)



7.3”

17”

Temperature Process windows have shrunk !



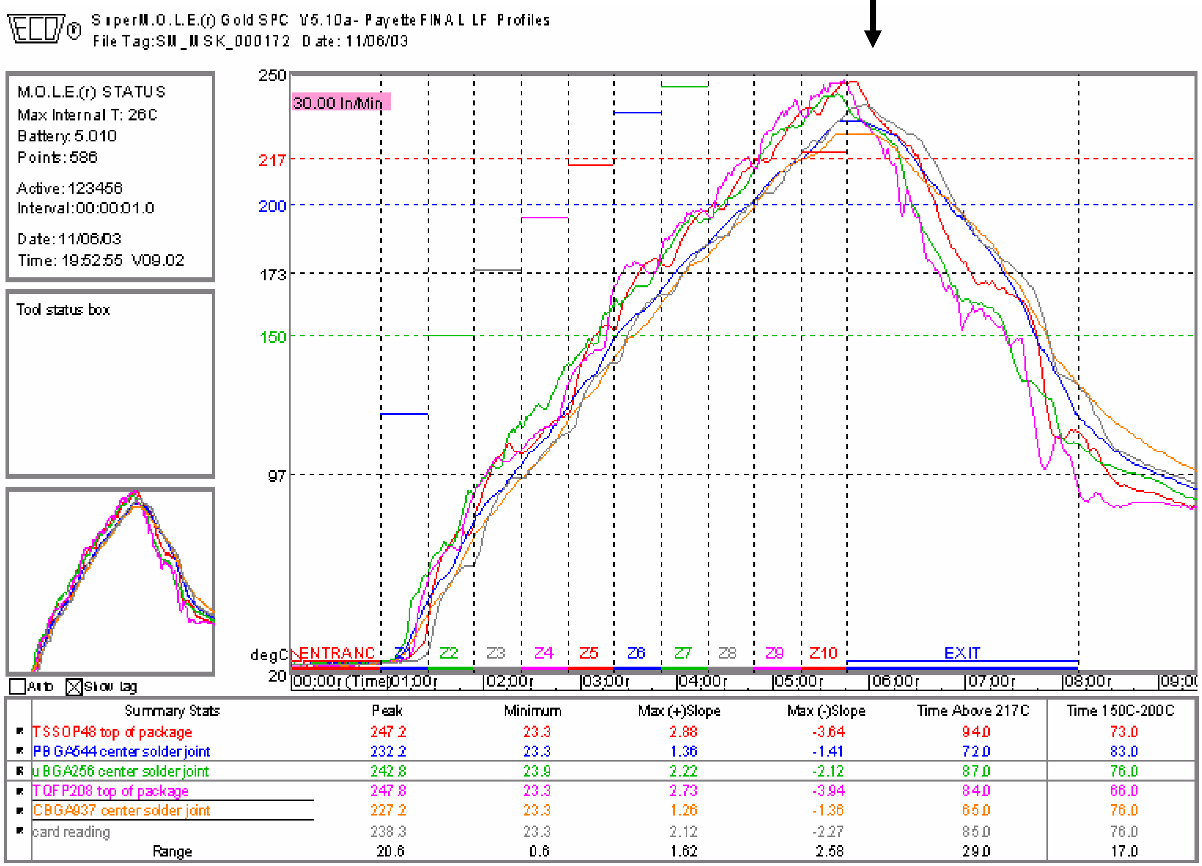
- 34° increase in T_{melt} from SnPb to Pb-free.
- Process windows are tighter due to component survivability specifications.
- Tighter process control is mandatory to ensure that component specs are not violated. J-STD-020C.
- Internal delamination, MSL and floor life affected.

0.135” thick (14 Layer) Reflow Profile

- 4 to 6 minute cycle times.
- Solder joint temp 230 - 250°C.
- ΔT ranges from 5 - 20°C (bodies & joints).
- TAL range 60 - 90 seconds.
- Linear ramp to reflow acceptable.

Need margin within MFG process:

248°C Max Peak (very tight)



SuperM.O.L.E.(r) Gold SPC V5.10a- Payette FINAL LF Profiles
File Tag:SM_MSK_000172 Date: 11/06/03

M.O.L.E.(r) STATUS
Max Internal T: 26C
Battery: 5.010
Points: 586

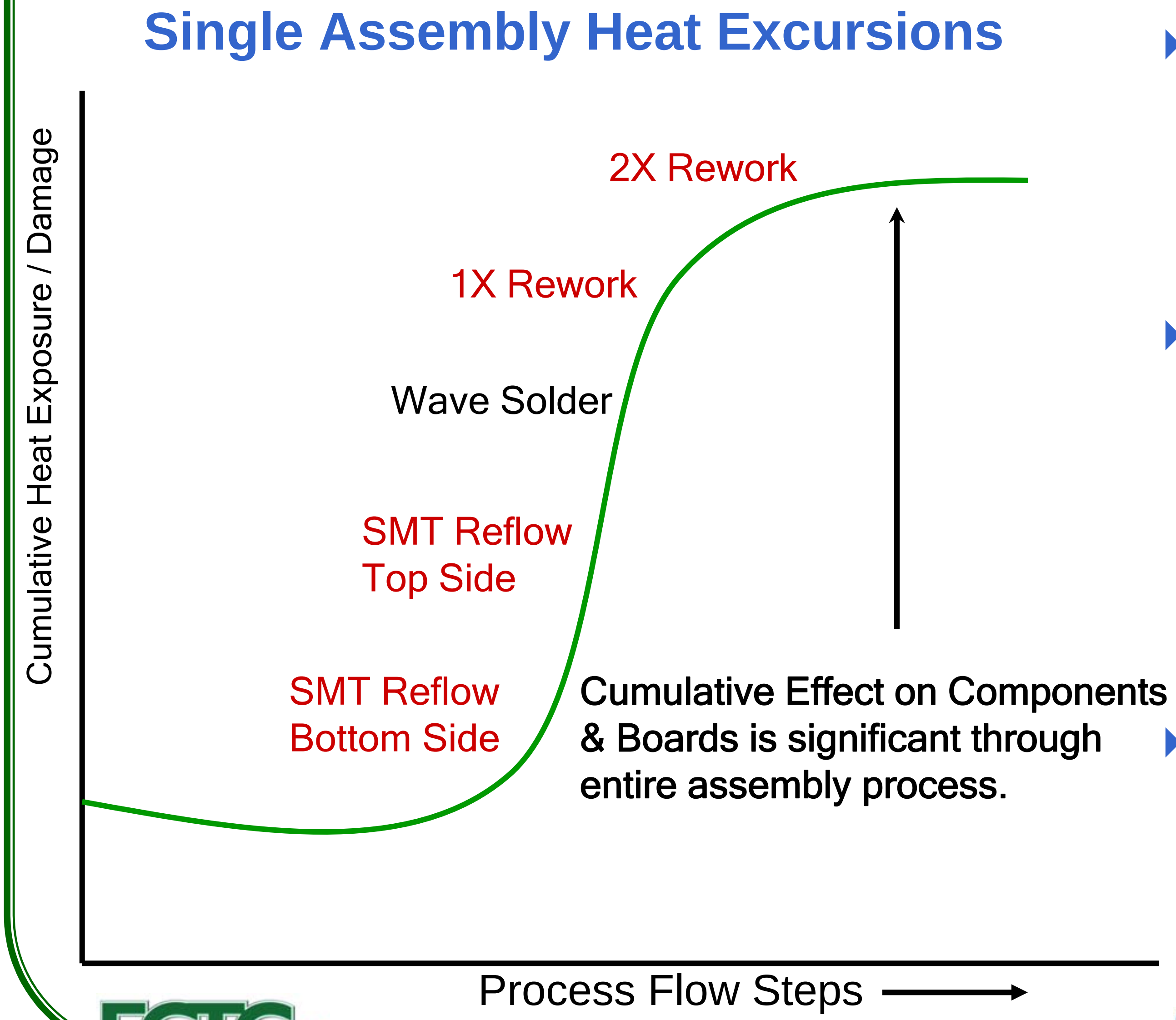
Active: 123456
Interval: 00:00:01.0

Date: 11/06/03
Time: 19:52:55 V09.02

Summary Stats	Peak	Minimum	Max (+)Slope	Max (-)Slope	Time Above 217C	Time 150C-200C
TSSOP48 top of package	247.2	23.3	2.88	-3.64	94.0	73.0
PBGA544 center solder joint	232.2	23.3	1.36	-1.41	72.0	83.0
uBGA256 center solder joint	242.8	23.9	2.22	-2.12	87.0	76.0
TQFP208 top of package	247.8	23.3	2.73	-3.94	84.0	66.0
CBGA937 center solder joint	227.2	23.3	1.26	-1.36	65.0	76.0
card reading	238.3	23.3	2.12	-2.27	85.0	76.0
Range	20.6	0.6	1.62	2.58	29.0	17.0

All assemblies run in air atmosphere.

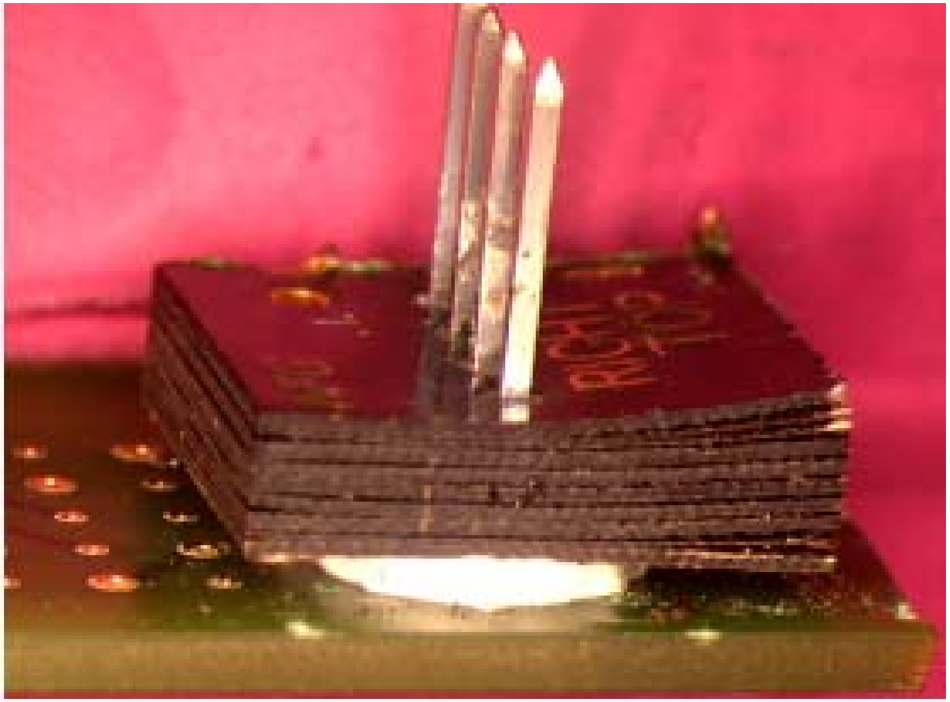
Cumulative Board Damage



Cumulative Effect on Components & Boards is significant through entire assembly process.

- **1 assembly can be exposed to as many as 5 thermal heat excursions.**
- **Component issues include increased MSL sensitivity, shorter floor life, and internal package failure.**
- **PCB issues include internal layer delamination, via cracking and board warpage.**

Laminate System Performance



SnPb Rated Laminate

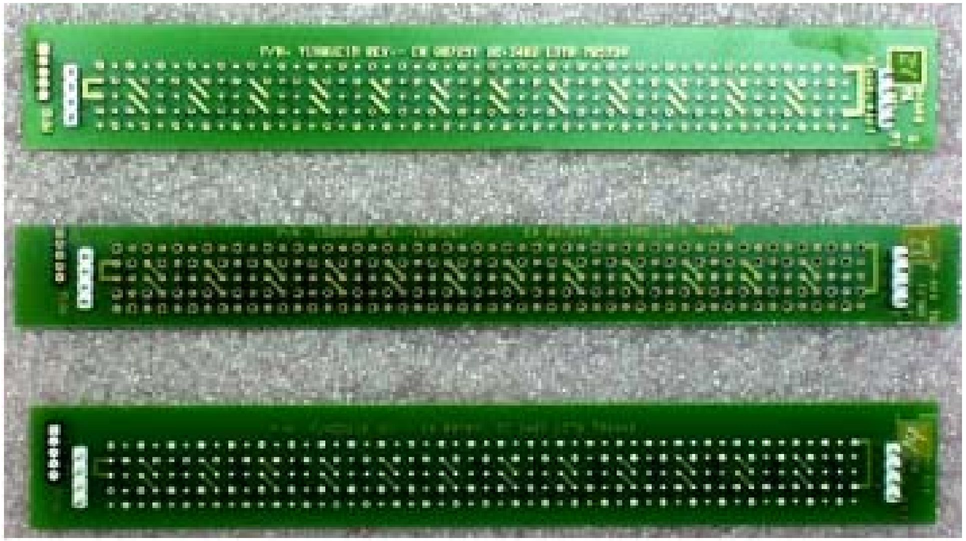
Pb-free Tested Laminate

- Top and bottom laminate run through exact same LF profile at same time.
- iNEMI team used a Pb-free tested laminate with success.
- Combination of Pb-free reflow pre-conditioning method prior to IST / CITC used for evaluation.

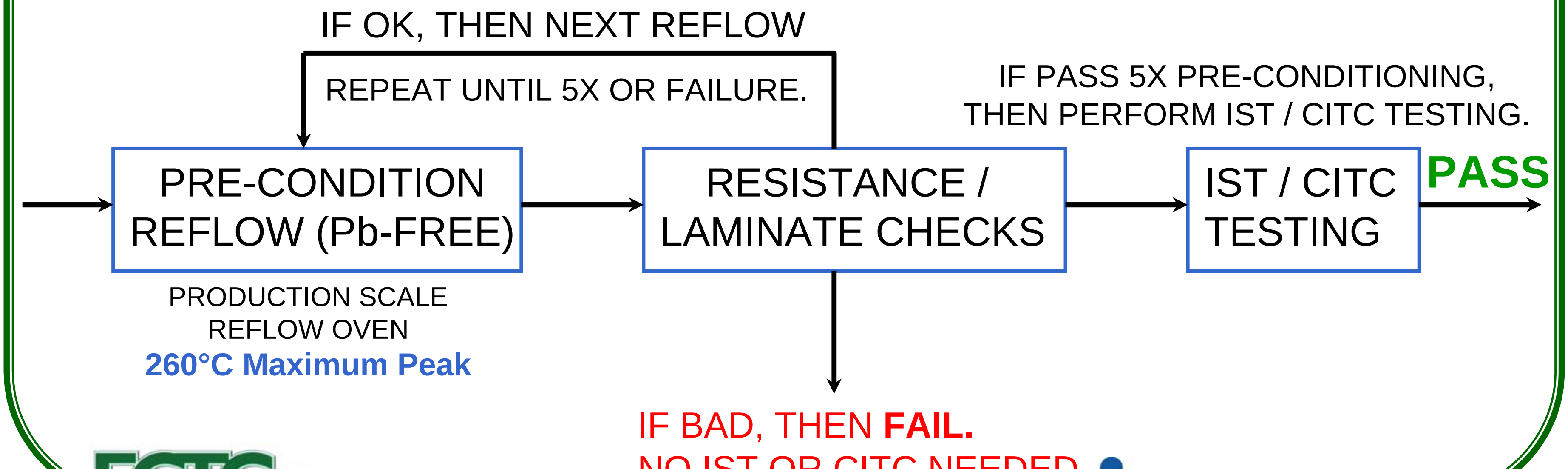
Board Pre-conditioning Method

Materials Required:

- IST / CITC Coupon Designs
- 10-zone convection reflow oven
- Multi-meter
- IST / CITC Testers



General Method:



IF OK, THEN NEXT REFLOW

REPEAT UNTIL 5X OR FAILURE.

IF PASS 5X PRE-CONDITIONING,
THEN PERFORM IST / CITC TESTING.

PRE-CONDITION
REFLOW (Pb-FREE)

RESISTANCE /
LAMINATE CHECKS

IST / CITC
TESTING

PASS

PRODUCTION SCALE
REFLOW OVEN
260°C Maximum Peak

IF BAD, THEN **FAIL.**
NO IST OR CITC NEEDED.

IPC Class 2 Assembly Findings

1. IPC Class 2 Pb-free SMT reflow processing windows will shrink. (Windows identified)

2. Multiple heat cycles cause significant component and laminate stress. Stress management is essential.

3. Reflow in air was shown to produce properly formed joints.

4. The use of N_2 was shown to promote wetting, and create shinier looking joints.(Improved aesthetics).

5. Coldest Solder joint on ANY Pb-free assembly should be no less than 230°C.

Rework Team Strategy

(1) Develop Pb-free rework processes for area array packages including uBGAs, PBGAs, and CBGAs for IPC Class 2 assemblies.

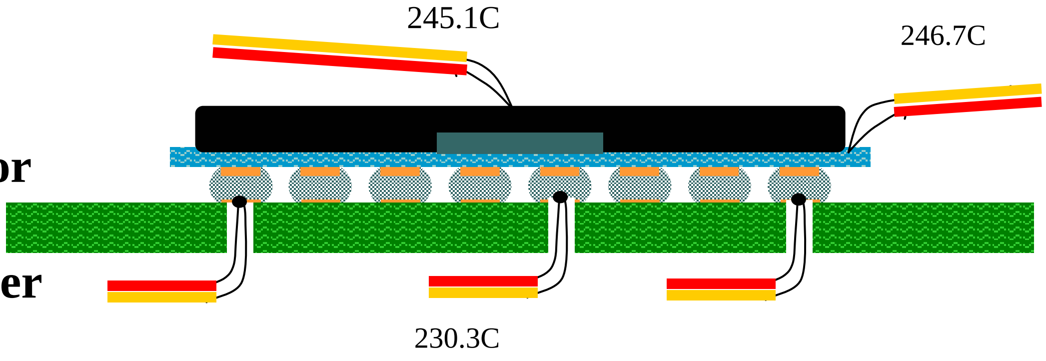
(2) Investigate the feasibility of Pb-free pin-through-hole (PTH) DIP component attachment rework process on IPC Class 2 boards.

Rework Profile Considerations

- Challenge
  - **Minimize top package temperature while allowing sufficient heat to form a solder connection**
- Lead-free Rework Observations
  - **Tighter process due to package temperature limitation**
  - **At a minimum, 230°C for solder joint temperature for rework**
  - **Approximately ~35% longer profiles for lead-free compared with SnPb**

Phase 3 Rework Profiling Target Parameters

Process	Min. Joint Temp (C)	Time Above Liquidus (sec)	Max Body Temp (C)
SnPb	200 - 205	45 - 90	220 - 240
LF SnAgCu	230 - 235	45 - 90	245 - 260



Actual Monitored Rework Reflow Values

Rework Profile Comparison

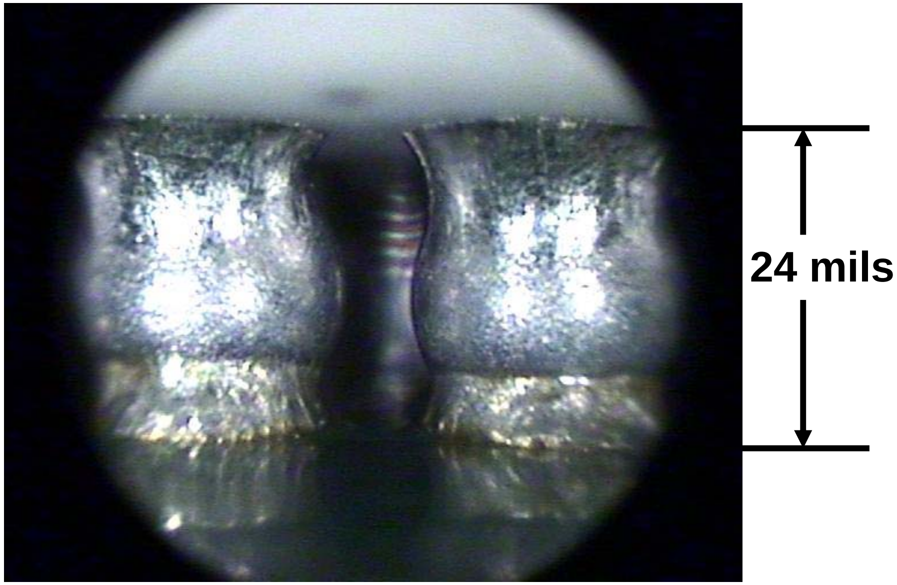
- **Minimum Lead-free solder joint temperature (230°C)**
- **Package temperature was close to the limit of maximum body temperature allowed**
- **Extended profiles for Lead-free (Avg: ~35% longer)**

135 mil Thick Profile Parameters

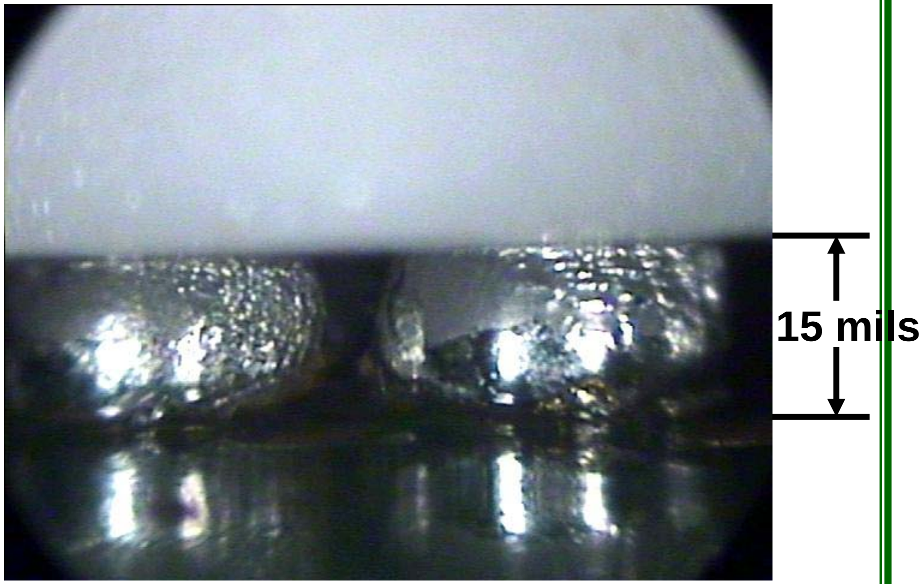
Package	SnPb			SAC		
	Min. Joint Temp (C)	Package Temp (C)	Time to Peak (sec)	Min. Joint Temp (C)	Package Temp (C)	Time to Peak (sec)
CBGA	201	202	580	235	238	675
uBGA	199	210	300	229	245	450
PBGA	200	220	450	230.3	247	650

Visual Inspection after CBGA-937 rework

Standoff height of dual melt and single melt balls is very different!



SnPb Rework



Lead-free SnAgCu Rework

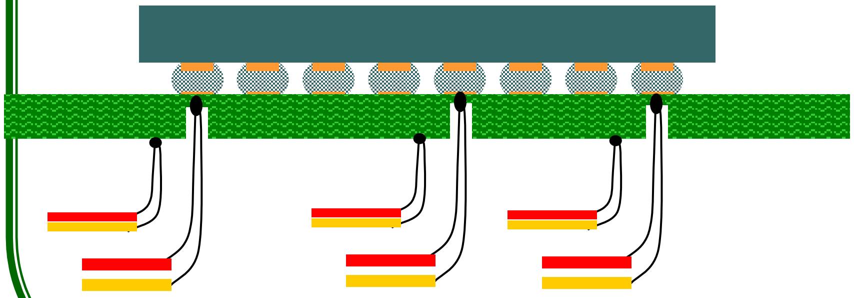
CBGA-uBGA Interaction Study

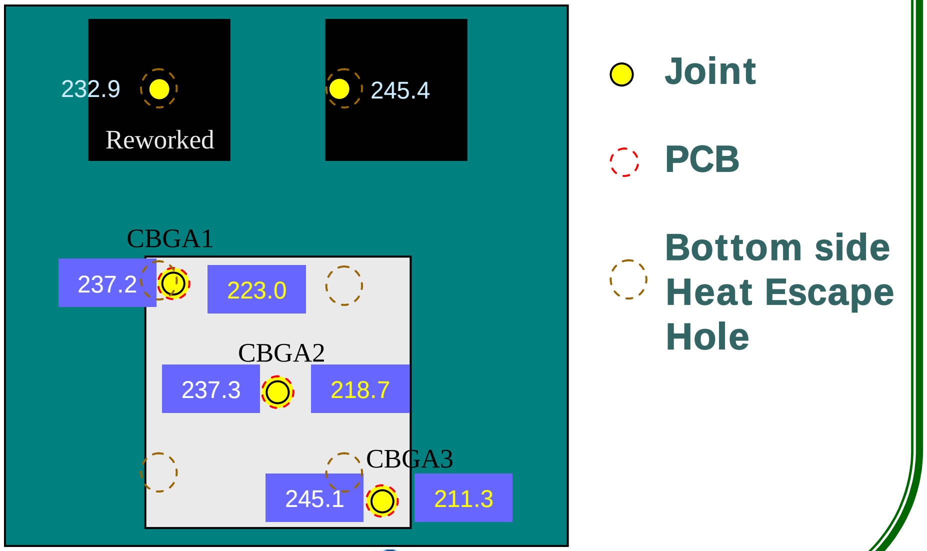
Observations:

- Adjacent CBGA had liquidus temperatures (0.65” away)
- Thermal gradient across the CBGA package (see table)

Joint and Package Temp Monitored Values

TC Location	Peak Temp (C)
Reworked uBGA Joint	232.9
Adjacent uBGA Joint	245.5
CBGA 1 Joint	223.0
CBGA 1 Bottom PCB	237.2
CBGA 2 Joint	218.7
CBGA 2 Bottom PCB	237.3
CBGA 3 Joint	211.3
CBGA 3 Bottom PCB	245.1



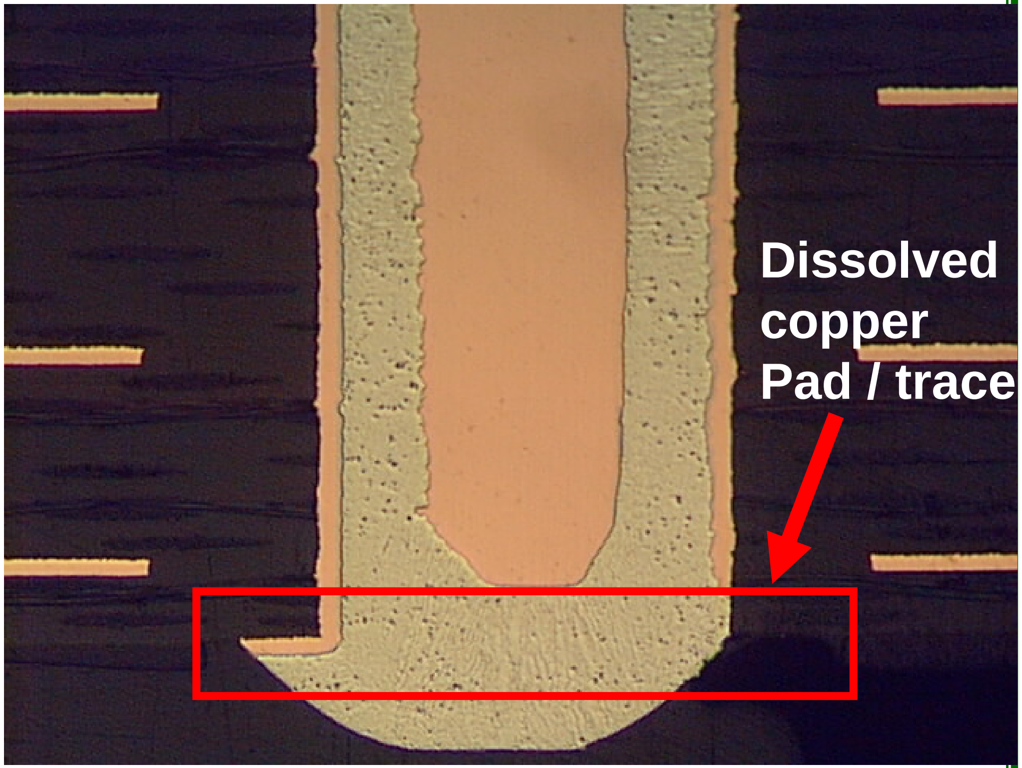


BGA Rework Best Practices

- Higher bottom heaters set point (~50°C or higher)
- Rework reflow profile consideration:
  - Peak temperature: 230°C (min. for joints) to 255°C (max for body) temperature
  - Time above liquidus: 45 to 90 seconds, and potentially up to 120 seconds
  - Linear ramp to peak temperature to help minimize delta T across component body
- Thermocouple attachment
  - At least 2 solder joint temperatures and 2 package body temperatures (center and corner for both)

Mini-Pot Results showing Copper Dissolution (SnAgCu, 135 mil thick, NiAu)

- Challenge
  - **Simulate current production process**
  - **Remove and replace a PDIP without board preheat**
- Rework Observations
  - **Achieving sufficient holefill resulted in the copper pad/trace dissolution on the bottom-side**
  - **Potential of having copper content at an undesirable level in the minipot**



Cross-section View of Solder Joint (274C)

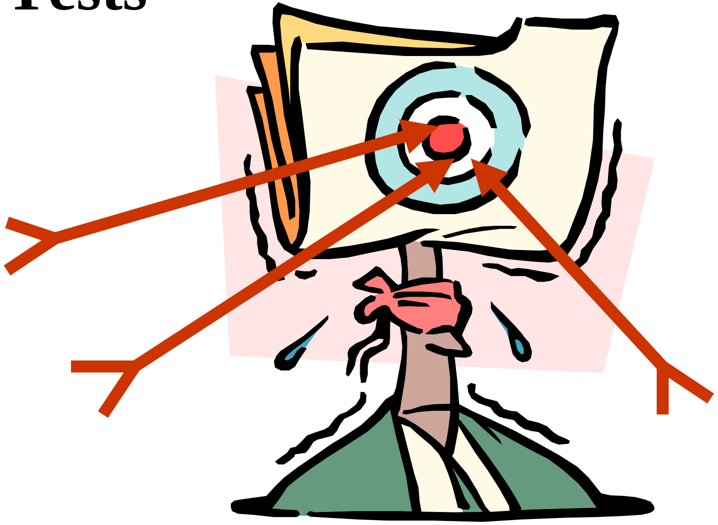
Summary of Key Rework Challenges

- **Lead-free PTH Rework**
  - Without board preheat, achieving "good / sufficient" holefill resulted in copper pad erosion
  - Maintaining a desirable copper level in the minipot

- **Lead-free BGA Rework**
  - Difficult to minimize top package temperature while allowing sufficient minimum peak solder joint temperatures
  - Adjacent and bottom side components undergo secondary reflow
  - Equipment not yet optimized for Lead-Free rework

Process Robustness Tests

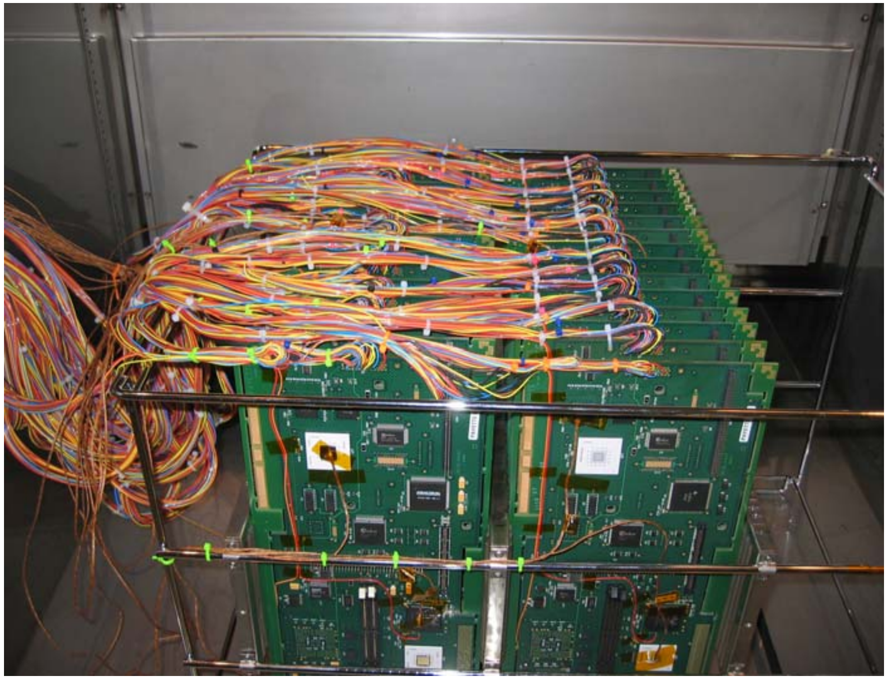
- **Accelerated Thermal Cycling Tests**
  - Experimental setup
  - CBGA results
  - Micro BGA results



- **Impacts of rework**
  - Thermal fatigue life
  - Yield
  - Secondary reflow of adjacent components
  - Other impacts
- **Bend Test**
  - Experimental setup
  - Results

ATC Testing of 56 As-assembled and Reworked Payette Test Boards

Exterior View

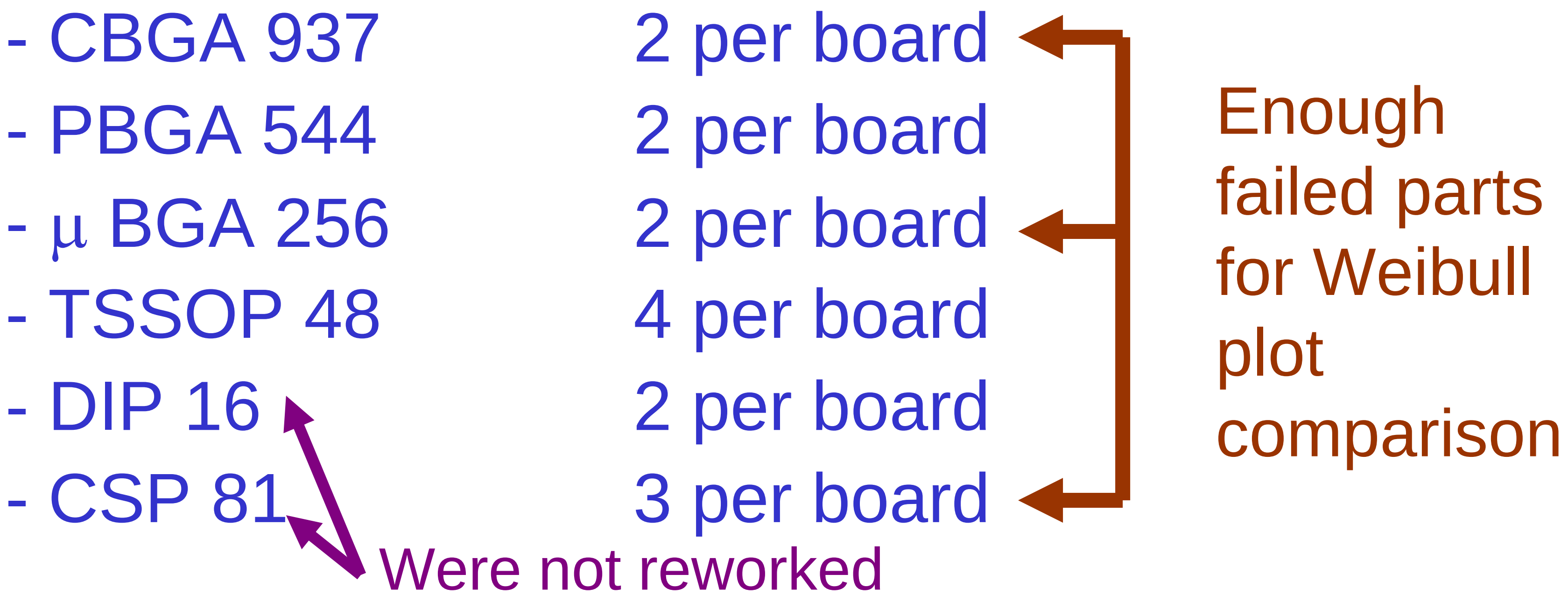


Interior View

0 to 100 ^{o}C ATC (with 10 minute Dwells) Test Chambers with continuous insitu daisy chain resistance monitoring of major component classes for > 5700 cycles (~ 6 months)

Components monitored in ATC

Variety of package / solder joint classes (area array, leaded, through-hole, etc.)-



- CBGA 937	2 per board
- PBGA 544	2 per board
- μ BGA 256	2 per board
- TSSOP 48	4 per board
- DIP 16	2 per board
- CSP 81	3 per board

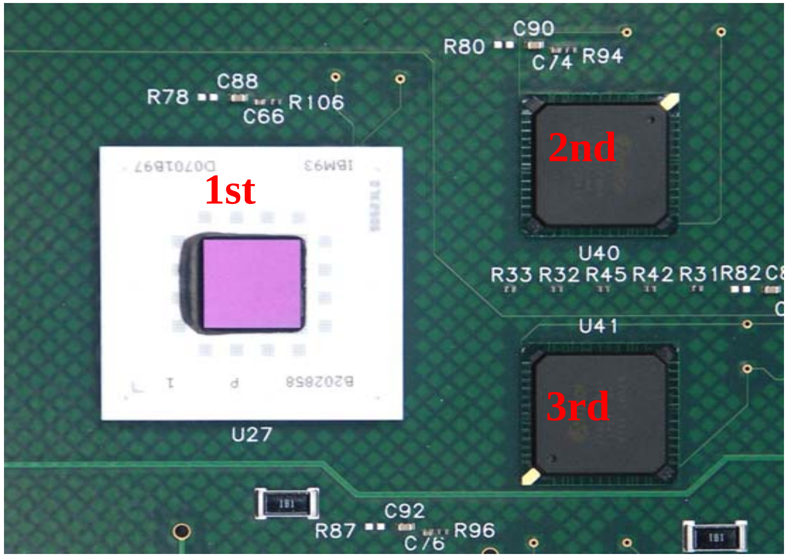
Enough failed parts for Weibull plot comparison

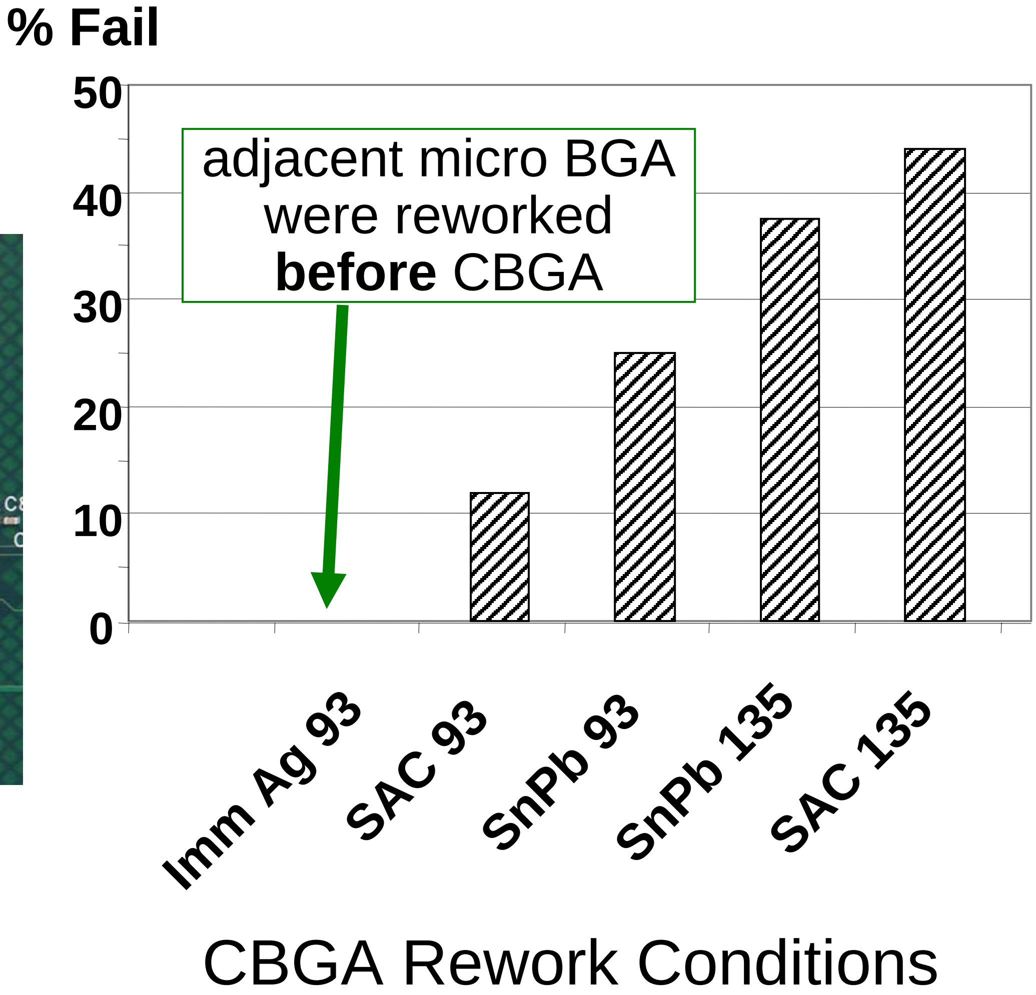
Were not reworked

TOTAL	840 components monitored

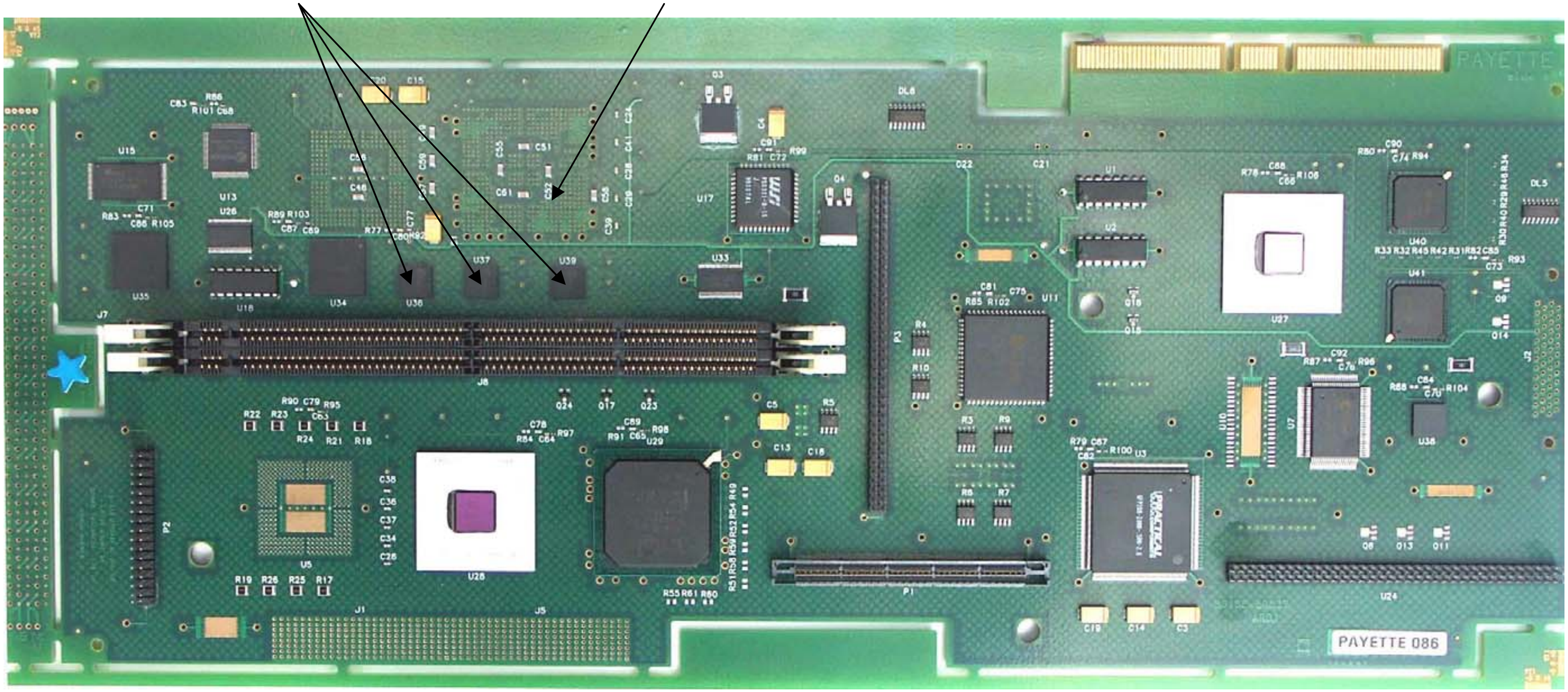
- ➢ **Pb-free solder joints had <u>longer</u> accelerated thermal fatigue life than SnPb solder joints.**

Rework Impact on the Yield of CBGAs

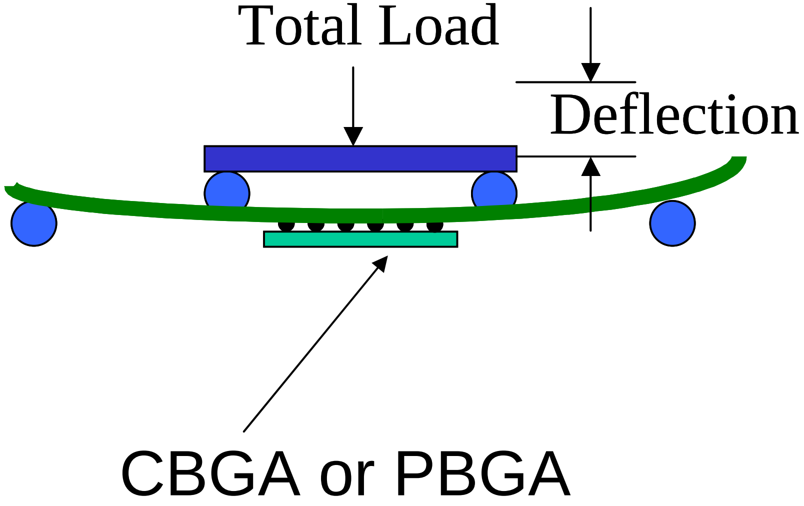


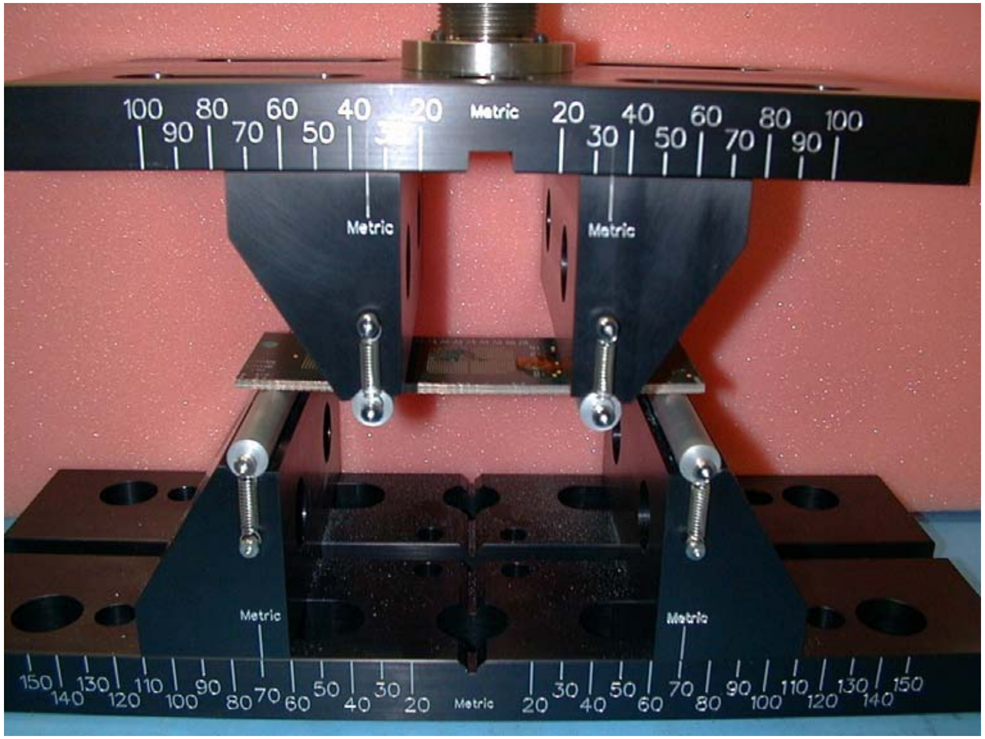

adjacent micro BGA were reworked **before** CBGA

Impact PBGA Rework on CSP 81



Board Bend Tests

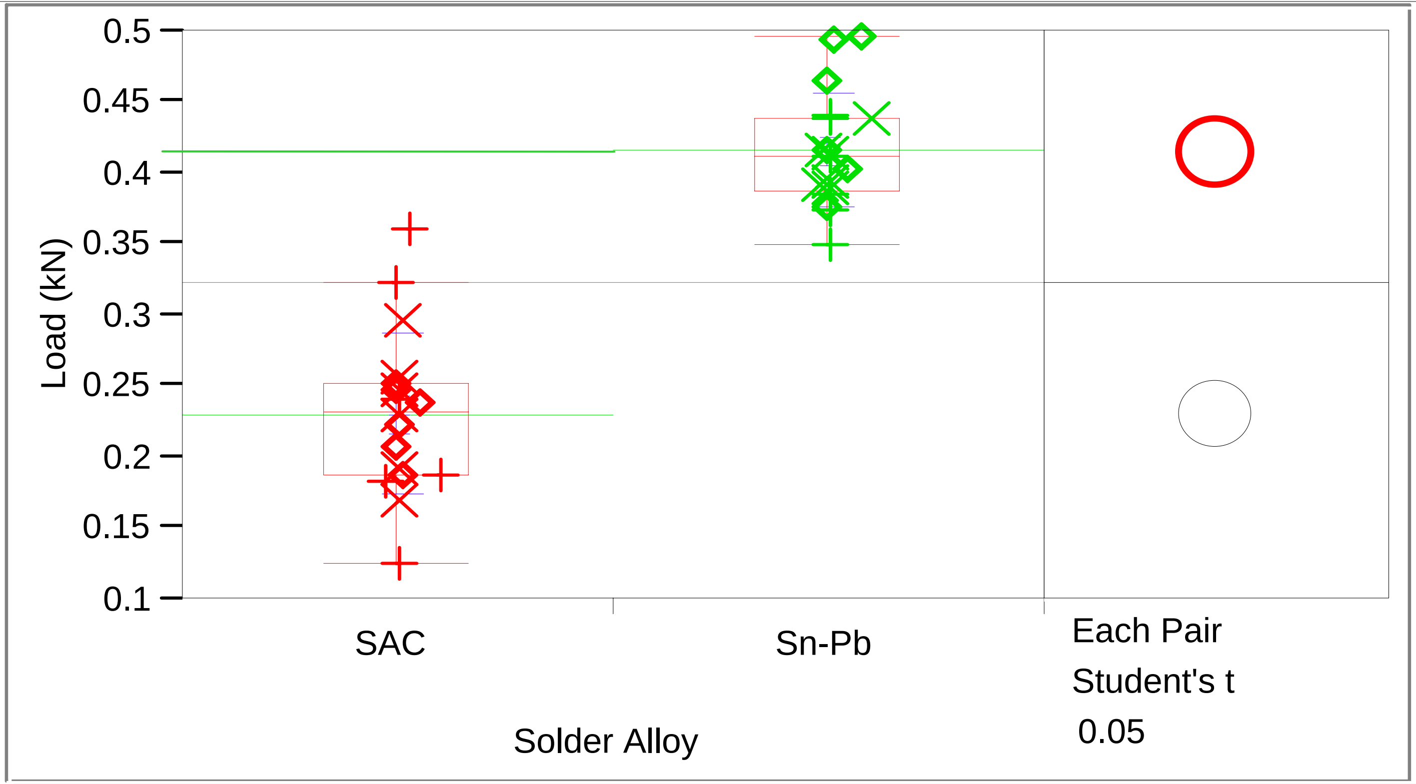




Four-point Bend Test Setup

SAC parts are more sensitive than SnPb

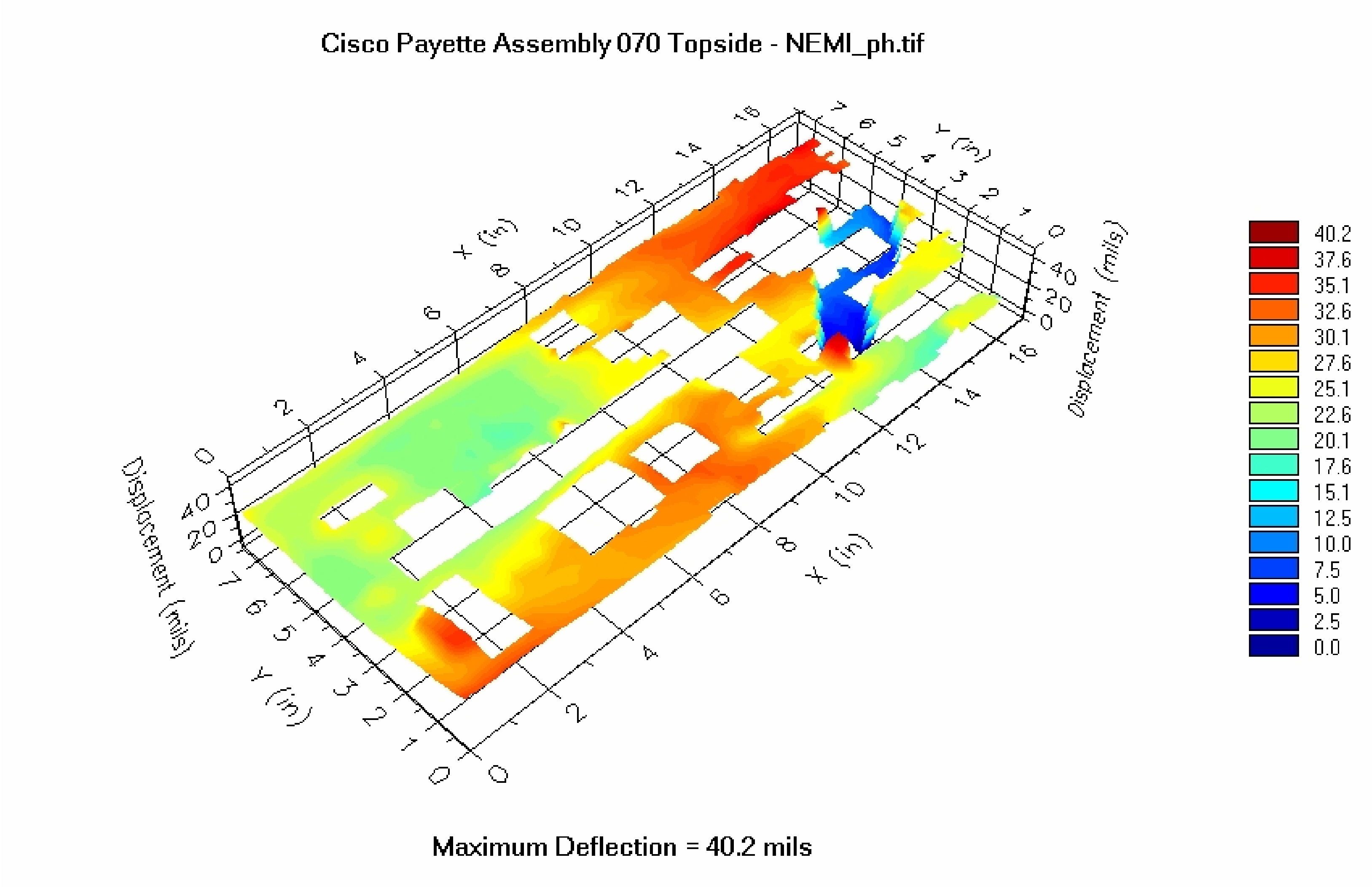
Oneway Analysis of Load (kN) By Solder Alloy



Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
SAC	18	0.230859	0.056591	0.01334	0.20272	0.25900
Sn-Pb	18	0.416101	0.040408	0.00952	0.39601	0.43620

Shadow Moiré on As-received Payette



Reliability Test Conclusions

- **ATC**
  - Pb-free solder joints parts had longer accelerated thermal fatigue life than the Sn-Pb parts
- **Impact of rework**
  - Observed secondary reflow of adjacent component solder joints
  - Voiding and solder mask adhesion degradation were observed on the micro BGA solder joints
- **Bend Tests**
  - SAC joint structures failed at lower bend loads than SnPb

Top 10 Key Conclusions

1. **Double-sided IPC Class 2 Leadfree Assembly and Rework Process Evaluated via Metallurgical / Reliability Analysis**
   - **93 and 135 mil thick PCB**
   - **Electrolytic NiAu and Imm Ag Surface Finishes**
   - **SMT / BGA Leads**
   - **Organic and Ceramic Components**

2. **Current As-Assembled SMT Toolset Acceptable for Leadfree Manufacturing Processes**
   - **10 Zone convection reflow ovens recommended**
3. **TOP / BOTTOM-SIDE Rework Reflow Concerns**
   - **Boards Greater-Than 93 mil Thick**
   - **Reflow of Non-Targeted Solder Joints (Collateral Damage)**
   - **Decrease in Reliability Life Observed**

Top 10 Key Conclusions (continued)

4. Rework Toolset Improvements Identified

- Minimize Collateral Damage to Adjacent Component Solder Joints
- Heat shields / Shrouds / Nozzles-Focus Thermal Energy
- Uniform Board Temperature Control Critical
- Improvements in Bottom Heating, Board Bias
- Need Additional Tolerance / Repeatability Studies
- Minimize dissolution of Cu on TH pads and vias

5. PCB Material Selection Critical

- Both laminates and laminate fabricator important
- Laminate Survivability Requires Testing
  - Repeated Exposures to SAC Process Temps
- Evaluated Board Performance
  - Interconnect Stress Test (IST)
  - Current Induced Temperature Cycling (CITC)

6. SAC Joint Temperatures

- 230 °C Minimum on “coolest joint” for Manufacturability

Top 10 Key Conclusions (continued)

7. SAC Component Temperatures Observed

- **230 °C – 260 °C**
- **J-STD-020C Needed for SAC Board Processing**

8. SAC Accelerated Thermal Cycle Fatigue Better SnPb

- **As-Assembled Builds**
- **Rework Builds**

9. SAC Boards Have More Mechanical Bend Sensitivity

10. No Reliability Impact

- **Electrolytic NiAu and Imm Ag**

Summary

- ☐ **As-Assembled SAC Process Capable**
- ☐ **Rework SAC Process Defined**
  - **Initiating iNEMI Project for SAC Rework Optimization**
  - **Have initiated iNEMI Wave Solder PIH Project**
  - **Have initiated iNEMI Surface Finished Project**
  - **Initiating iNEMI Mixed Soldering Project**
- ☐ **Project Report Available on CD to iNEMI Members in June 2005**

For more information: Contact iNEMI: at www.iNEMI.org

Acknowledgements- Key Contributors

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