Use of Nanotechnology for Electronics Packaging Applications – European View

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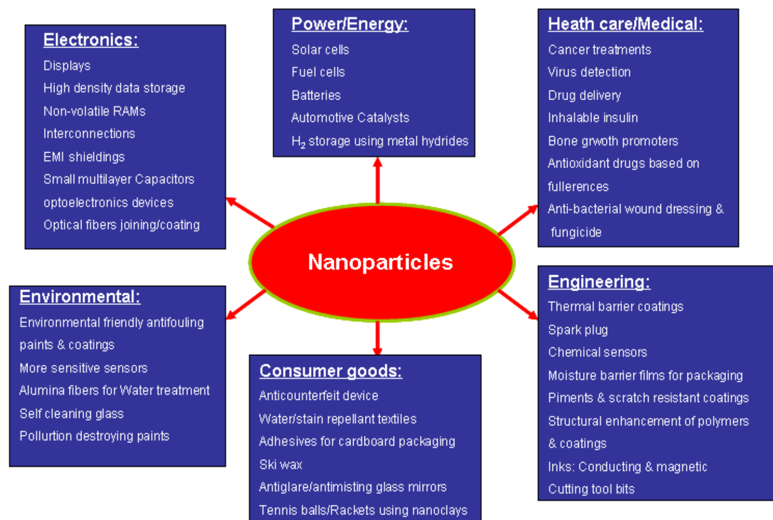
- European Platform in Nanoelectronics (Eniac)
- Funded EU Programs in 7th Frame Program in ICT fields with focus on Nanoelectronics
- Some examples of nanomaterials and process development – Nano-Thermal Interface Material, Nanocooler, Nano Interconnect, Nano solder paste
- Reliability models development
- Encapsulaton of OLED devices with Nano-ACA

Definition of Nano Particles

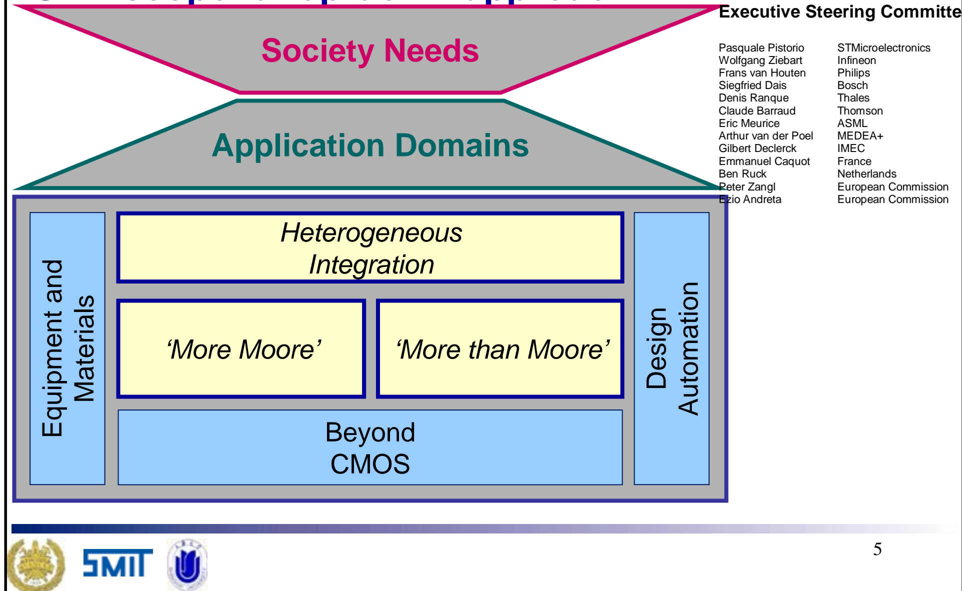
Particles in size range 10^{-9}m are knwon as nanoparticles or sub-micron particles. They are also known as quantum dots due to quantum property possessed by them.

Nanoparticles in Various Fields

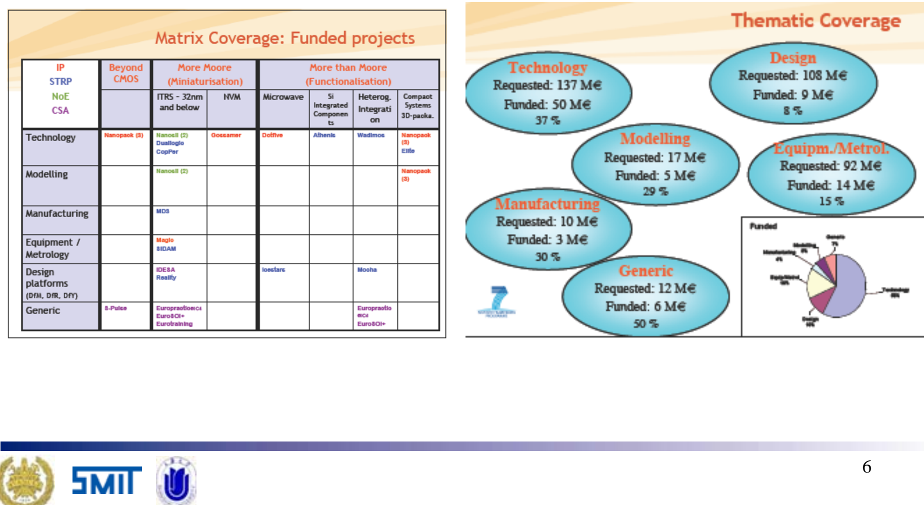


European Network for Nanoelectronics (ENIAC)

SRA scope: a top-down approach



IST-2007.3.1: Next-Generation Nanoelectronics: Components and Electronics Integration - Fundin results (Ref: Vergera, EU)



Matrix Coverage: Funded projects

IP / STRP / NoE / CSA	Beyond CMOS	More Moore (Miniaturisation)		More than Moore (Functionalisation)			
		ITRS - 32nm and below	NVM	Microwave	Si Integrated Components	Heterog. Integration	Compact Systems 3D-packa.
Technology	Nanopack (3)	Nanosil (2) Duallogic CopPer	Gossamer	Dotfive	Athenis	Wadimos	Nanopack (3) Elite
Modelling		Nanosil (2)					Nanopack (3)
Manufacturing		MD3					
Equipment / Metrology		Magic SIDAM					
Design platforms (DfM, DfR, DfY)		IDESA Reality		Icestars		Mocha	
Generic	S-Pulse	EuropracticeIC4 EuroSOI+ Eurotraining				Europractice IC4 EuroSOI+	

IST-2007.3.1: Next-Generation Nanoelectronics: Components and Electronics Integration; EU IP Project

Large-scale integrating project (IP) proposal

ICT Call 1

FP7-ICT-2007-1

Proposal No: 216176

Total budget 12 MEURO

Nano Packaging Technology for Interconnect and Heat Dissipation

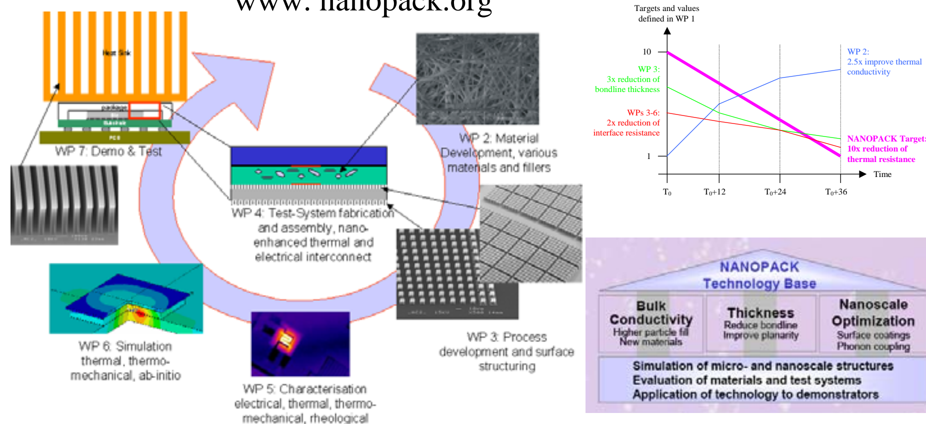
NANOPACK

Participant no. *	Participant organisationame	Part. short name	Country
1 (Coordinator)	Thales Research & Technology	TRT	France
2	Budapest University of Technology and Economics	BME	Hungary
3	Robert Bosch GmbH	Bosch	Germany
4	Institut d'Electronique de Microtechnologie et de Nanotechnologie (CNRS in A2 form)	IEMN	France
5	Chalmers University of Technology	CHALMERS	Sweden
6	Electrovac AG	EVAC	Austria
7	FOAB Elektronik AB	FOAB	Sweden
8	Fraunhofer Institute IZM	F-IZM	Germany
9	IBM Zürich Research Laboratory	IBM	Switzerland
10	Catalan Institute of Nanotechnology	ICN	Spain
11	MicReD Ltd.	MicReD	Hungary
12	Berliner Nanotest und Design GmbH	Nanotest	Germany
13	Thales Avionics	THAV	France
14	VTT Micro- and Nano-electronics	VTT	Finland

Overall objective of the NANOPACK Program

Develop new thermal interface technologies for low thermal resistance by employing nano-modified surfaces and materials along with methods for characterization and simulation with respect to thermal, electrical and reliability-related properties.

www. nanopack.org



Nano-Pack Focus at SMIT Center, Chalmers University of Technology

Nano-Thermal interface material

package

Die

Substrate

PCB

CNT-based microchannel coolers

CNT-based high thermally conductive fine pitch interconnects

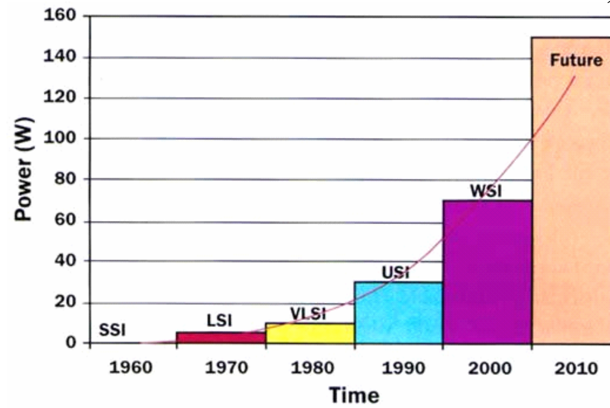
SMIT

Nano-Thermal Interface Material

SMIT

Heat development of CPU

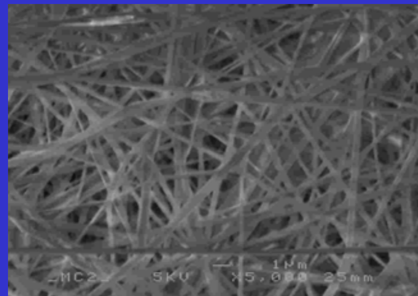
"If chip makers had continued on their old path, by the year 2015,microprocessors would be throwing off more watts per square millimeter than the surface of the sun." – *IEEE SPECTRUM, 1st Issue, 2006*



Timeline plot of device technology with respect to power dissipation

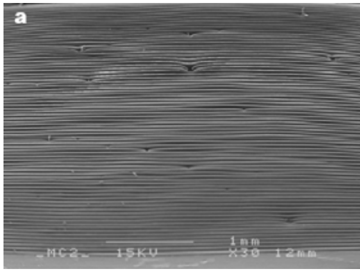
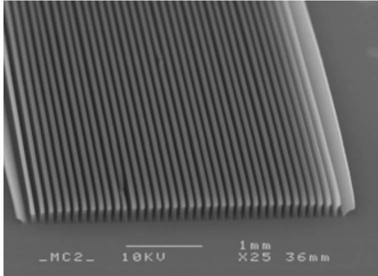
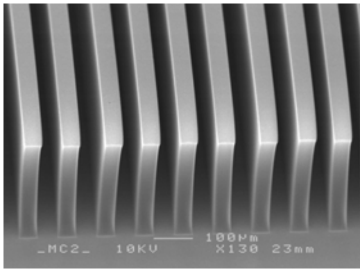
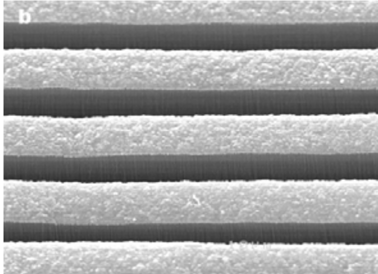
(source: http://www.electronics-cooling.com/html/2000_dec_a1.html)

Nano-TIM



Microcooler Based CNT

CNT-based microchannel coolers

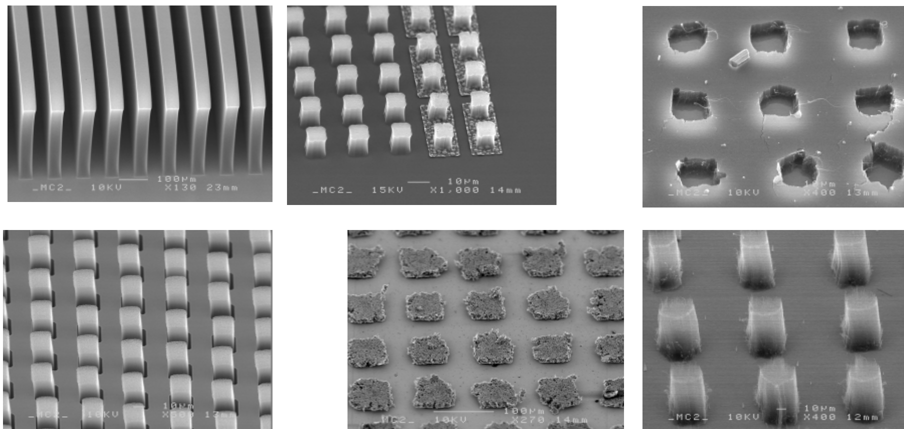
Results

50μm wide channels. Hights of the fins are 100μm and 300μm respectively. The surrounding temperature is 23°C.

Sample	1	2	3	4
Description	CNT cooler	Silicon cooler with fins	Silicon cooler without fins	Natural air convection
Power of resistor (W)	2.13	1.95	1.95	1.85
Flow rate (ml/min)	35.7	38.5	34.5	/
Temperature of resistor (°C)	42	42	50	56

Development and Characterization of Microcoolers using Carbon Nanotubes, Teng Wang, Martin Jönsson, Elisabeth Nyström, Zhimin Mo, Eleanor E.B. Campbell and Johan Liu, ESTC2006, September 5-7, 2006, Dresden, Germany, pp.881-885.

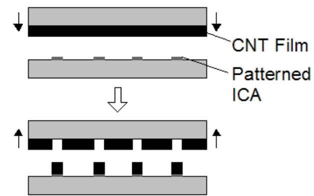
CNT based packaging research and development at SMIT Center



- Growth of CNTs with or without patterns on different substrates
- Low temperature transfer of CNTs by conductive adhesives
- Integration of these technologies into various structures

Transfer of CNT Bundles

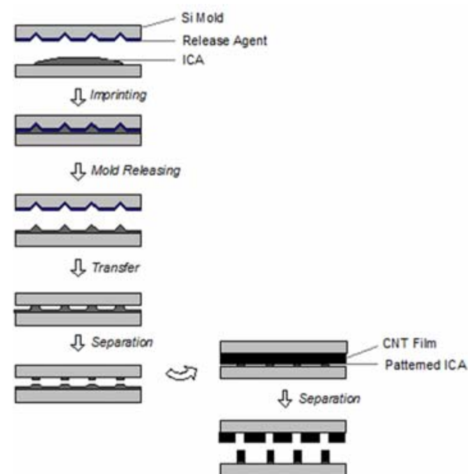
- Motivation
  - to integrate CNTs into temperature-sensitive processes and materials (CNT growth temperature normally higher than 700ºC)
  - to promote the adhesion between CNTs and the substrate



Technology used
  - Transfer of un-patterned CNT film by patterned isotropic conductive adhesive (ICA)

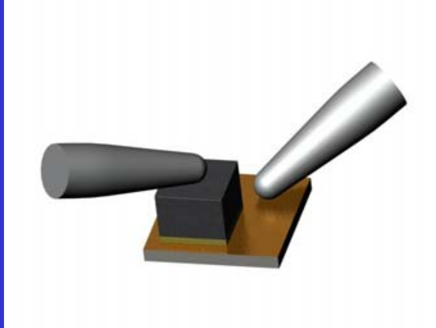
CNT Transfer by ICA

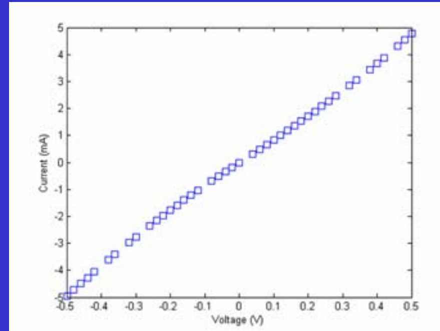
- Patterning of ICA
  - An "imprinting and transfer" process
- The transfer and formation of CNT bumps achieved at the same time



IV Measurement of CNT-ICA Structure

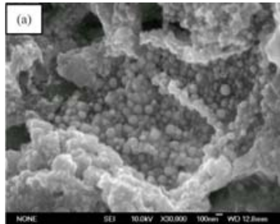
- **Two probe measurement**

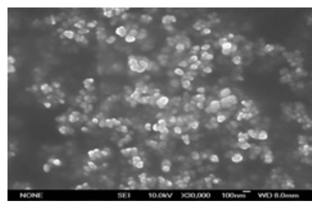


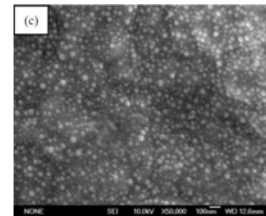


Low Temperature Transfer and Formation of Carbon Nanotube Arrays by Imprinted Conductive Adhesive, T. Wang, B. Carlberg, M. Jönsson, G.-H. Jeong, E. E.B. Campbell and J. Liu, APPLIED PHYSICS LETTERS **91**, 093123 _2007.

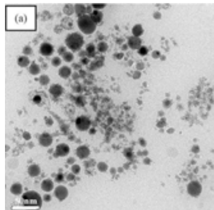
Nano Lead Free Solder Paste

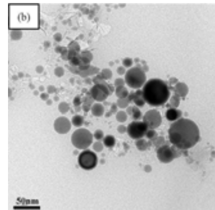


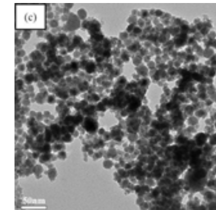




(a) Sn-3.0Ag-0.5Cu, **(b) Sn-0.4Co-0.7Cu** **(c) Sn-57Bi**

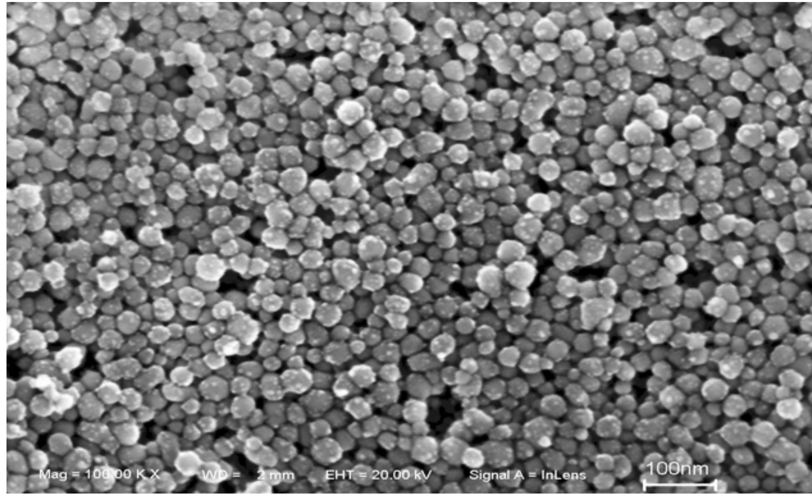






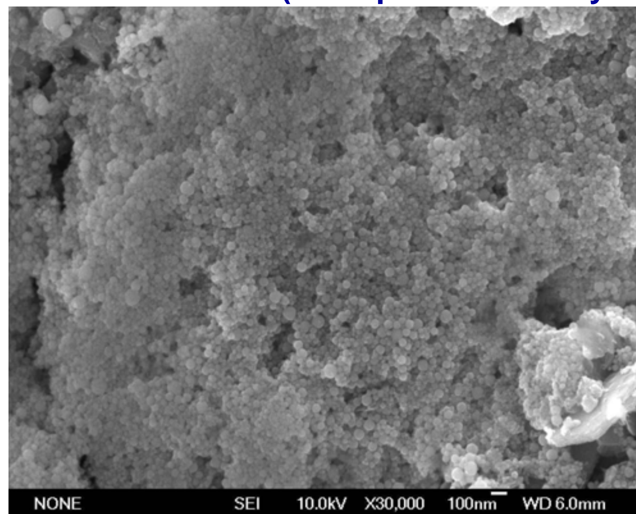
Characterization of Nanoparticles of Lead Free Solder Alloys, Wanbing Guan, Suresh Chand Verma,Yulai Gao, Cristina Andersson, Qijie Zhai1 and Johan Liu, (ESTC2006), September 5-7, 2006, Dresden, Germany, pp.7-12.

Nanosized-Lead Free Powder: Sn58Bi

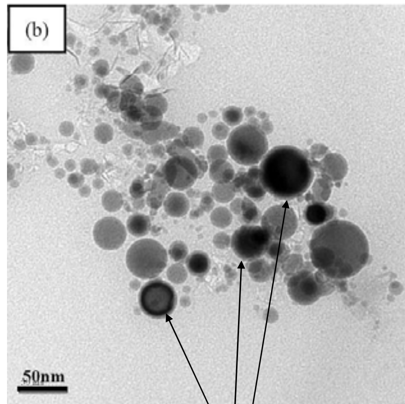


TMS Online Spotlight paper, Sept 5, 2007 http://materialstechnology.tms.org

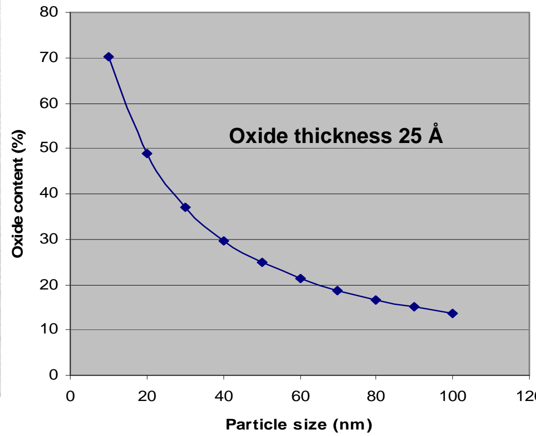
High volume of nanoparticles produced with good size control and distribution (Example: SAC305 system)



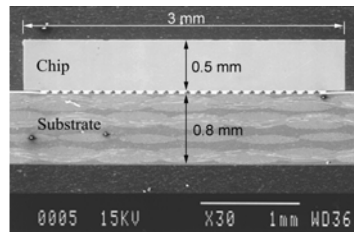
Oxide content in nano-particles

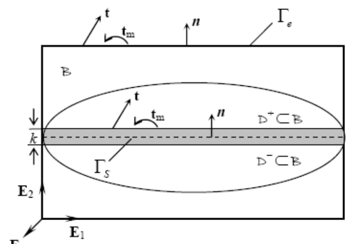


Oxide layer



Reliability modelling using micropolar interface model to describe the interfacial properties and inhomogenities for microsystems





Sketch map of the interconnect system

Displacement $\mathbf{u} = \mathbf{u}(\mathbf{x},t)$
Rotation $\theta = \theta(\mathbf{x},t)$

Interface

$$\mathbf{u} = \mathbf{u}_c(\mathbf{x},t) + H_s(\mathbf{x})\mathbf{d}_u(\mathbf{x},t)$$
$$\theta = \theta_c(\mathbf{x},t) + H_s(\mathbf{x})d_\theta(\mathbf{x},t)$$

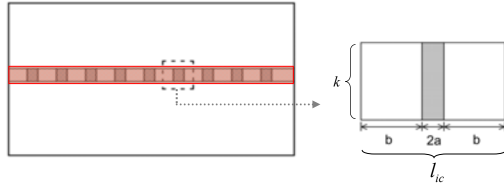
Continuous part — Discontinuity

Regularization

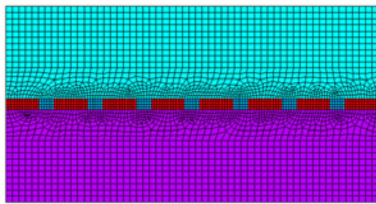
Kinematic equations
Balance relations
Constitutive relations
……

Micropolar Interface Model

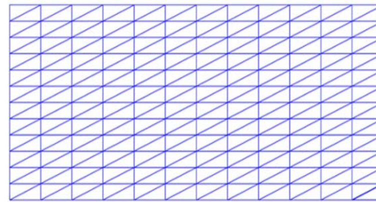
Interface/interconnect with internal structures



Internal structure parameters can be involved in interface stiffness coefficients (intrinsic)

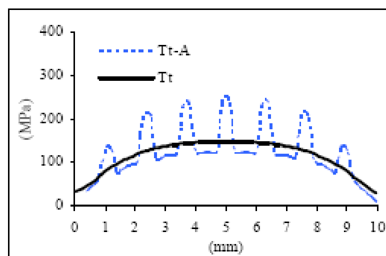


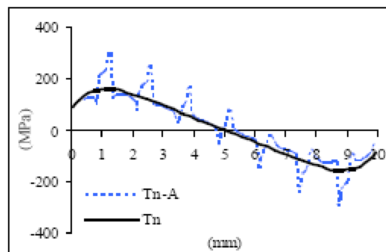
Mesh in ANSYS resolving finescaled interface



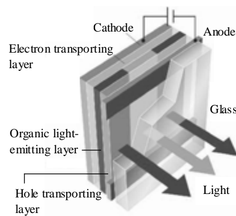
Mesh in micropolar model simulation resolving macroscale

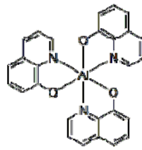
Stress distribution along the interface centerline



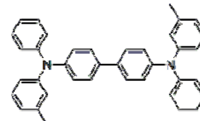


OLED Encapsulation by Nano Anisotropic Conductive Adhesive With controlled filler Size and Properties

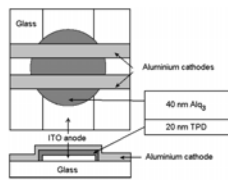




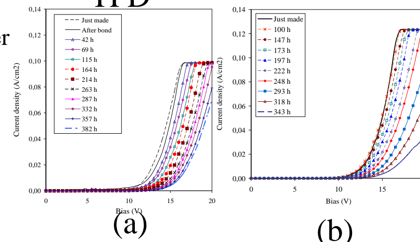
Alq3 as green light emitter



TPD



Operating OLED sample



IV characteristics of OLED samples at different exposure time: (a) Encapsulated sample; (b) Reference sample.

Acknowledgements

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