



# IPC/iNEMI Reliability Summit

Michael Freda, Karl Sauter,  
Keith Newman & David Love

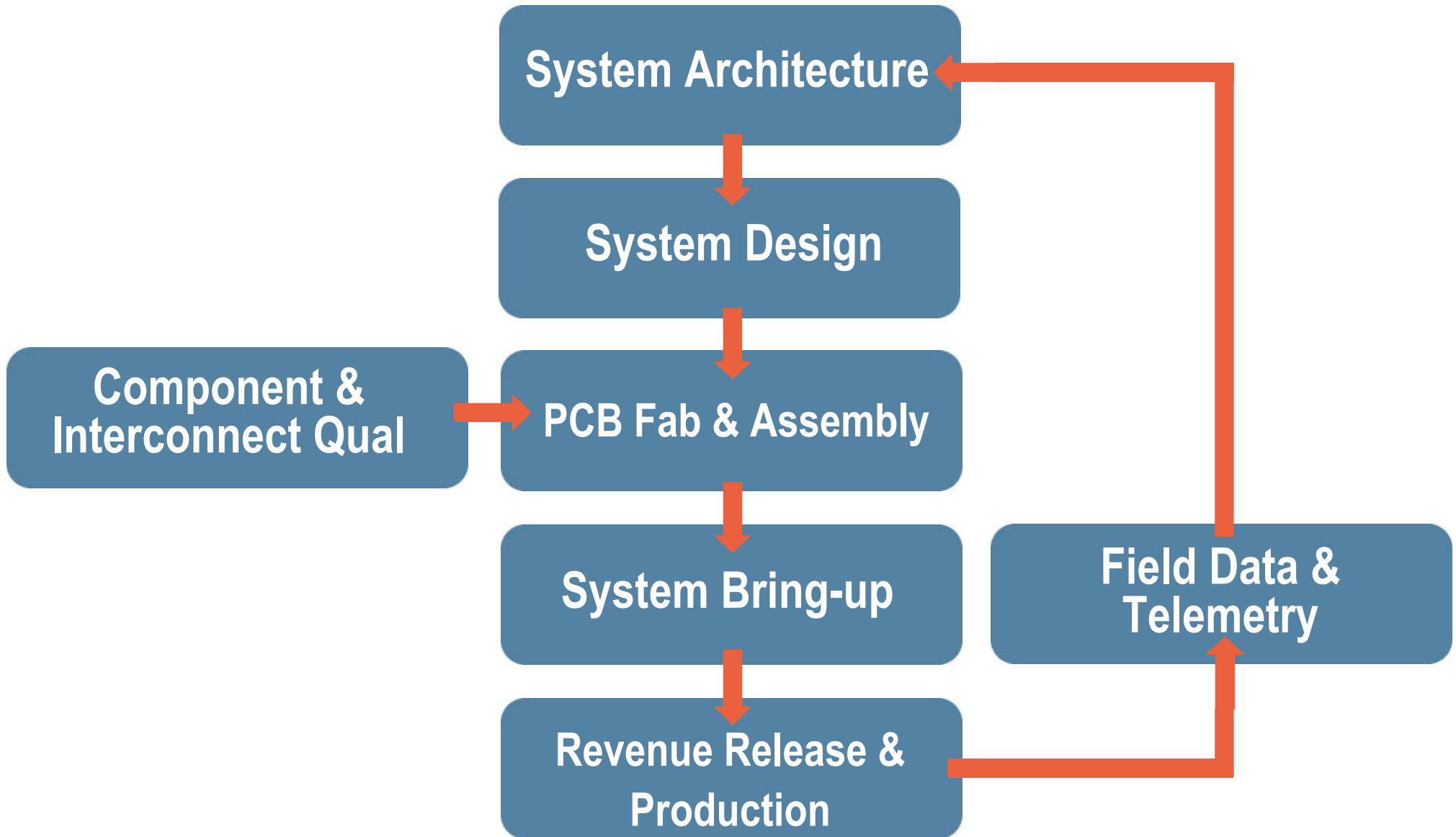
Sun Microsystem, Inc.  
Semiconductor Packaging & PCB Technology  
Interconnect Technologies & Materials



# Reliability@Sun

- High Level View
- Detail on Interconnect Reliability
- Interconnect Reliability Philosophy
- Summary
- Q & A

# High Level View of Reliability@Sun



# High Level View of Reliability@Sun

- System Architecture

- > RAS

- Architect to eliminate single points of failure
    - Example #1, fans
      - Monitor torque/speed to understand when fan failure is expected
      - Design-in excess fan capacity, i.e., is  $2N$  or  $N+1$  required
      - Use telemetry capability to “call home” for replacement when needed
      - Hot swap replacement to eliminate system down-time
    - Example #2, use integration at the chip level & silicon scaling to reduce the number of L1, L2 & L3 interconnects

- > FIT Rates

- Need to understand failure rates of all components & interconnects

# High Level View of Reliability@Sun

- System Design
  - > Simulation
  - > Test Vehicles
  - > Verification of simulation models
  - > Layout design rules
    - Interactive design rule enforcement
  - > Multiple levels of design reviews
    - Product engineering, OPS engineering, Suppliers...
  - > On-site DFM & DFA review by suppliers
  - > Post-check prior to fab sign-off & release to fab

# High Level View of Reliability@Sun

- Component level qualification
  - > Pre-qualification of laminate materials
  - > L1 & L2 interconnect qualification
- PCB Fabrication
  - > On board or on panel process monitors
    - Impedance, DC resistance, CAF, IST
  - > First article report with Cpk data
    - Requires action plan if inadequate Cpk
- Assembly
  - > L2 & L3 interconnect qualification
  - > Use strain gages to monitor PWB strain during board assembly, test & shipment & to optimize process

# High Level View of Reliability@Sun

- System Bring-up
  - > DVT (Design Verification Test)
    - Signal integrity DVT
    - Functional DVT
    - Configuration DVT
  - > RQT (Reliability Qualification Test)
    - Run sufficient number of system hours to validate MTBF
      - Quantity of systems & time...
  - > ORT (Ongoing Reliability Test)
    - Sample plan selected to detect a change in reliability baseline

# High Level View of Reliability@Sun

- Field Operation
  - > Continuous System Telemetry - System variables continuously sampled & recorded, i.e., “Black Box”
  - > Data analyzed remotely using advanced statistical pattern recognition software (MSET – Multivariate State Estimation Technique)
  - > MSET software can identify onset of potential failures & allow for proactive correction
  - > Telemetry harness captures actual field use conditions, aiding correlation between accelerated stress testing & end-use lifetime

# Reliability@Sun

- High Level View
- **Detail on Interconnect Reliability**
- Interconnect Reliability Philosophy
- Summary
- Q & A

# Detail on Interconnect Reliability

- Solder Joint Reliability
- CAF Testing
- Via reliability testing
- Hi-Pot testing

# Solder Joint Reliability





- Solder joint integrity test assessment methods
  - > Component-level
    - Solder ball attached to component
  - > Board-level
    - Component attached to PWB
- Solder joint stress conditions
  - > Thermal
    - Power cycling (main & mini) in actual use
    - Ambient operating temp (cyclic & high temp)
  - > Mechanical
    - Component handling, test & shipment
    - Board assembly, handling test & shipment

Component & assembly suppliers need to look at both sides of this issue, not just one side...

# Solder Joint Reliability, cont'

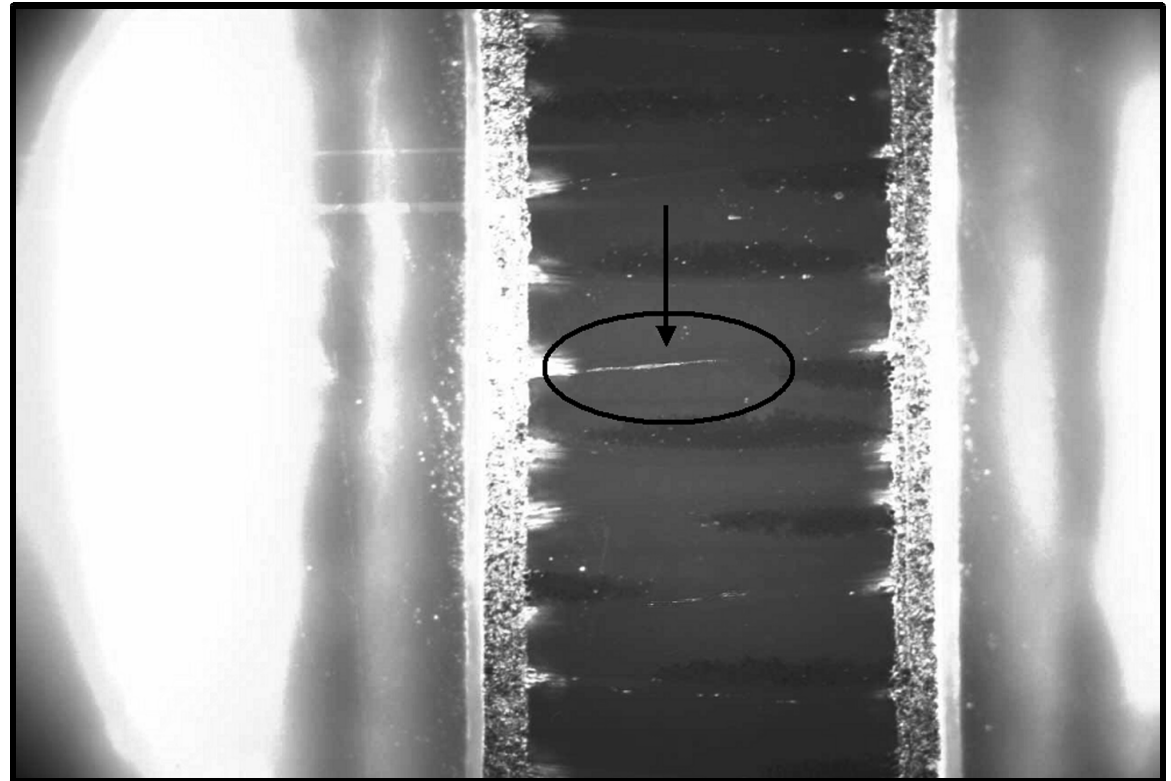
- Solder joint stress conditions, cont'
  - > Mechanical
    - Component handling, test & shipment
    - Board assembly, handling test & shipment
  - > End use
    - Drop/impact (test simulates 6 foot fall off a lift-gate truck)
    - Keypad
- Standardized test methods
  - > Component-level
    - Solder ball shear (JESD22-B117A)
      - Low-speed (0.1 - 0.8 mm/s)
      - High-speed (100 - 4000 mm/s)

# Solder Joint Reliability, cont'

- Standardized test methods, cont'
    - > Solder ball pull (release 6/2007)
      - Low-speed (0.1 - 15 mm/s)
      - High-speed (15 - 1000 mm/s)  **NEW!**
  
  - Board-level
    - > Temperature Cycle (IPC-9701A)
    - > Monotonic Bend (IPC/JEDEC-9702)
    - > Cyclic Bend (JESD22-B113) 
    - > Mechanical Shock
      - Handheld devices (JESD22-B111) 
      - Large devices & sub-assemblies (IPC-9703 draft)  **Sun plans to use**
- Applicable to handheld devices**

# CAF Testing (IPC-TM-650 2.6.25)

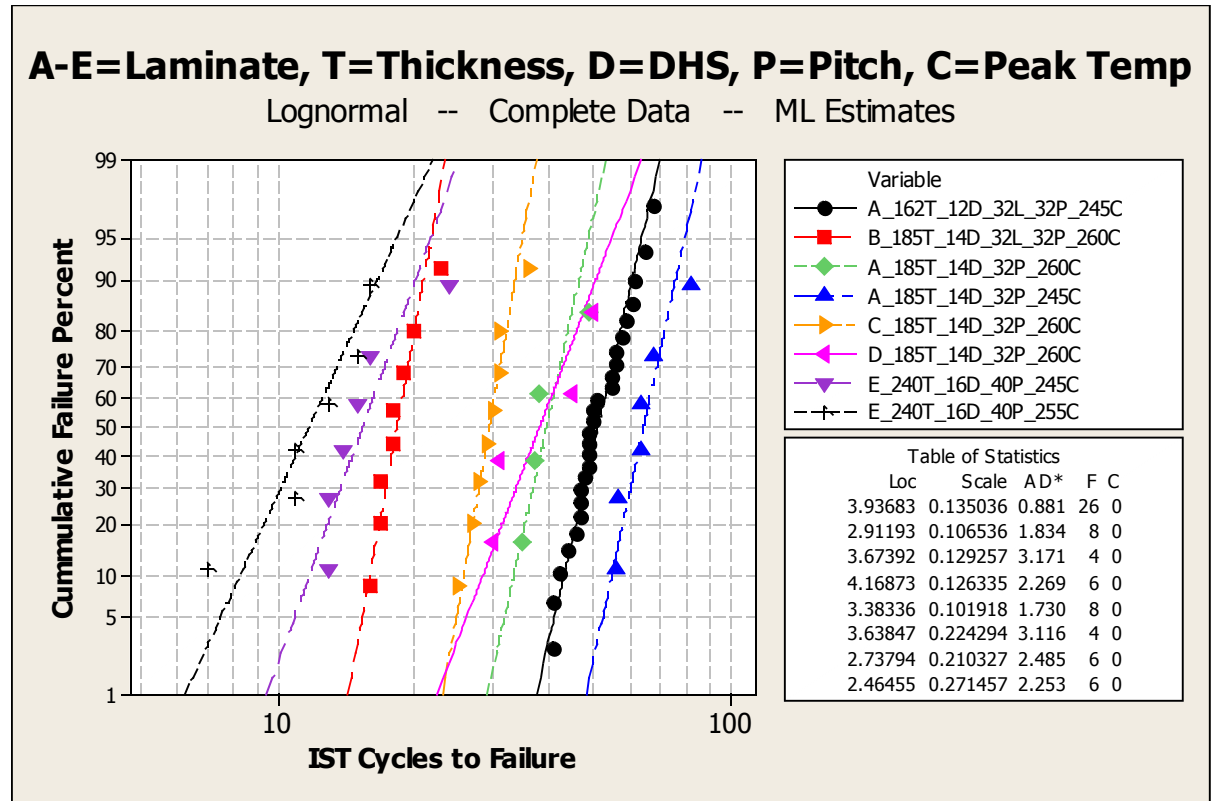
- Necessary requirement as pitch & drill edge-to-edge pitch decreases
- Long term reliability issue driven by
  - > Temperature
  - > Humidity
  - > Bias voltage
- Key factors are:
  - > Laminate material
  - > Layer ionic cleanliness
  - > Amount of drill fracture
- Moving from qualification to baseline with on-board coupons



# Via Reliability Testing

- Qualification

- > 3x & 6x thermal stress
  - (IPC-TM-650 2.6.8)
- > APD-Oil-T-Shock
  - (IPC-TR-579)
- > Interconnect Stress Test
  - (IPC-TM-650 2.6.26)
- > Highly Accel Thermal Stress
  - (MIL-STD-202 Method 107)
- > Kelvin 4-probe of via resistance
  - Measure, 6x reflow, measure...



- Process control

- > Thermal stress used for routine lot acceptance
- > IST used for product development & quarterly process baseline
- > Sun requires cycling to failure & allows testing at reflow peak

- Able to predict field life from thermal testing at multiple temperatures

# Hi-Pot Testing

- Required for UL compliance, test is...
  - > 500 VDC minimum, 50 M $\Omega$  minimum
  - > 50 volt/sec ramp to 500VDC then 5 second hold
- Issues
  - > Boards used to have GND & one or two voltages
    - Three combinations to test or 45 seconds to test per board
    - Easy for fabricator to find plane combinations to test
  - > Today boards have very complex power domains
    - Have one part number with 14 voltage potentials on 42 nets
    - Total combinations are  $[n*(n-1)]/2=91$  or 22.75 minutes/board
    - Testing needs to be well documented by Sun
    - Eliminate combinations where there is no adjacency (91  $\blacktriangleright$  15 or 3.75 min)
    - Fabricators need to use a bed of nails for Hi-Pot testing

# Reliability@Sun

- High Level View
- Detail on Interconnect Reliability
- **Interconnect Reliability Philosophy**
- Summary
- Q & A

# Interconnect Reliability Philosophy

- Use industry standards whenever possible
  - > If standard does not exist, work with industry to develop
    - IPC/JEDEC-9704 Strain Gage, IPC/JEDEC-9702 Monotonic Bend, IPC-TM-650 2.6.25 Conductive Anodic Filament (CAF) Resistance Test, IPC-9701 Solder Joint Reliability, IPC-4101B Base Material...
  - > Collaboration & partnership is a part of Sun's DNA
    - Active in IPC, iNEMI, HDPUUG, JEDEC, University partners...
- Collect data to make decisions
  - > Use industry standard test methods to collect data
  - > Use Sun specific requirements for the pass/fail criteria
  - > Baseline supplier processes with meaningful data & work on continuous improvement

# Reliability@Sun

- High Level View
- Detail on Interconnect Reliability
- Interconnect Reliability Philosophy
- **Summary**
- Q & A

# SUMMARY - Reliability@Sun

- System reliability is a complex task
  - > 1<sup>st</sup> need to minimize un-reliability in the system architecture
  - > then need to aggressively work on the remaining largest contributors
- You must understand the reliability of all components & of all interconnects
  - > Data, data, data...
- The best & most sensible practice is to collaborate with the industry on standards because...
- Sun is not big enough to do it alone



# Thank You Any Questions?

[Michael.Freda@SUN.Com](mailto:Michael.Freda@SUN.Com)

[Karl.Sauter@SUN.Com](mailto:Karl.Sauter@SUN.Com)

[Keith.Newman@SUN.Com](mailto:Keith.Newman@SUN.Com)

[David.Love@Sun.COM](mailto:David.Love@Sun.COM)