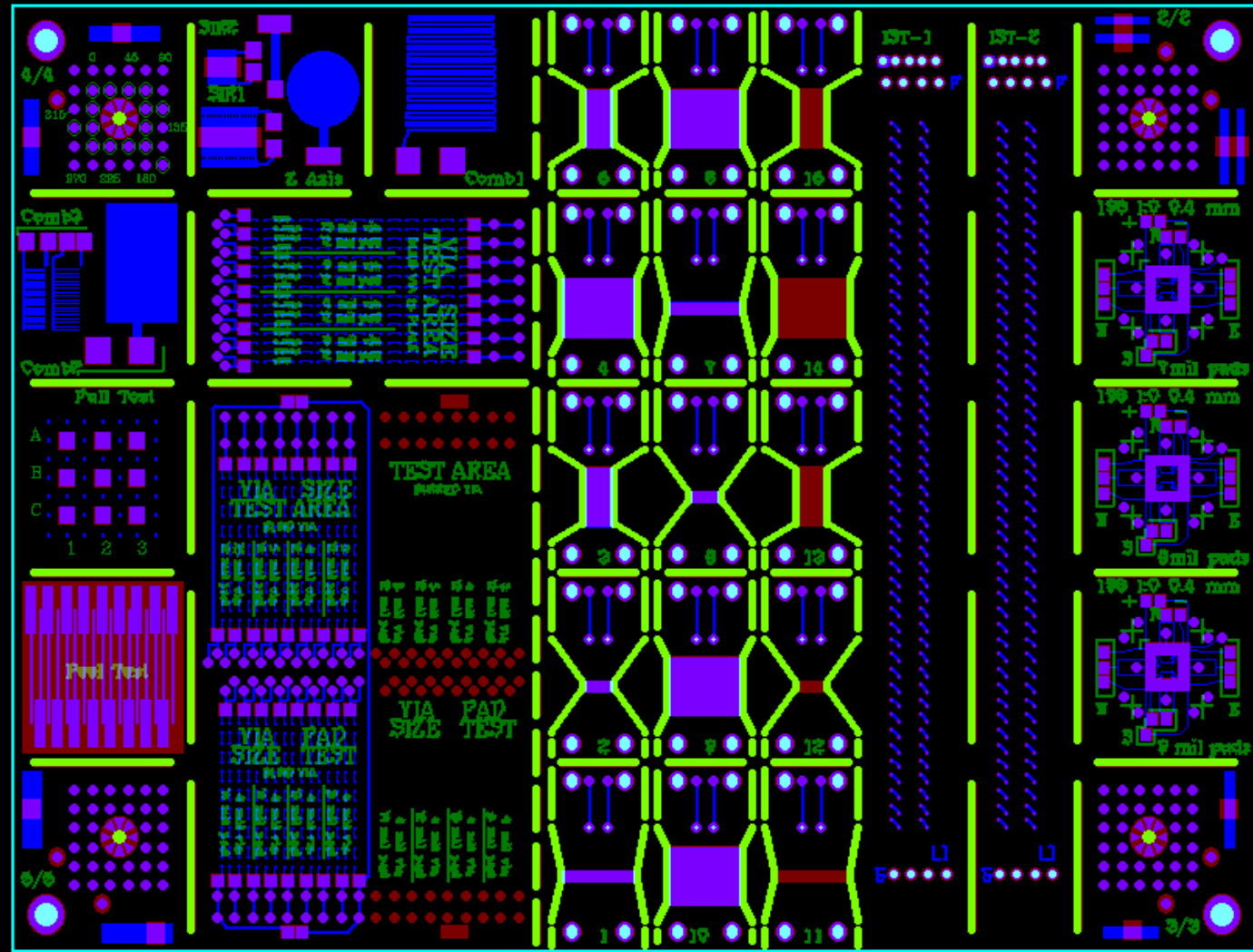


Guidant - CRM
Advanced Process Development (APD)
Test Board # 1
(Dyconex)

Specifications / Design Overview

5 inch

1 inch
1 inch
1 inch
1 inch
1 inch

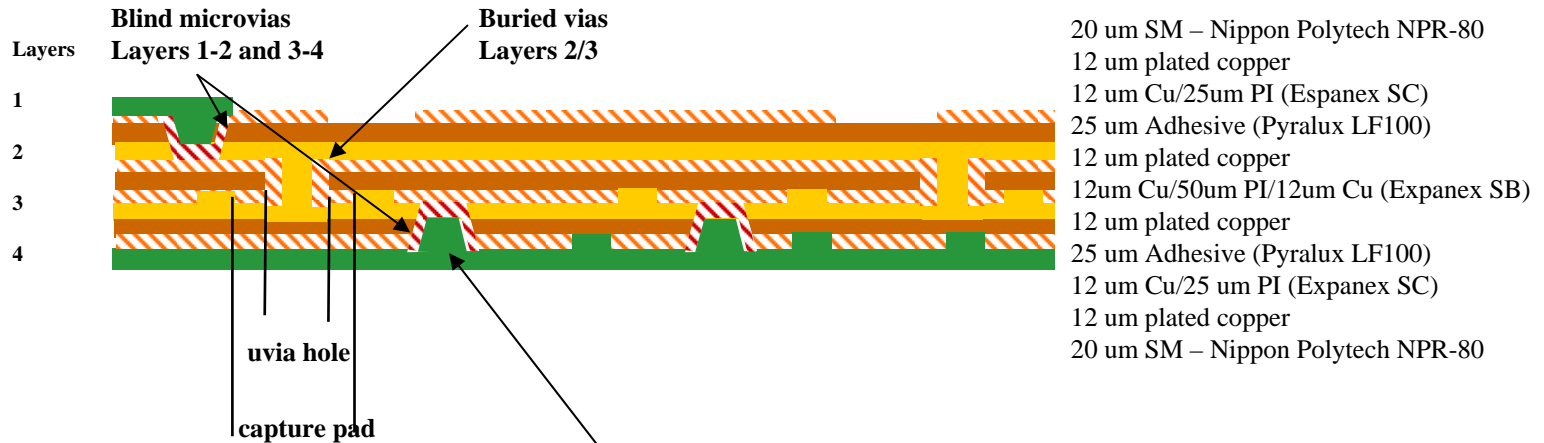


1 inch 1.95 inch 2.45 inch 0.6 inch 1 inch

7 inch

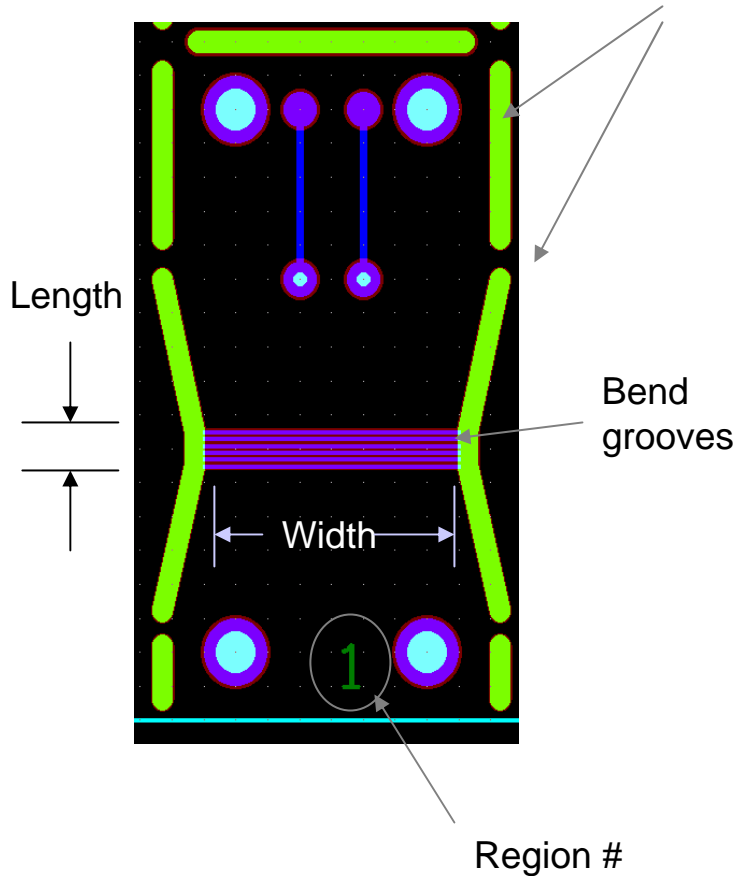
Typical construction of 4 layer flex test board

1-1-1 Construction layout For 4 layer Blind and Buried Flex Circuit

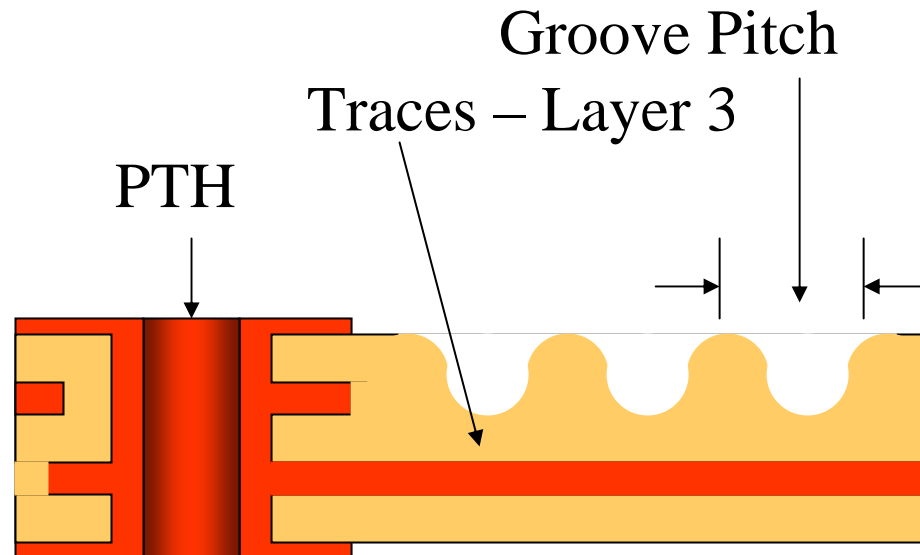


Via Construction : Laser, plasma, etc

Remove – 0.031" router cutter regions



Bend Region Side View



Region 1

Grooves – 0.010" Pitch (layer 1)

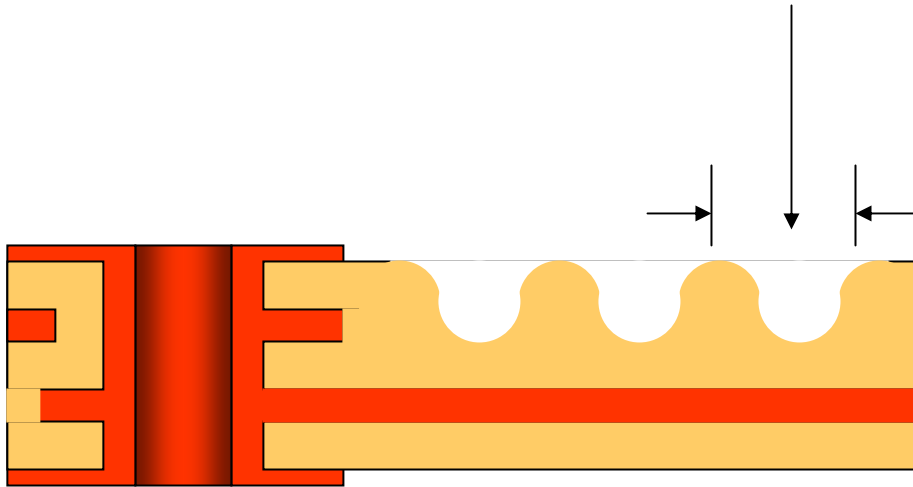
Traces – 0.005" line/space (layer 3)

Bend Width 0.40"

Bend Length 0.050"

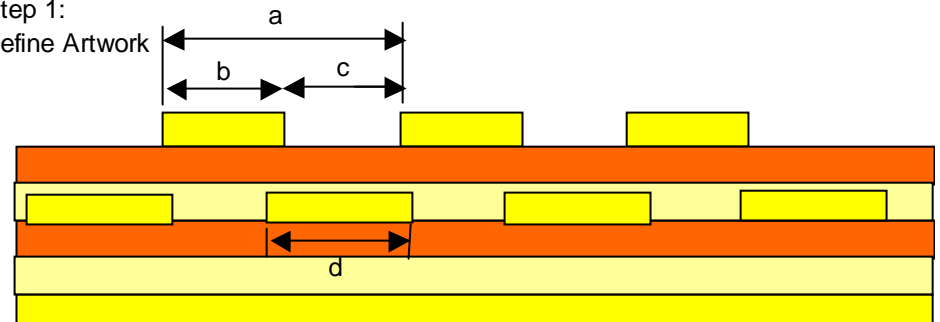
Bend Groove Design Dimensions

Groove Pitch (a)



(Dyconex Defined)			
PCB Bend Area Design (Figure 1) (mm)			
a	b	c=a-b	d
0.254	0.14	0.114	0.127
0.305	0.157	0.147	0.16
0.254	0.135	0.119	0.132
0.305	0.152	0.152	0.165

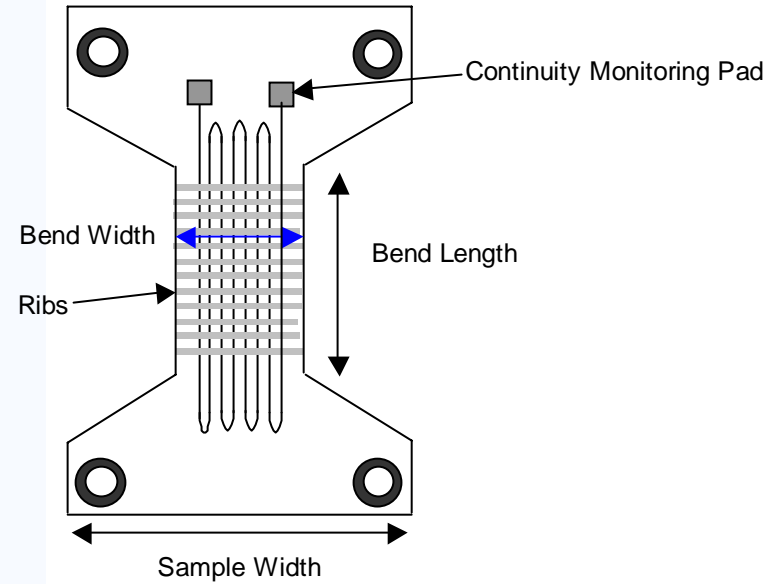
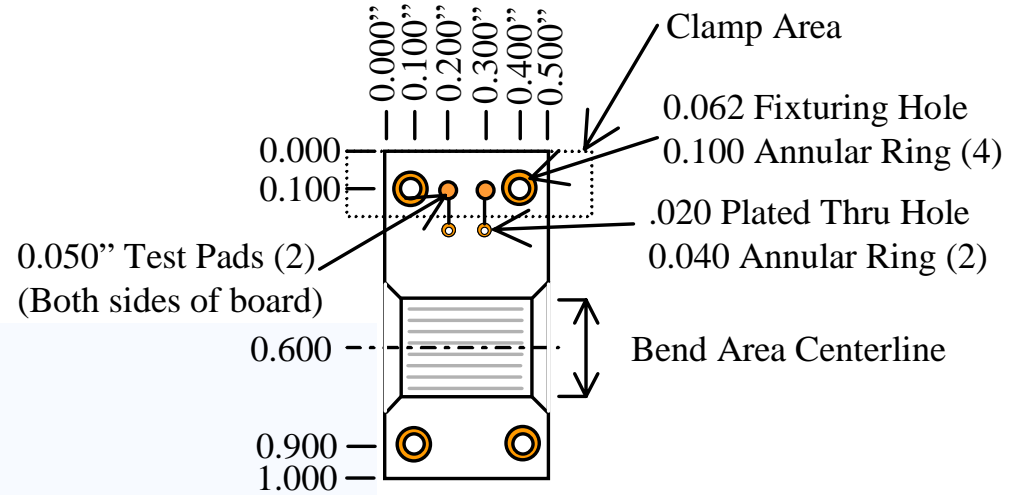
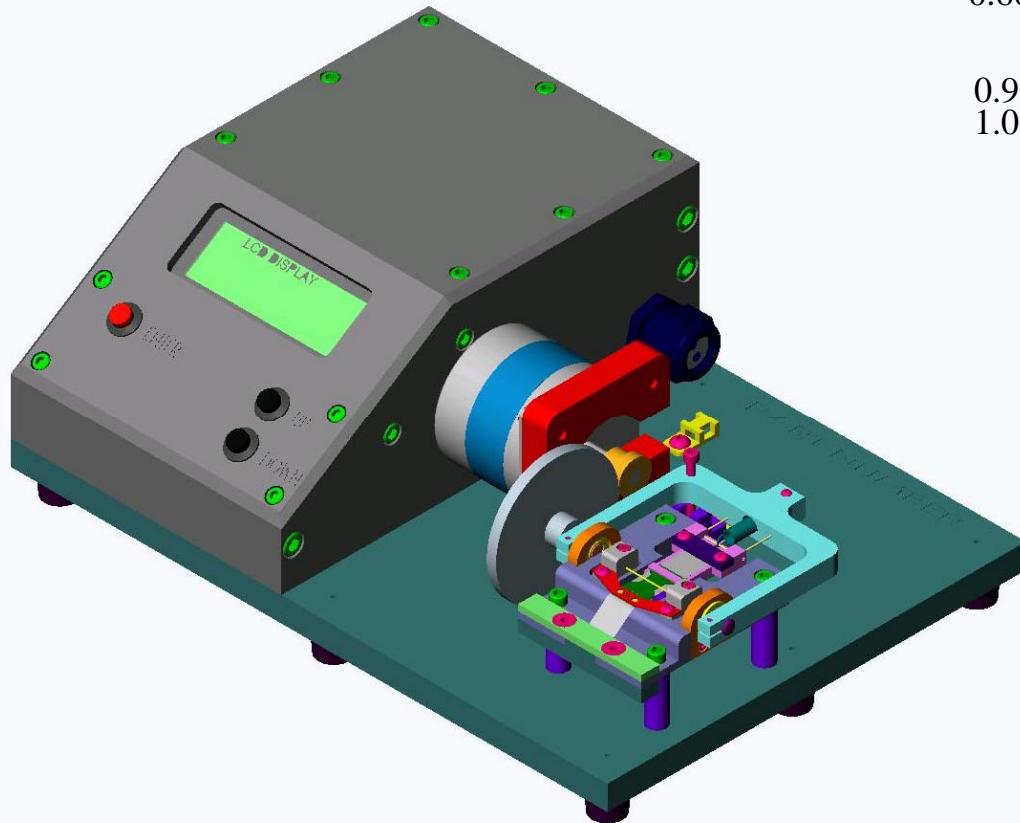
Step 1:
Define Artwork



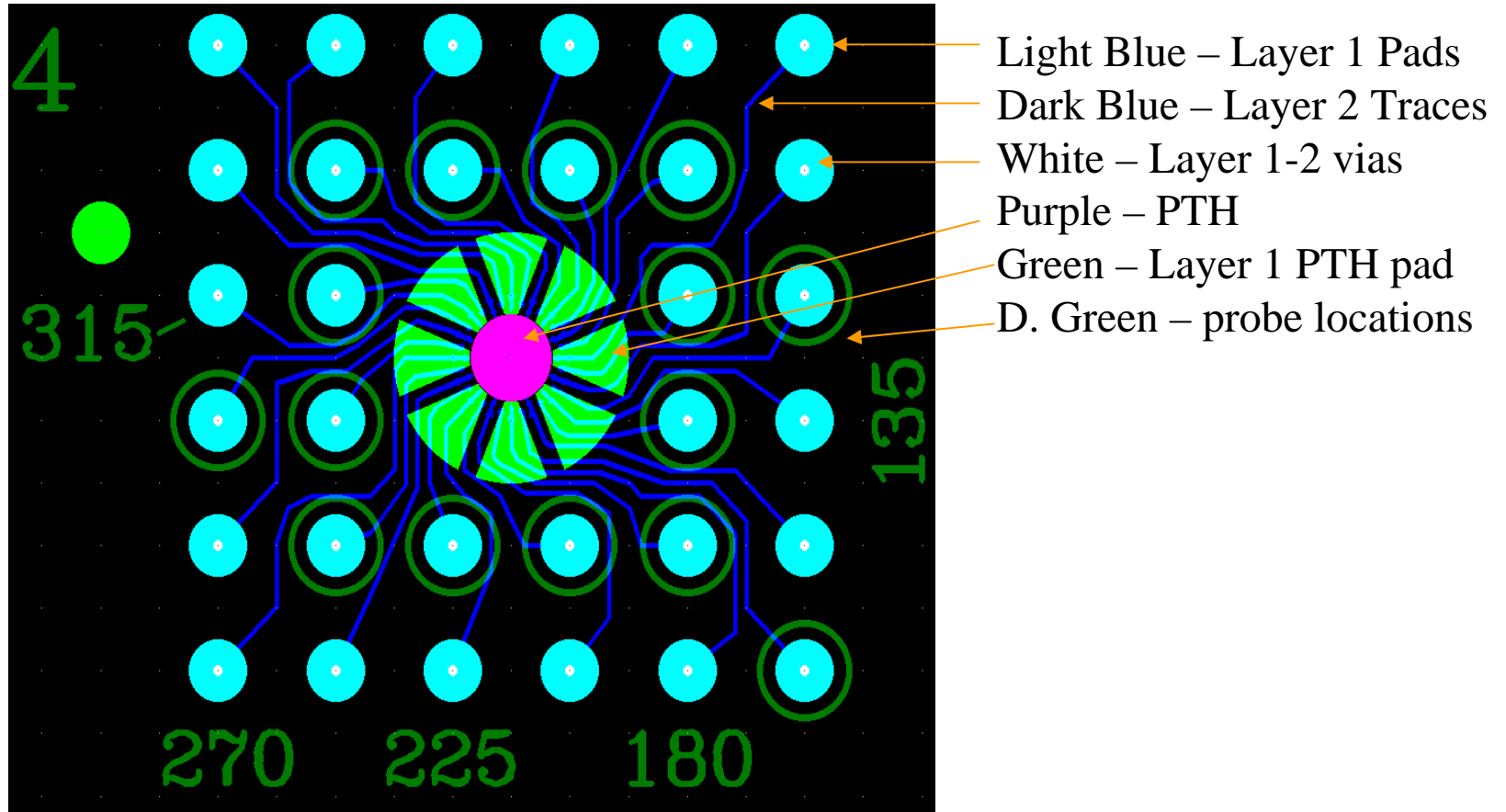
Bend Groove Design Dimensions

Site	Pitch (mm)	d-c ratio	trace width	Bend Length	Bend Width	Dim a (mm)	Dim b (mm)	Dim c (mm)	Dim d (mm)	Note
1	0.254	0.005"	0.005"	.050"	.400"	0.254	0.140	0.114	0.127	Ribs
2	0.305	0.005"	0.005"	.050"	.150"	0.305	0.157	0.147	0.160	Ribs
3	0.254	-.005"	0.005"	.300"	.150"	0.254	0.135	0.119	0.132	Ribs
4	0.305	-.005"	0.005"	.300"	.400"	0.305	0.152	0.152	0.165	Ribs
5	0.254	0.005"	.004"	.300"	.150"	0.254	0.140	0.114	0.127	Ribs
6	0.305	0.005"	.004"	.300"	.400"	0.305	0.157	0.147	0.160	Ribs
7	0.254	-.005"	.004"	.050"	.400"	0.254	0.135	0.119	0.132	Ribs
8	0.305	-.005"	.004"	.050"	.150"	0.305	0.152	0.152	0.165	Ribs
9	0.254	0.005"	0.005"	.300"	.400"	0.254	0.140	0.114	0.127	Ribs
10	0.254	-.005"	0.005"	.300"	.400"	0.254	0.135	0.119	0.132	Ribs
11	n/a	n/a	.005"	.050"	.400"	n/a	n/a	n/a	n/a	Smooth
12	n/a	n/a	.005"	.050"	.150"	n/a	n/a	n/a	n/a	Smooth
13	n/a	n/a	.005"	.300"	.150"	n/a	n/a	n/a	n/a	Smooth
14	n/a	n/a	.005"	.300"	.400"	n/a	n/a	n/a	n/a	Smooth
15	n/a	n/a	.004"	.300"	.150"	n/a	n/a	n/a	n/a	Smooth

Bend Test Machine & Coupon

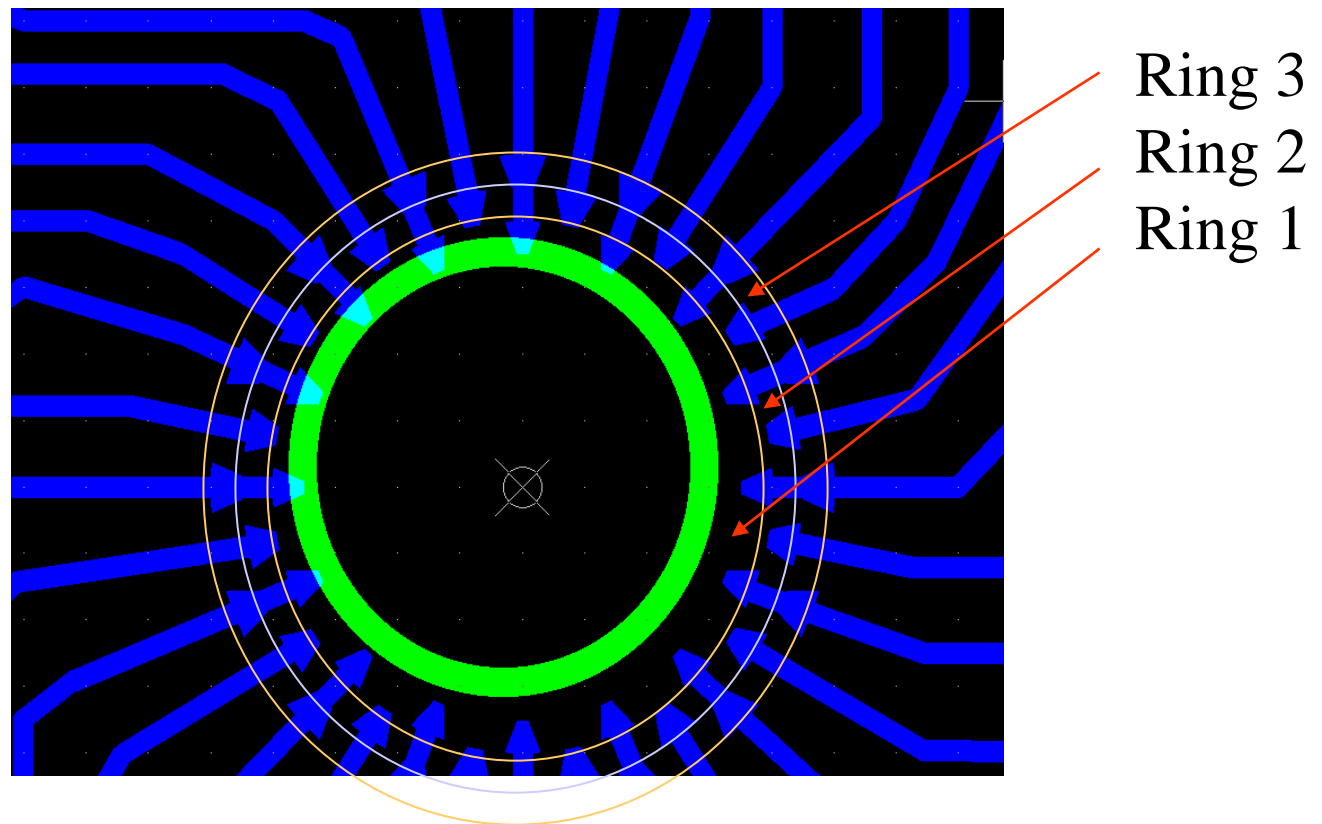


Probe Regions – Qty – 8 (4 top and bottom)



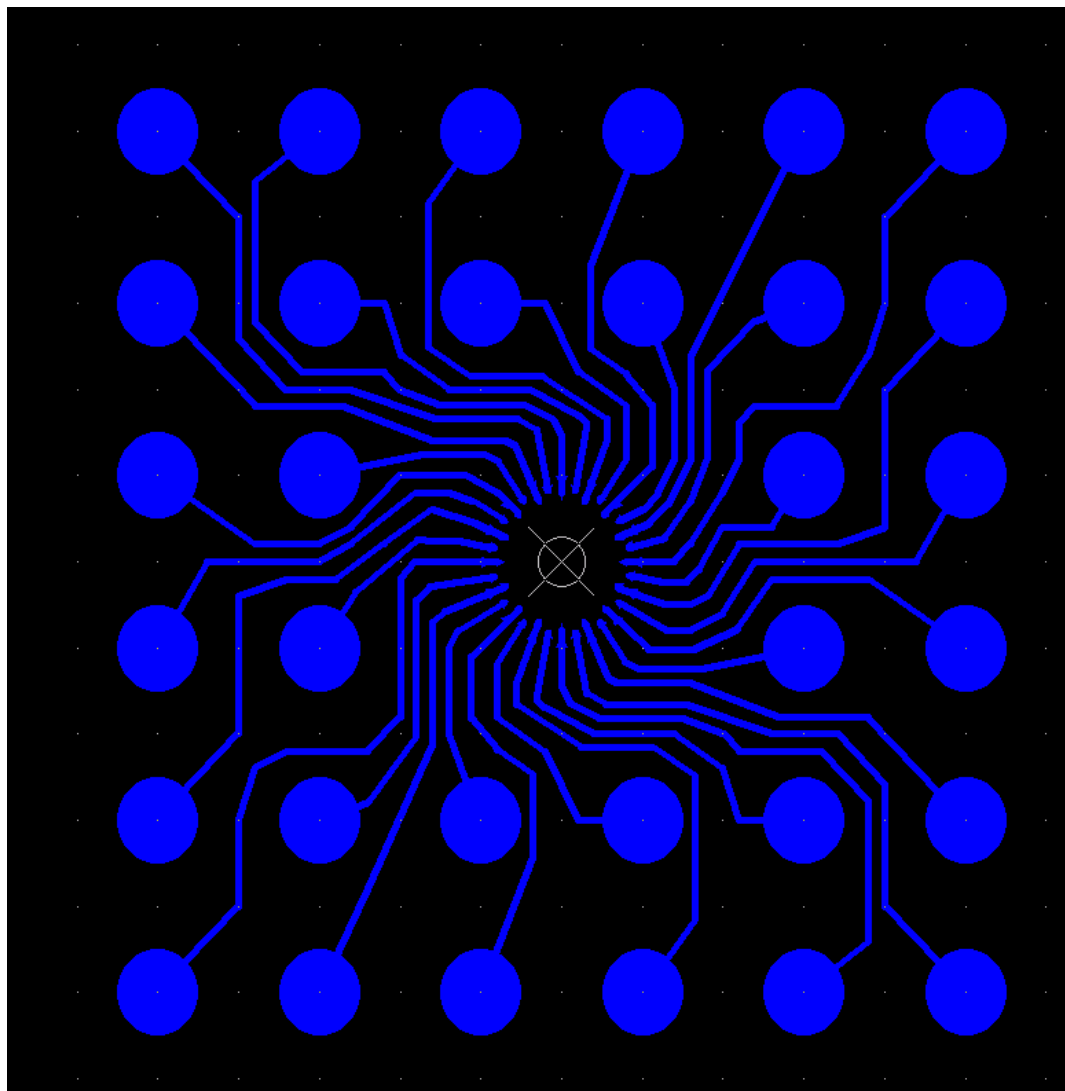
Layer to Layer Positional Test

As PTH position shifts,
Continuity in chains change location
Resolution in 360 degrees
Detects approx 1/2 mil shifts or less



A B C D E F

1
2
3
4
5
6



Electrical Map

#	R,C	Ring	#	R,C	Ring
1	B1	1,3	17	E6	1,3
2	B2	2	18	E5	2
3	C1	1,3	19	D6	1,3
4	C2	2	20	D5	2
5	D1	1,3	21	C6	1,3
6	D2	2	22	C5	2
7	E1	1,3	23	B6	1,3
8	E2	2	24	B5	2
9	F1	1,3	25	A6	1,3
10	E3	2	26	B4	2
11	F2	1,3	27	A5	1,3
12	F3	2	28	A4	2
13	F4	1,3	29	A3	1,3
14	E4	2	30	B3	2
15	F5	1,3	31	A2	1,3
16	F6	2	32	A1	2

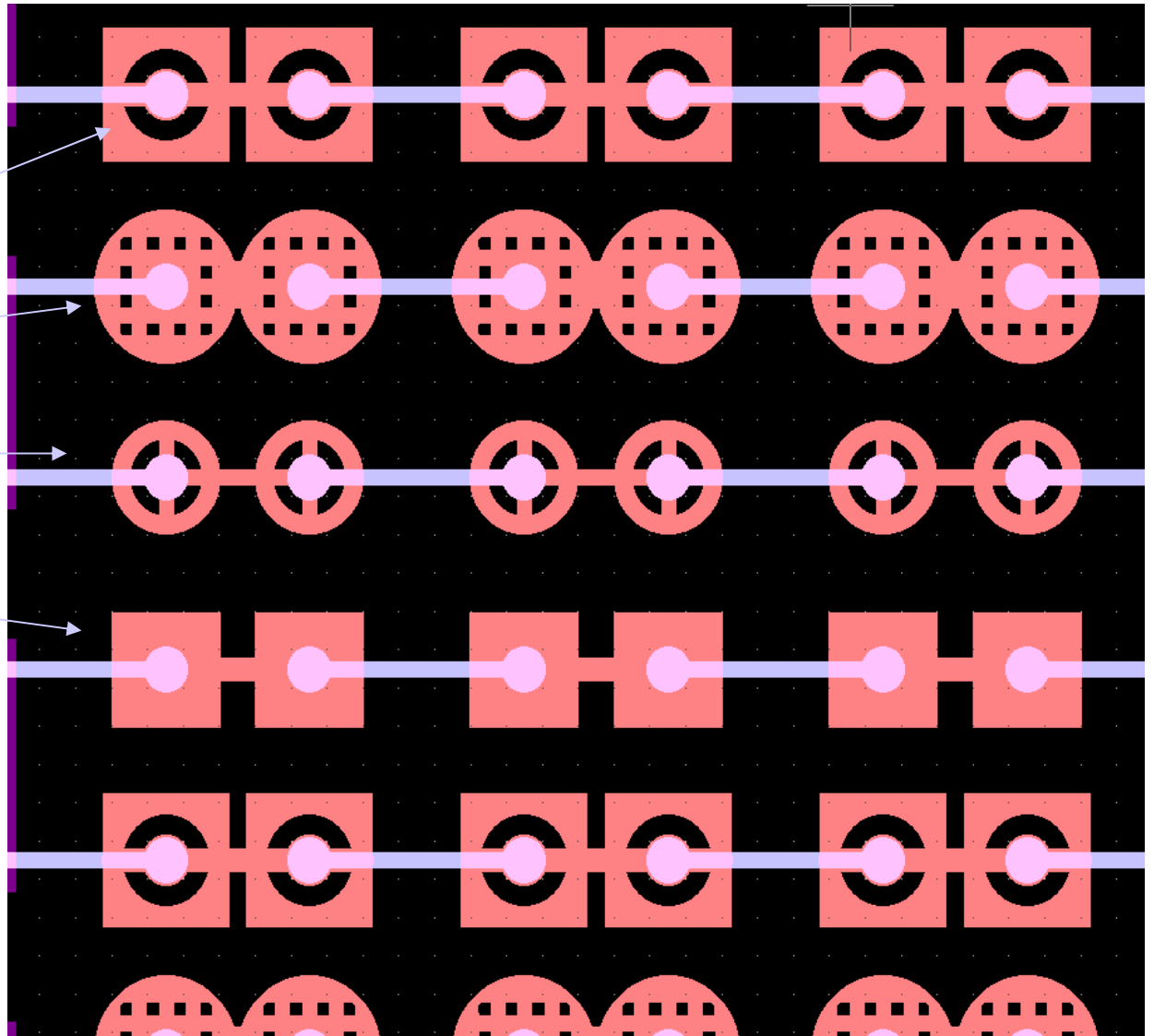
Inner Layer Pad Design

2 Spoke Relief

“Waffle”

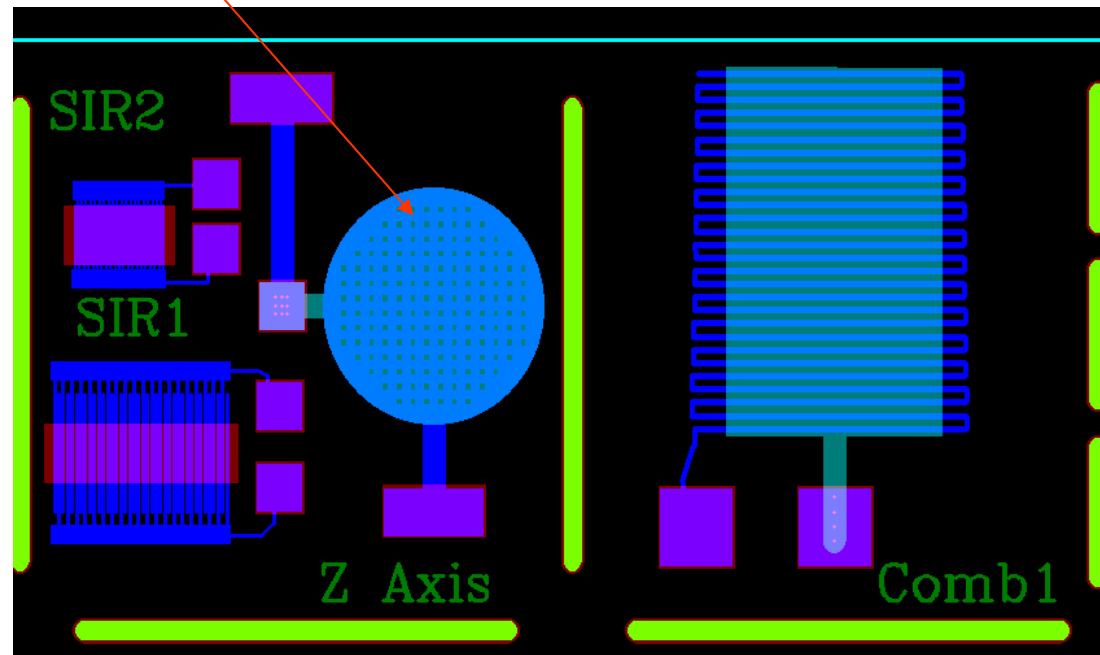
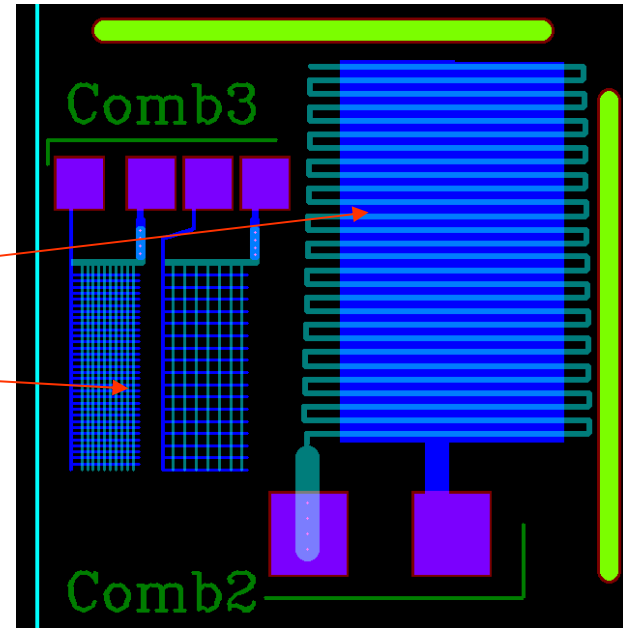
4 Spoke Relief

Solid Pad



Electrical and dielectric Property test coupons

- Z-axis conduction / cross talk
- X-Y dielectric signal integrity
- Z-Axis Capacitance
- SIR

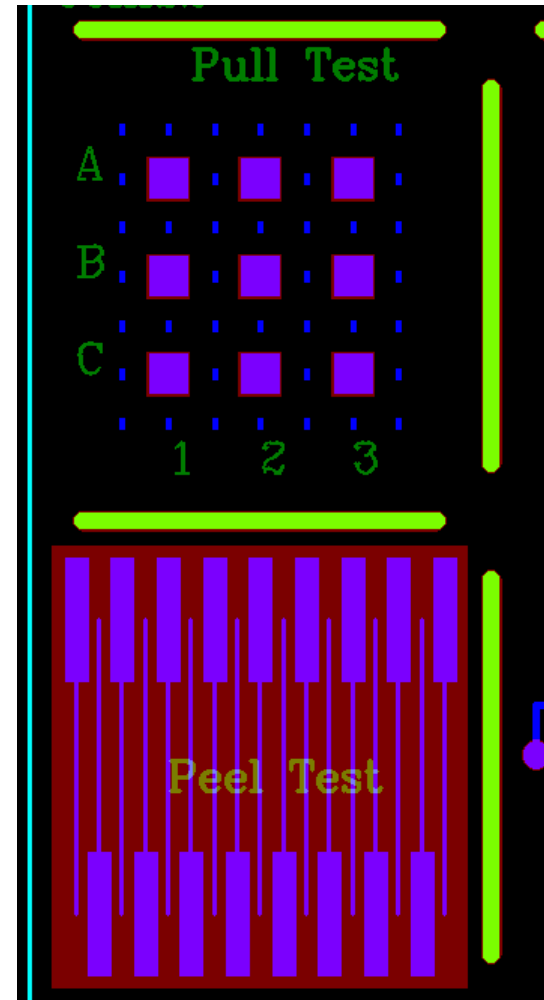
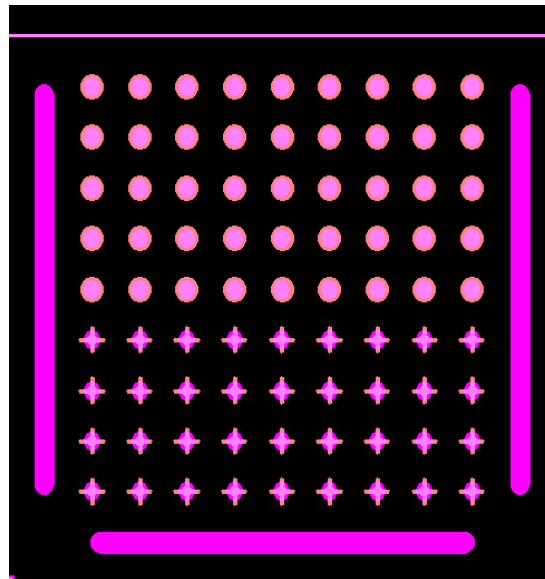


Copper Adhesion Test

Pull test coupons for pads

Peel test for trace adhesion

SMD/NSMD pads for shear



Via Test Coupons

Blind and buried vias

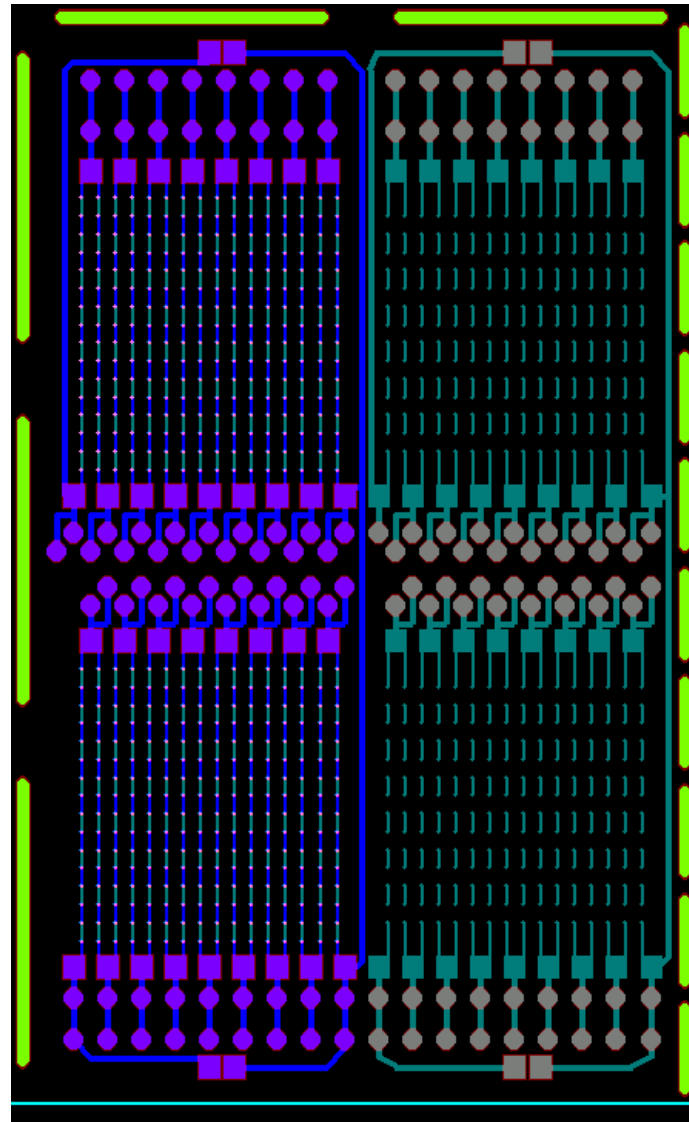
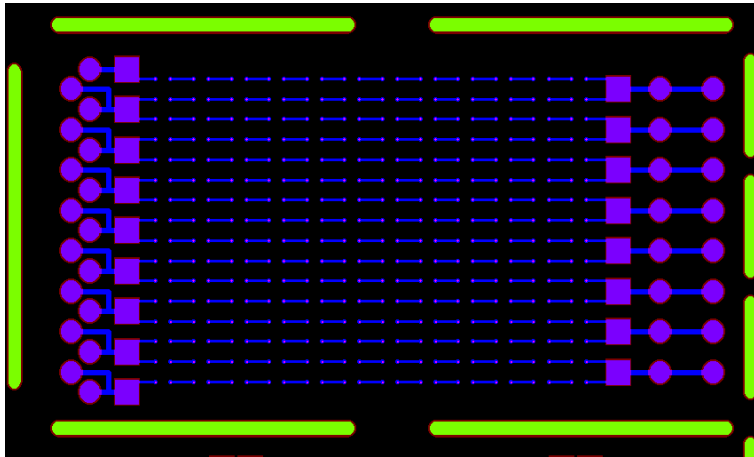
Top & bottom side

Inner layer pad design testing

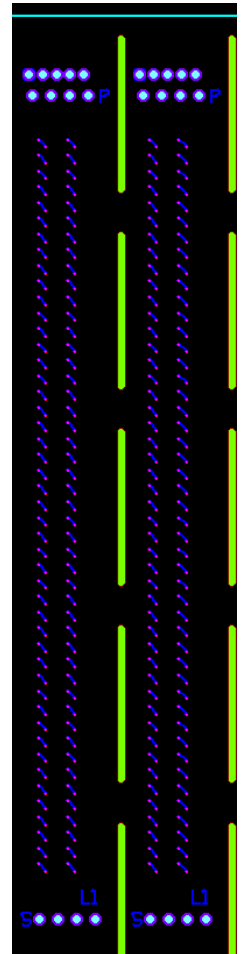
Via size / pad size testing

Daisy chain 4 point probe

IST testing



IST



Fine Pitch CSP

0.4 mm pitch

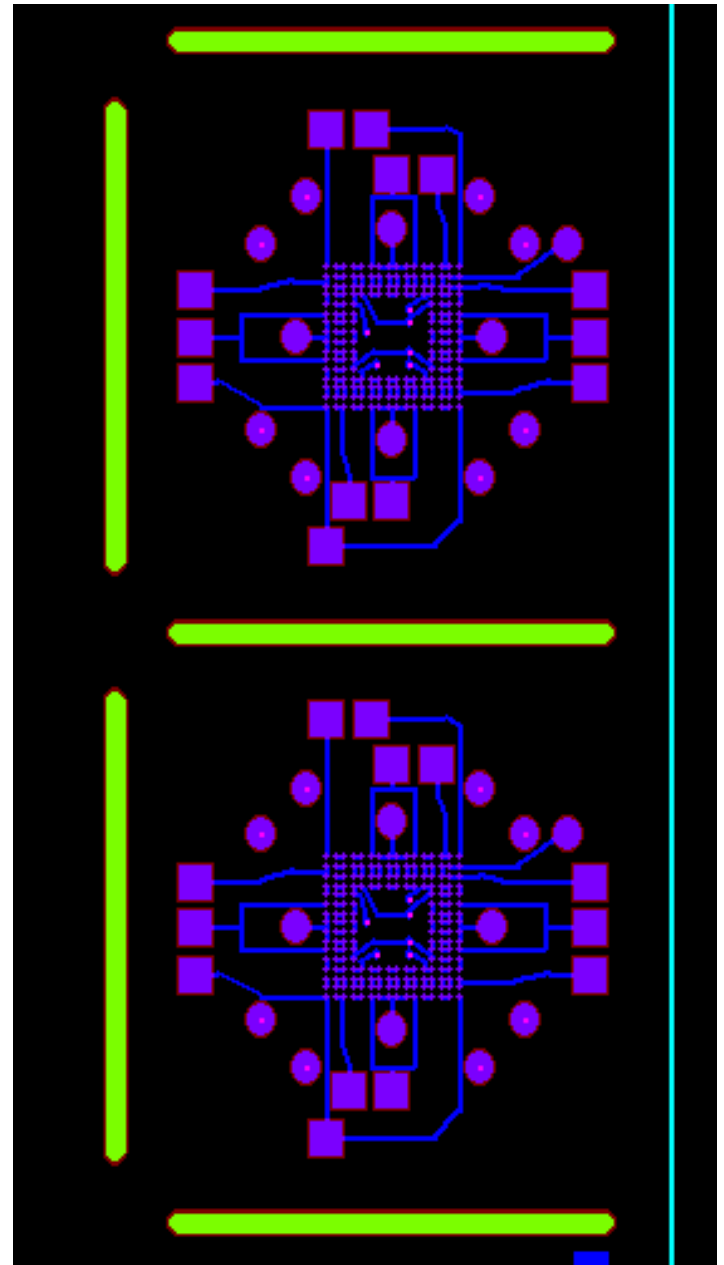
192 I/O

Sn/Pb or Pb-free solder

Molded wirebond device

Pad size variation

Process development tool



Small Passives

0 Ohm resistors

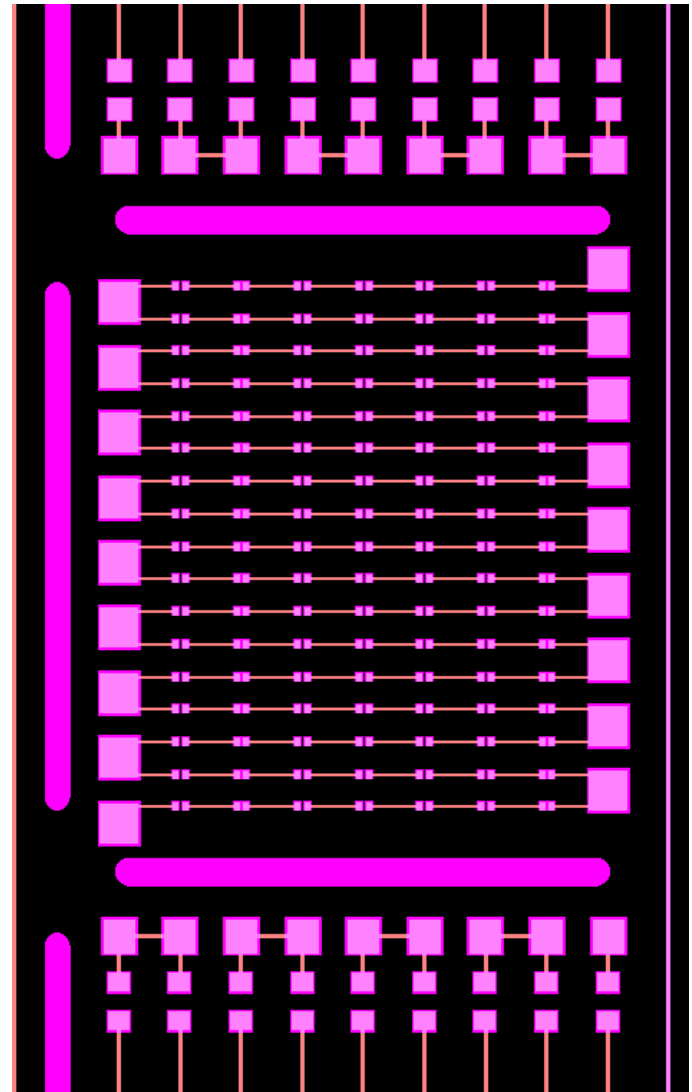
0805 (0.08" x 0.05")

0603 (0.06" x 0.03")

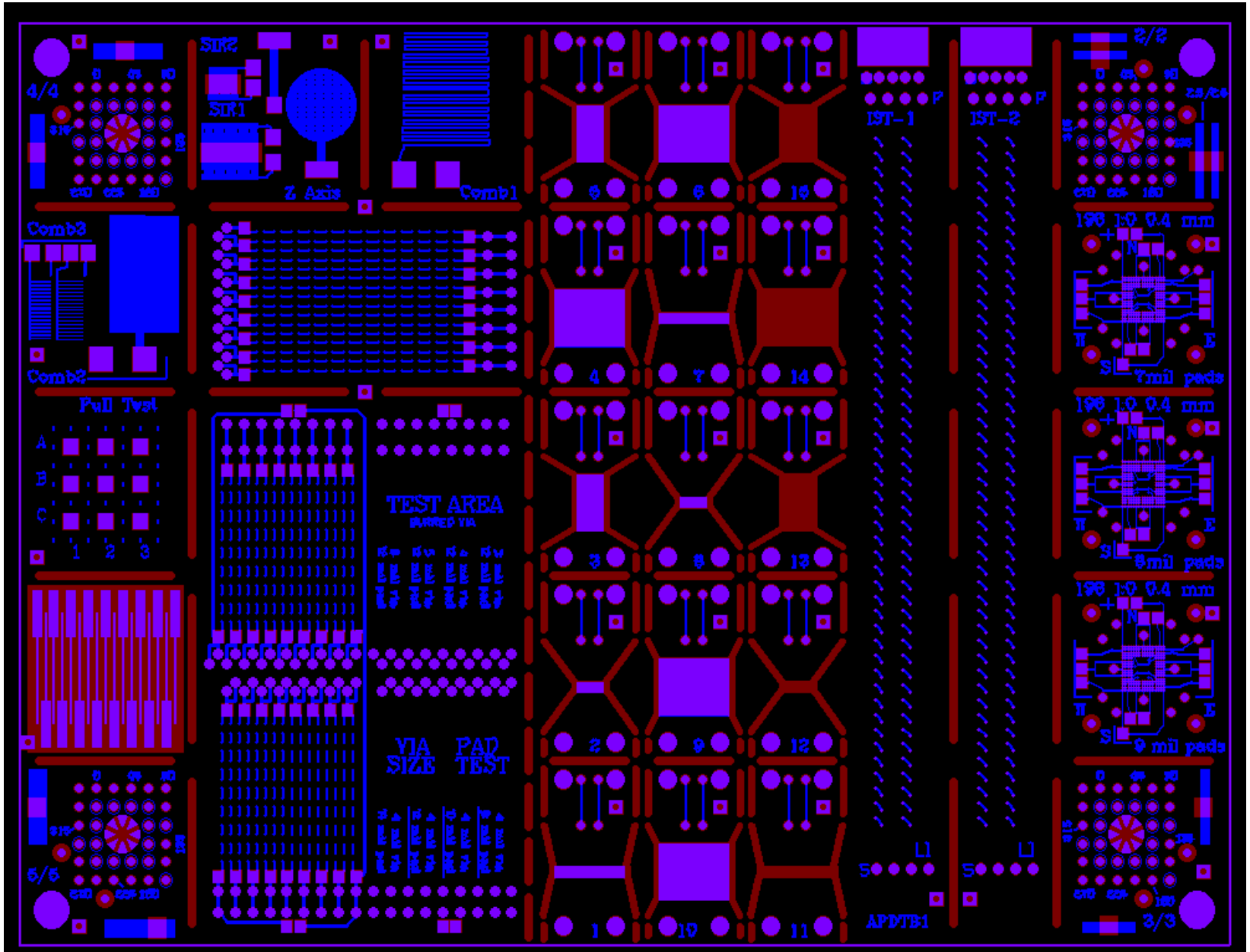
0402 (0.04" x 0.02")

0201 (0.02" x 0.01")

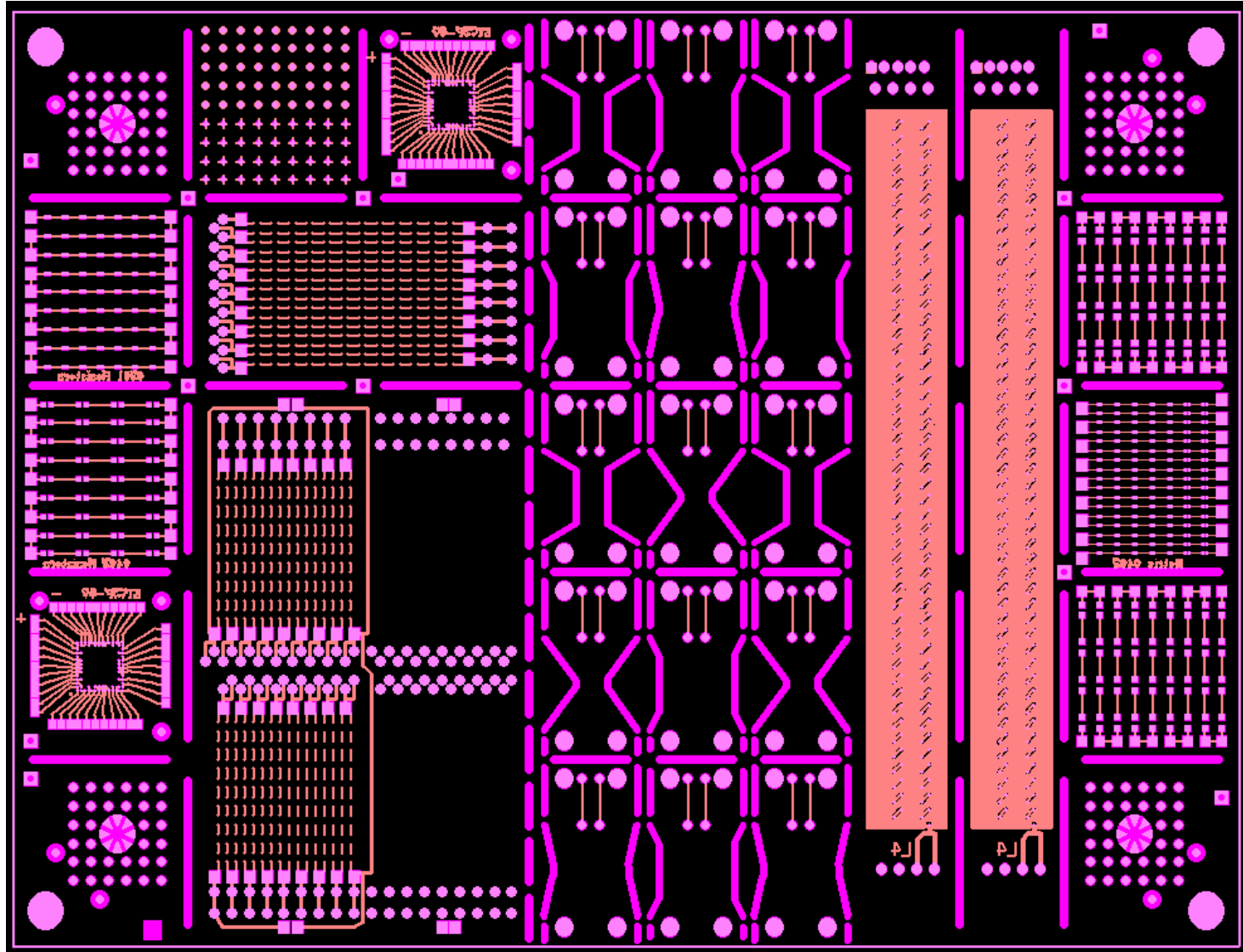
M0402 – 0.4 mm x 0.2 mm
(0.016" x 0.008")

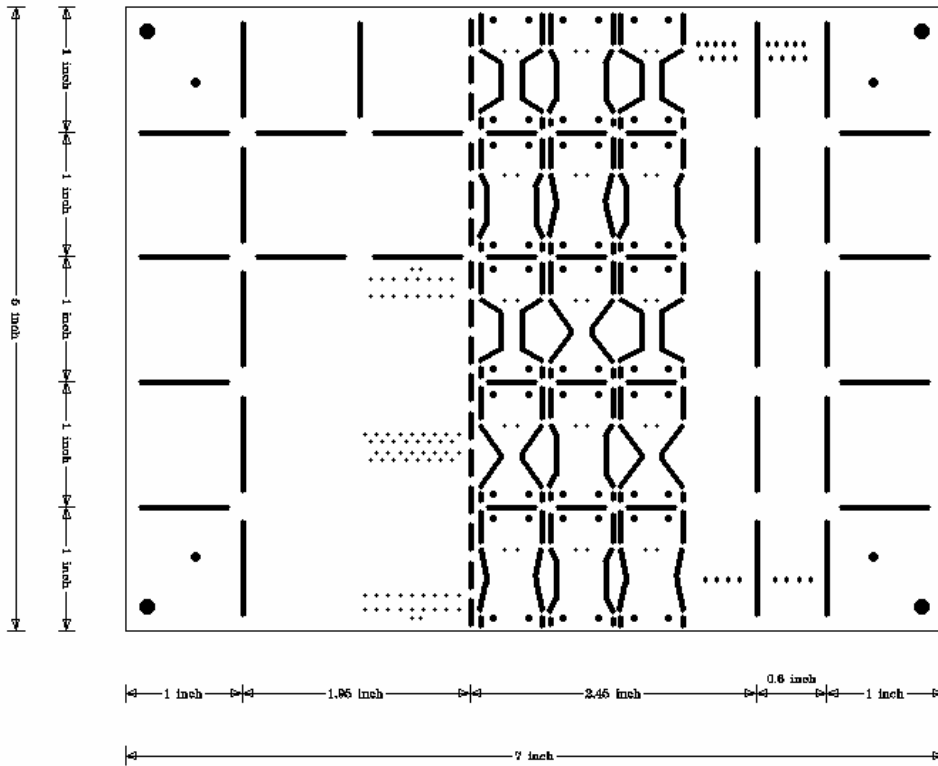


Top Side of PCB



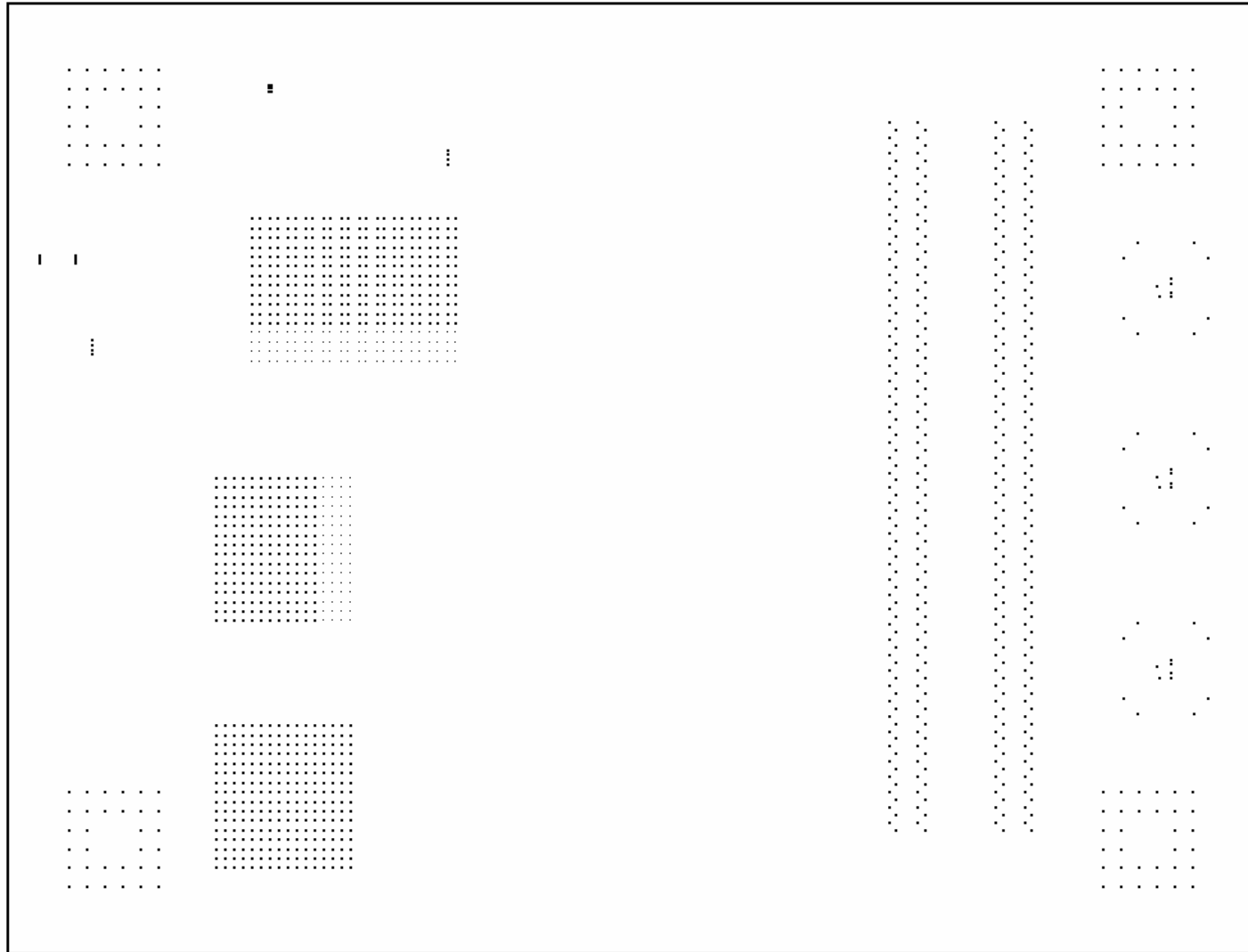
Test Board – Back side



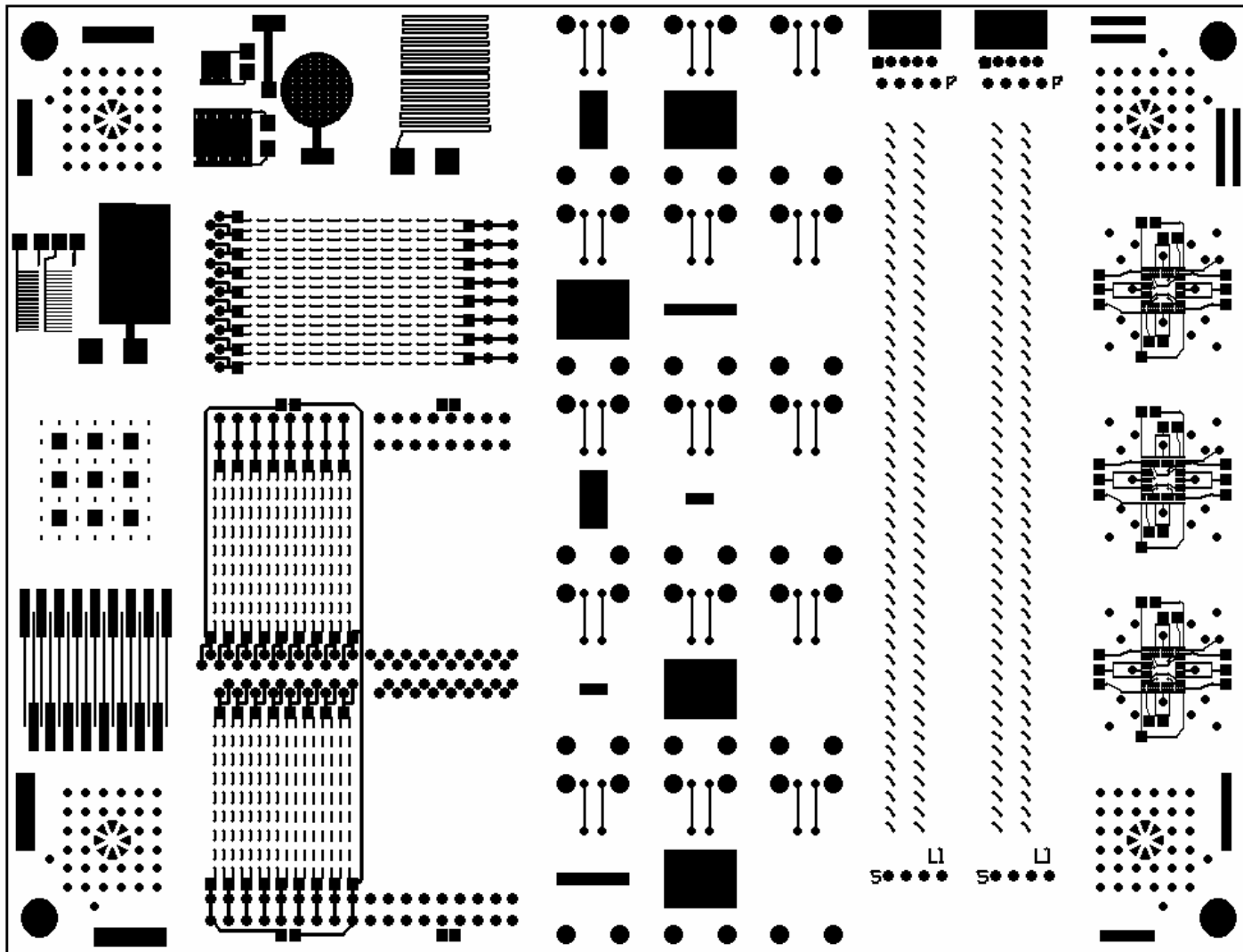


Drill & Routing Notes			
Drills	Size	Count	Feature
D92	0.125"	4	Plated Through Hole
D87	0.089"	4	Plated Through Hole
D116	0.048"	28	Plated Through Hole
D80	0.020"	101	Plated Through Hole
D13	0.8" x 0.031"	12	Routed Slot
D15	0.031" x 0.8"	16	Routed Slot
D129	0.46" x 0.031"	12	Routed Slot
D152	0.031" x 0.25"	16	Routed Slot
D131	0.031" Cutter		Routed Pattern
D25	0.082"	60	Plated Through Hole

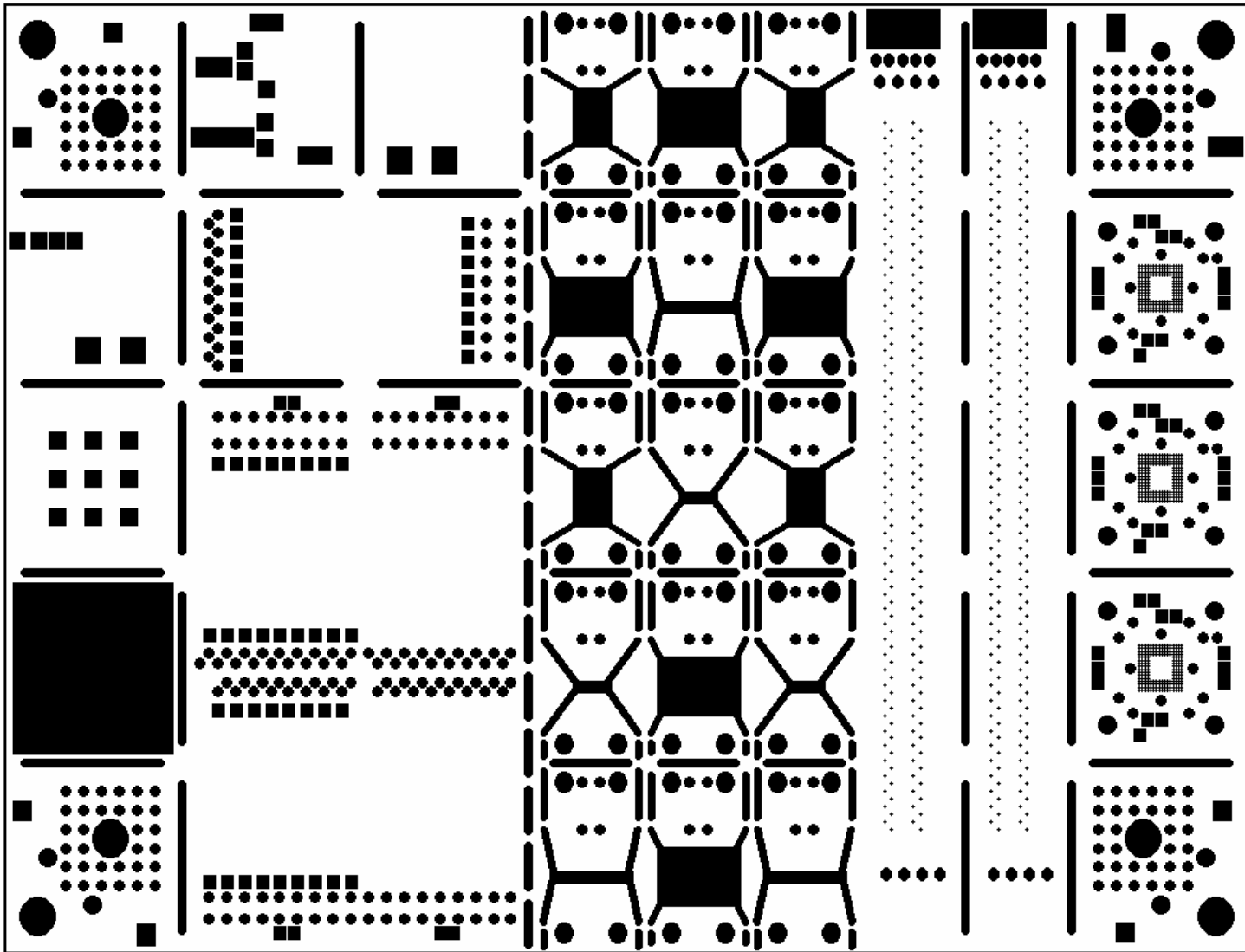
Drill & Route



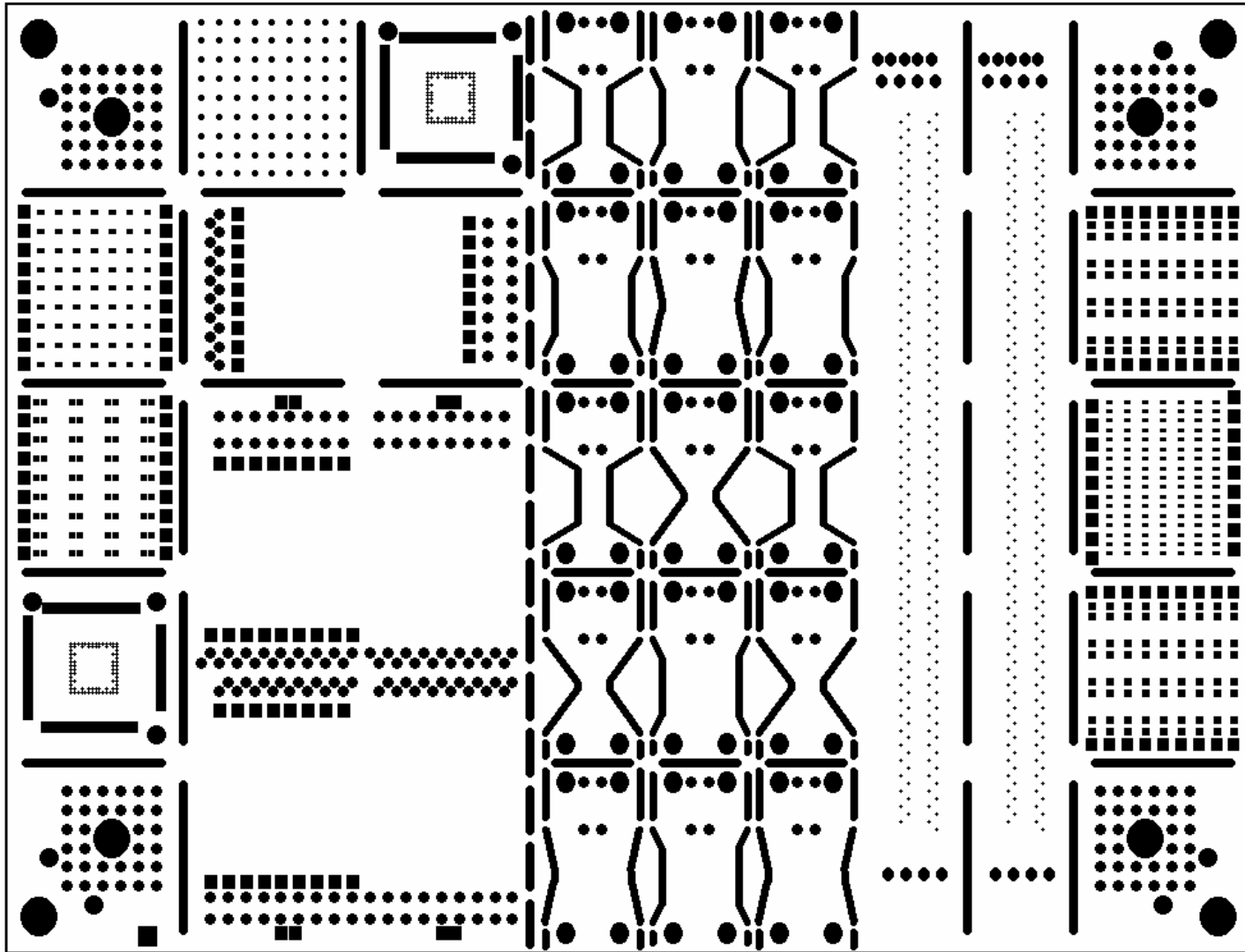
Layer 2 – Blind Via 1-2 (Connects top layer with inner layer 1)



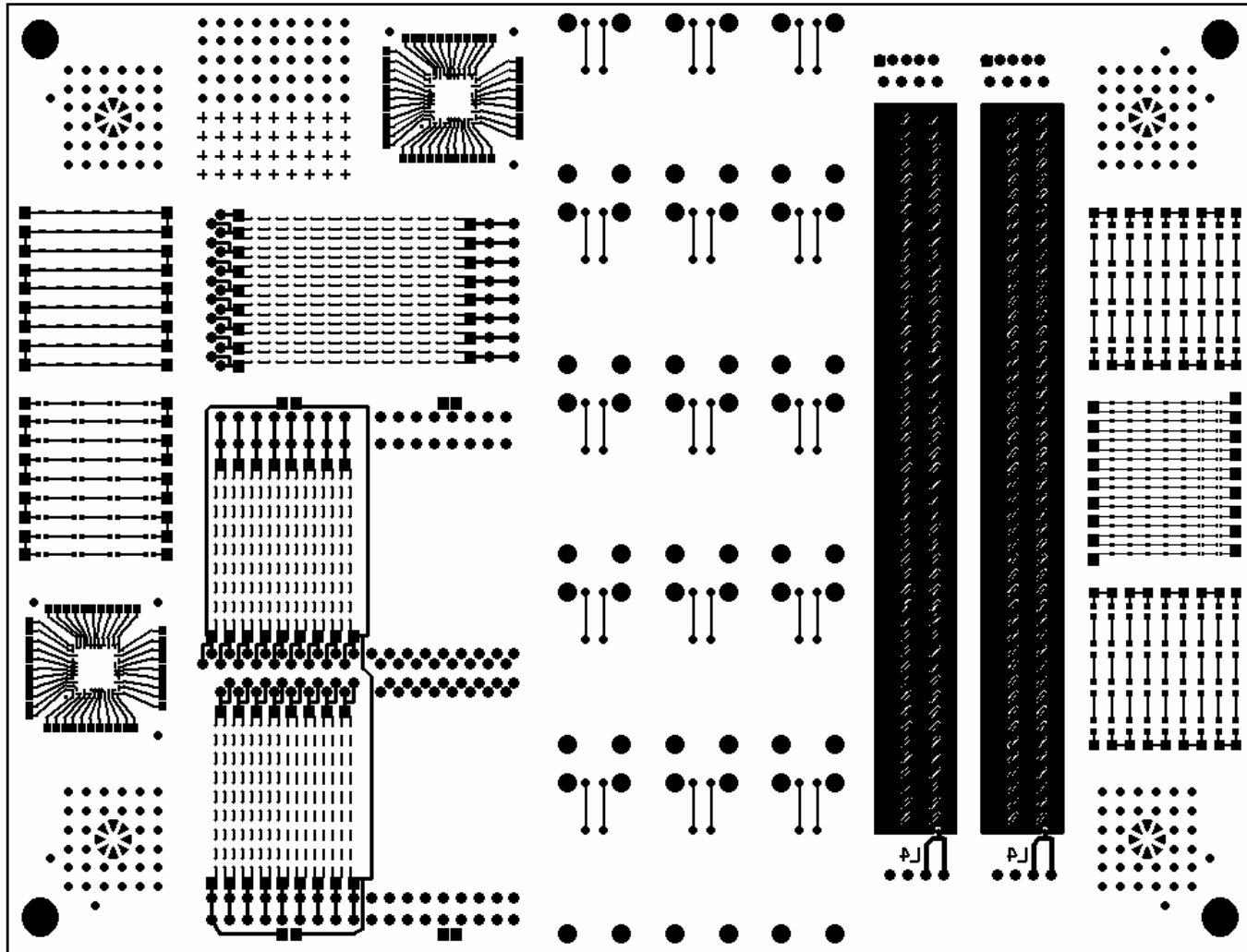
Layer 3 – Top Side Circuitry



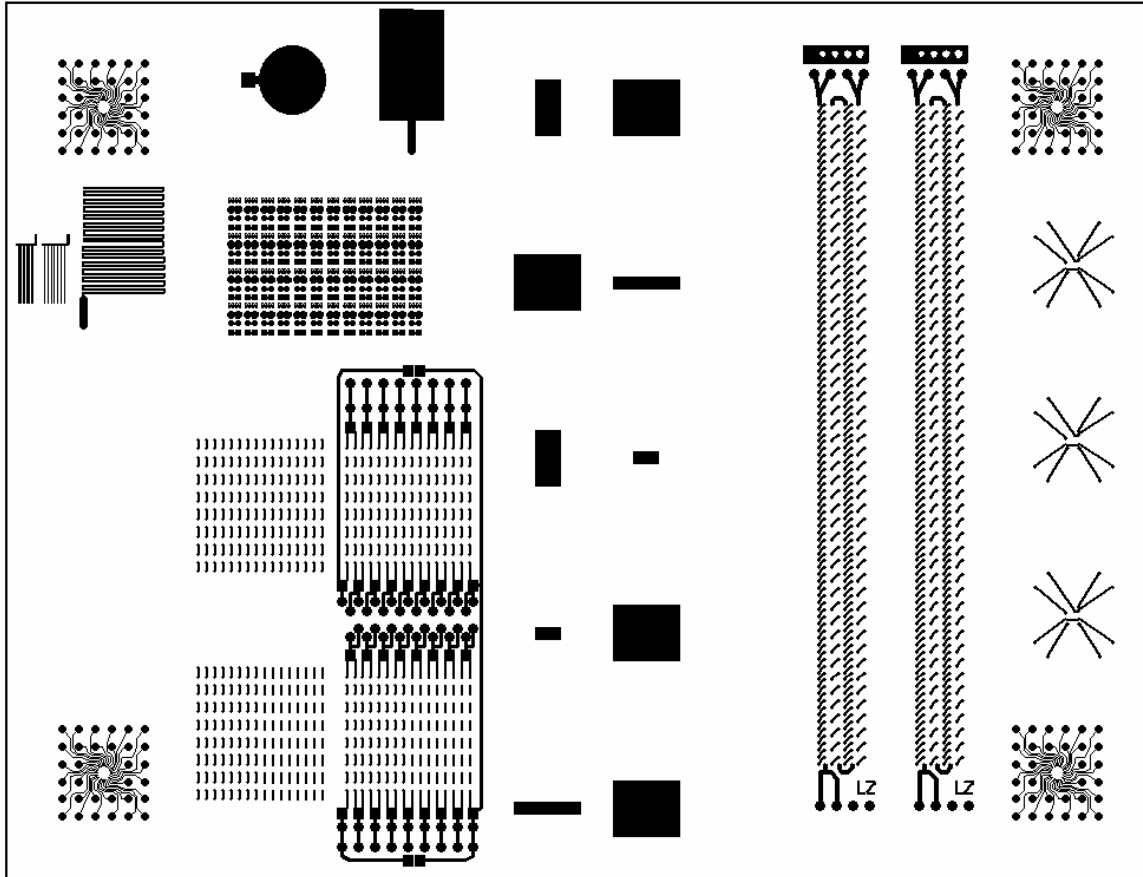
Layer 5 – Top Side Solder Mask



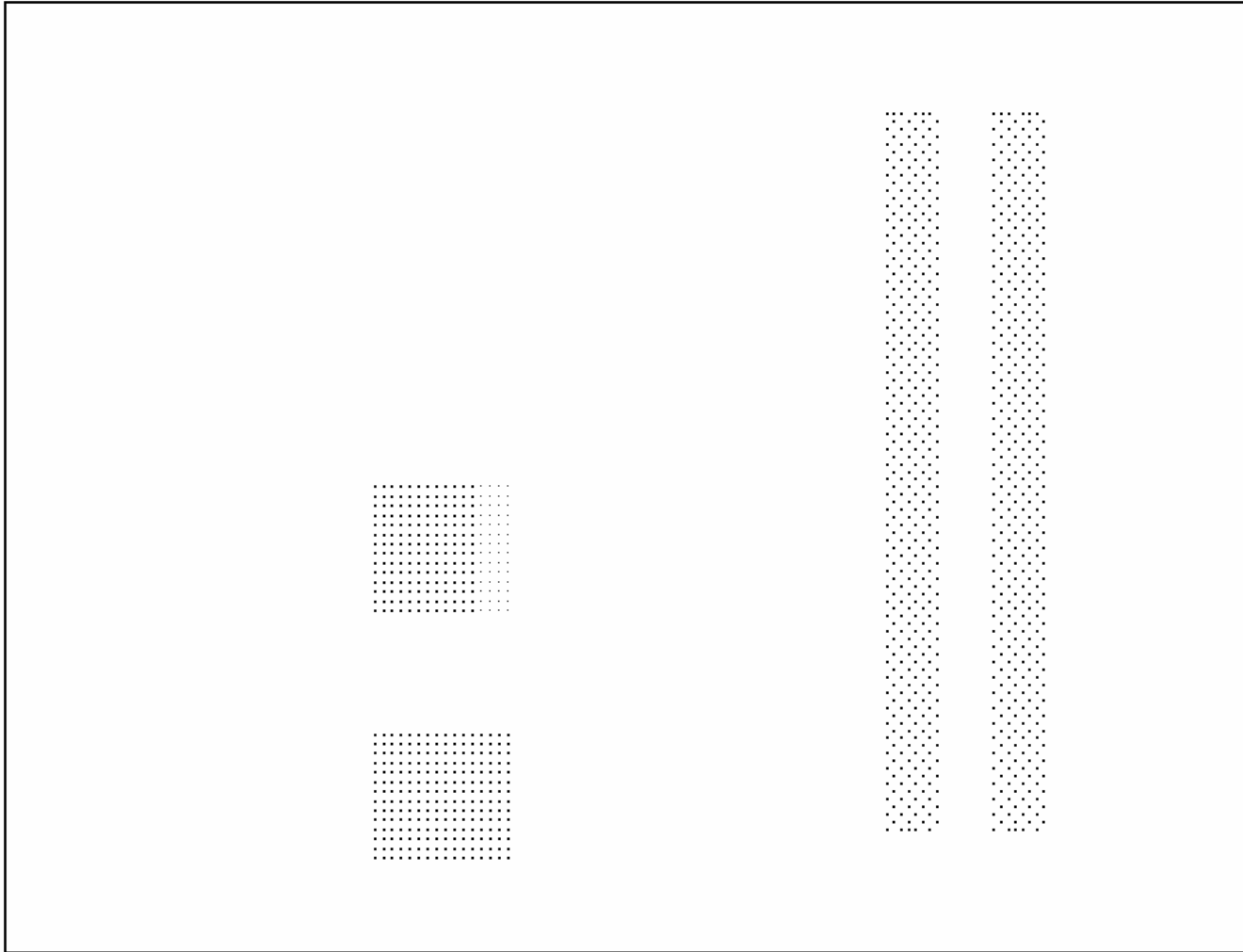
Layer 6 – Bottom Side Solder Mask



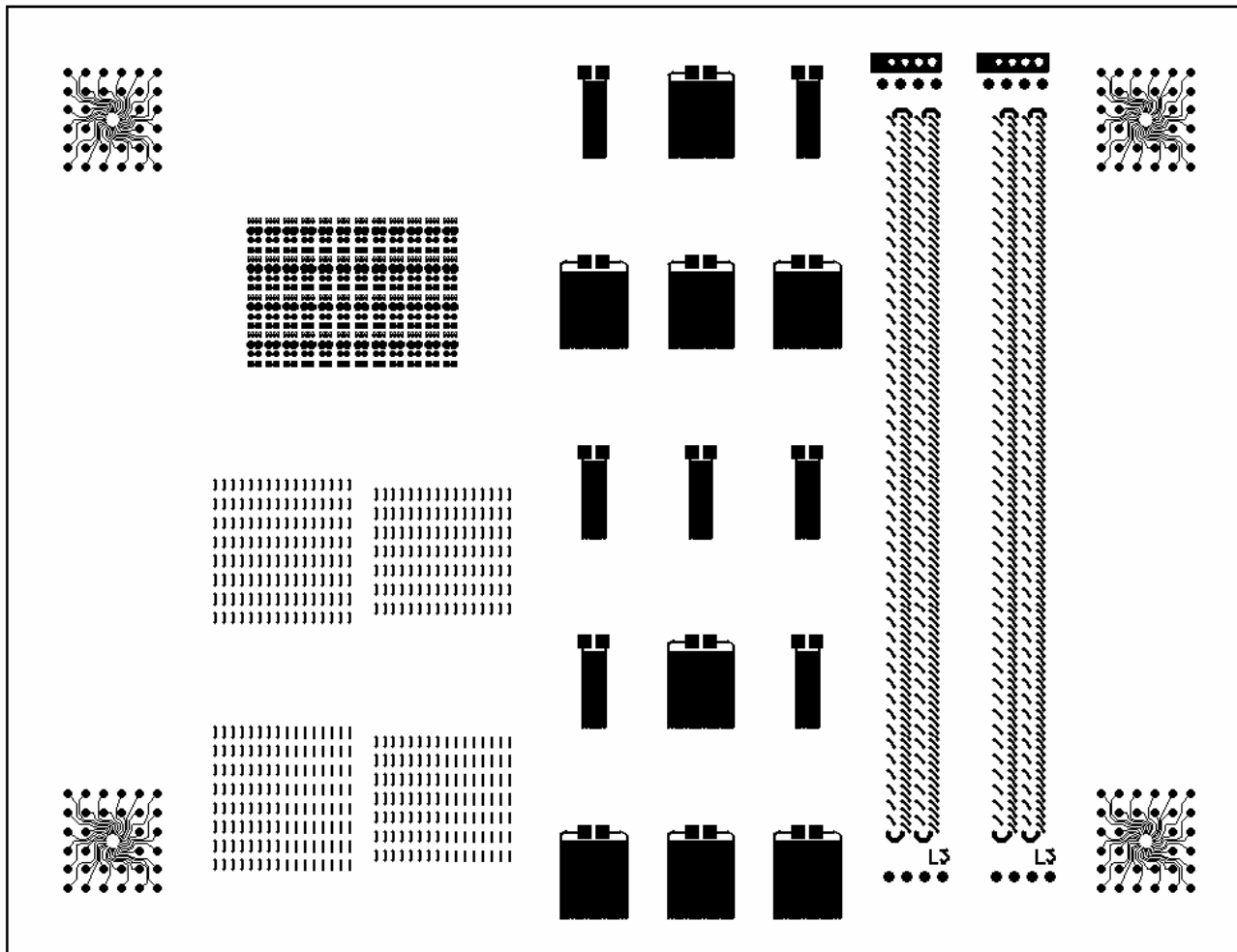
Layer 8 – Bottom Side Circuitry



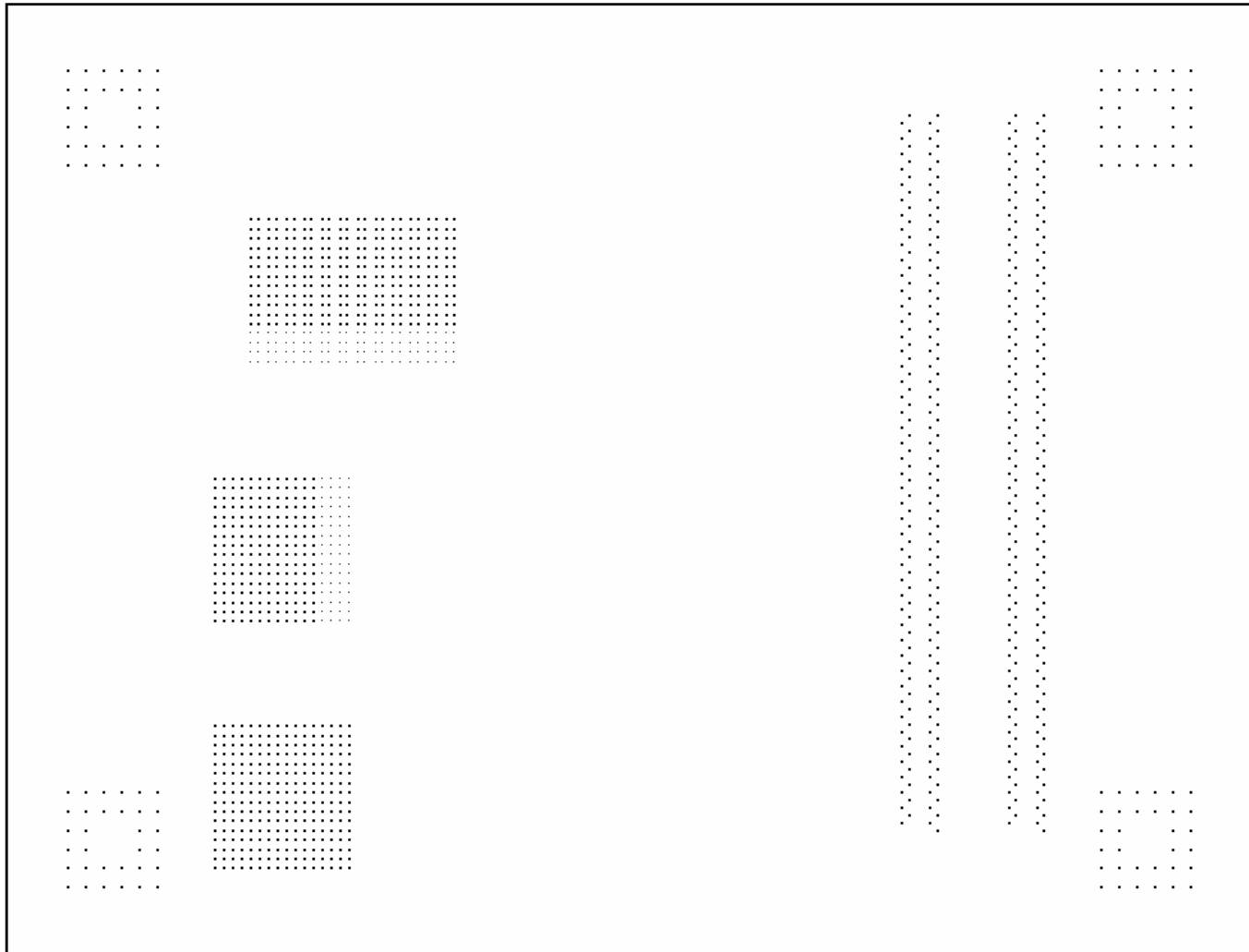
Layer 9 – Inner Layer 1 (Board copper layer 2) Circuitry



Layer 10 – Buried Vias – Connects inner layer 1+2



Layer 11 – Inner Layer 2 (Board copper layer 3) Circuitry



Layer 12 – Blind Vias (Connects Inner Layer 2 and Bottom Layer)