



International Electronics Manufacturing Initiative

# Lead-Free Rework Optimization Project

*Chair: Jasbir Bath, Solectron*

- **Reliability tests in the previous NEMI lead-free assembly and rework project (presented at APEX 2006) indicate a need to construct a Rework Optimization Project.**
- **Thermal fatigue life of certain components on the NEMI Payette board such as the CBGA937, uBGA256, CSP81 was reduced after rework.**
- **This project would evaluate and recommend best practices, rework equipment requirements, impact of adjacent component temperatures and procedures for best-of-breed lead-free rework processing.**

## **Rework optimization project** **(4 areas of work)**

- 1) Rework tolerances and repeatability (Rework equipment manufacturers)**
- 2) Optimized heat transfer into reworked boards and work to reduce adjacent (Top and Bottom) component temperatures: use of heat shrouds, more uniform board heating, heat shields**
- 3) BGA Socket and FCBGA component rework**
- 4) Lead-free mini-pot wave connector rework**

**Overall project chair: Jasbir Bath, Solectron**

**1) Rework tolerances and repeatability**

**Chair: Jasbir Bath, Solectron**

**2) Optimized heat transfer into reworked boards and work to reduce adjacent component temperatures**

**Chair: George Forrest/ Joe Devaney, Alcatel**

**3) BGA Socket and FCBGA package rework**

**Chair: Alan Donaldson, Intel**

**4) Lead-free mini-pot connector rework**

**Chair: Denis Jean, Plexus**

**Co-Chair: Jenny Porter, Solectron**

**5) Rework Reliability Testing/ Failure Analysis**

**Chair: Dave Love, SUN**

## 1) Rework machine repeatability and tolerance

**Stage 1: Rework manufacturer to use ECD rework rider with defined lead-free profile settings on a specific machine**

**Stage 2: Same test at rework manufacturer with same machine model but with different rework machine**

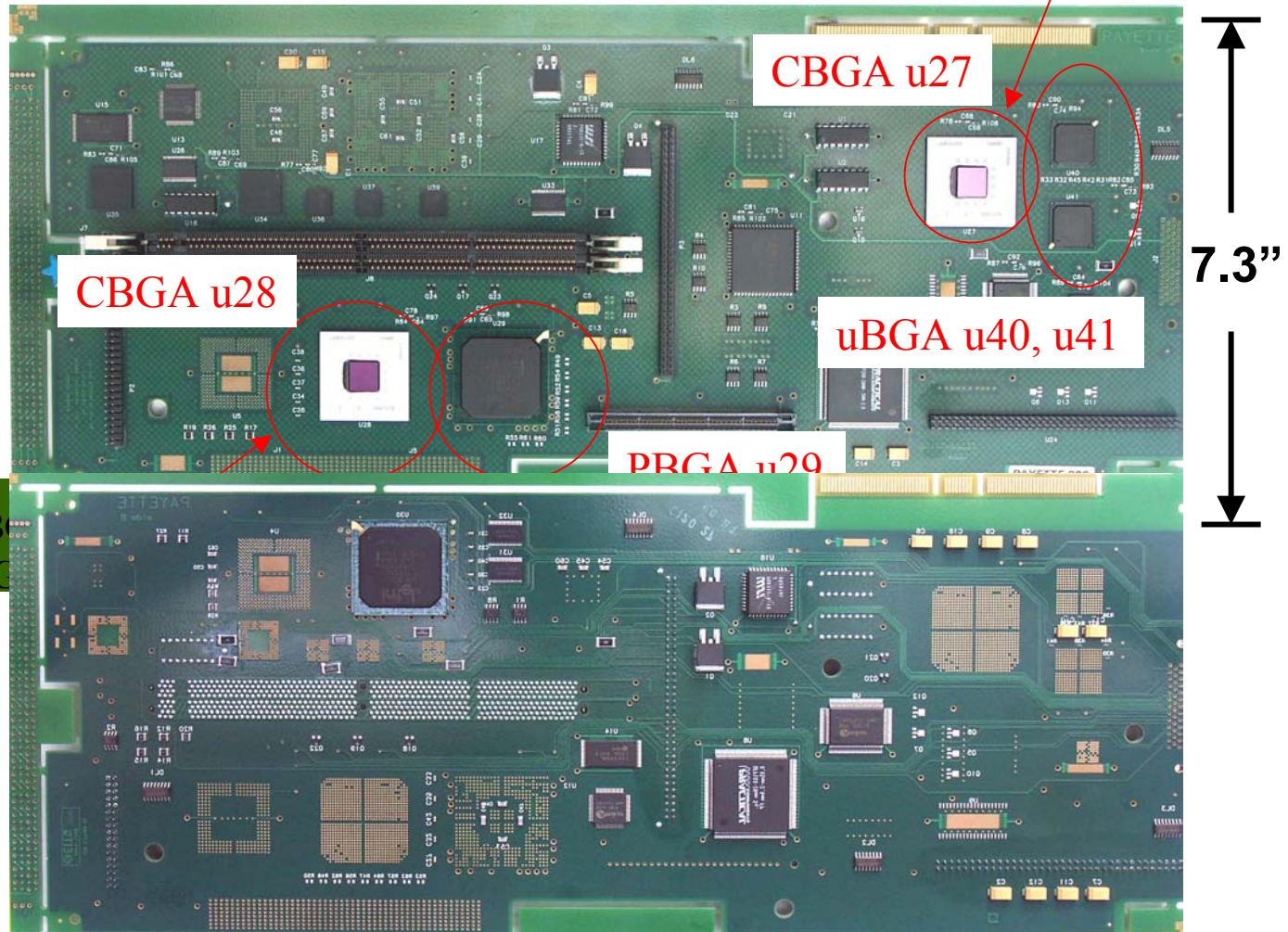
**Stage 3: Same test conducted at OEM/ EMS site with rework equipment at site.**

**Compare data from each three stages to determine and improve rework machine repeatability and tolerances**

## CBGA and uBGA Rework

Open CBGA solder joint after micro-BGA rework

Side A (top)  
14 Cu layers,  
0.093" and  
0.135" thick,  
Electrolytic NiAu  
and Imm Ag



Good CBGA after PBC

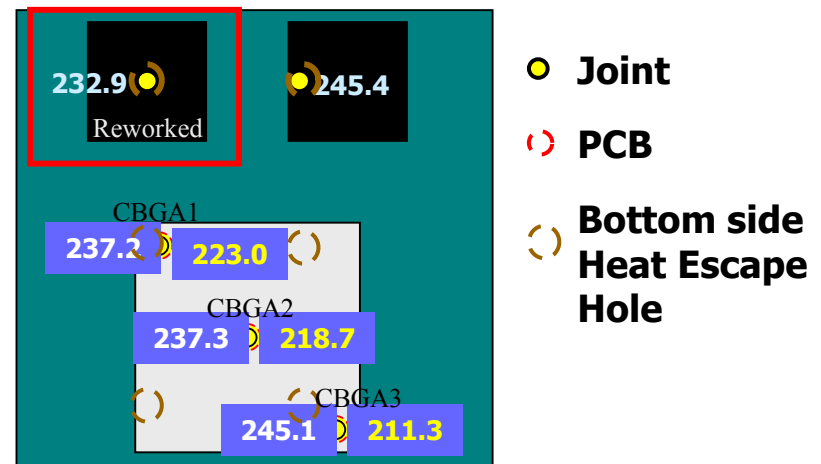
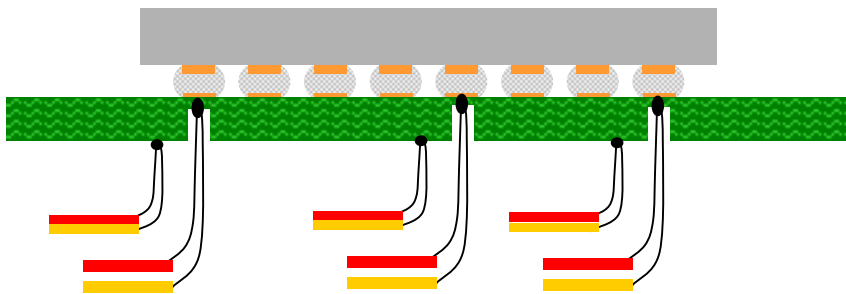
Side B (bottom)  
(SMT + Wave)

- **Observations:**
  - Adjacent CBGA had liquidus temperatures (0.65" away)
  - Thermal gradient across the CBGA package (see table)

**Joint and Package Temp Monitored Values**

TC Location	Peak Temp (C)
Reworked uBGA Joint	232.9
Adjacent uBGA Joint	245.5
CBGA 1 Joint	223.0
CBGA 1 Bottom PCB	237.2
CBGA 2 Joint	218.7
CBGA 2 Bottom PCB	237.3
CBGA 3 Joint	211.3
CBGA 3 Bottom PCB	245.1

CBGA solder joints above and below liquidous temperature



## **2) Optimized heat transfer into reworked boards and work to reduce adjacent component temperatures**

**CBGA/ uBGA: heat shrouds, more uniform board heating, heat shields (ceramic and other materials)**

**Other developments/tools to consider: Thermal modeling software to replicate issue :conduction versus convection heat into boards**

**Use Thermal Imaging Equipment to measure heat distribution of bottom heaters which affects heat into board**

**Reliability(ATC): Confirm reliability of CBGA after rework of uBGA**

**Limited work done for lead-free BGA socket and FCBGA rework.**

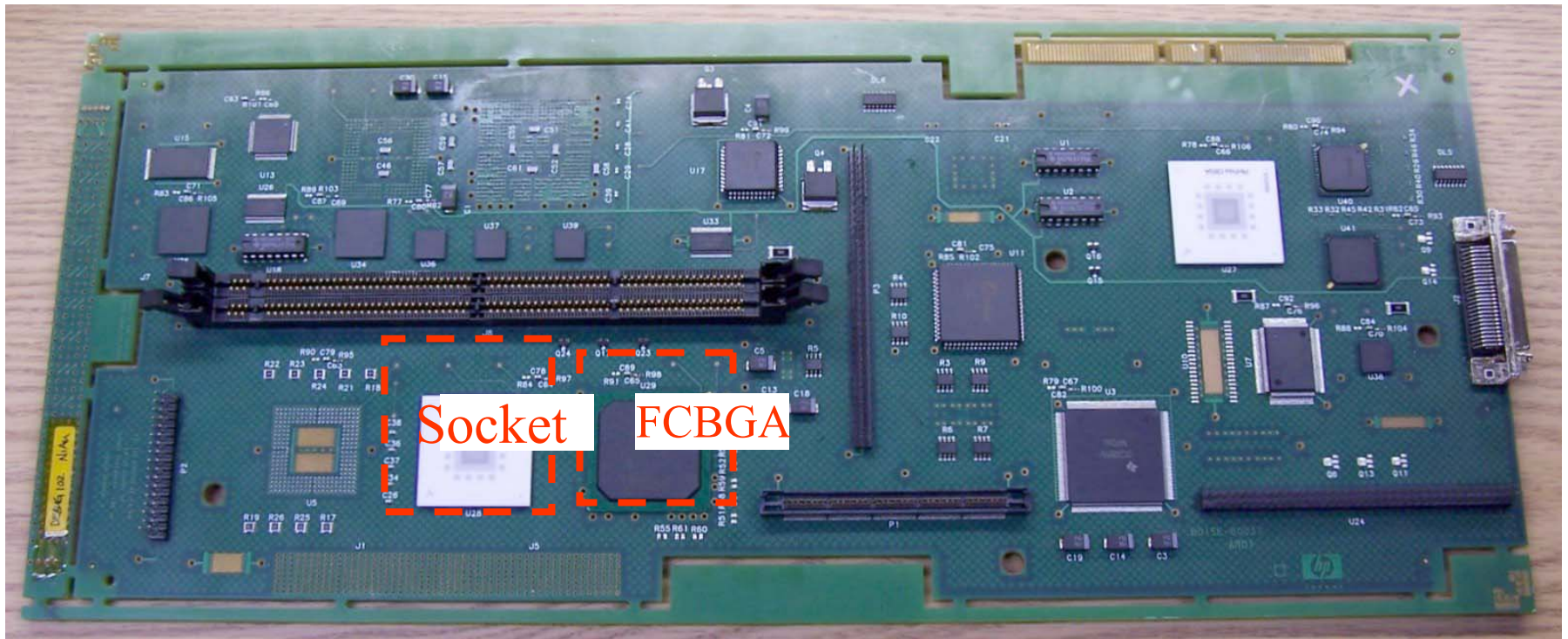
**Excessive Temperature and warpage issues are 2 main concerns**

**3a) BGA Socket rework**

**BGA Socket Connector mPGA 604 I/O, 1.27mm pitch, 45 x 50mm**

**3b) FCBGA 1680 I/O, 45mmX 45mm sq, 1mm pitch: Same component as used on NEMI surface finish project board**

**NEMI Payette Board Redesign required for both components**



- BGA Socket location — remove CBGA & some caps/resistors
- FCBGA location — remove BGA & some caps/resistors

### 3) BGA Socket and FCBGA Rework Timelines/ Milestones

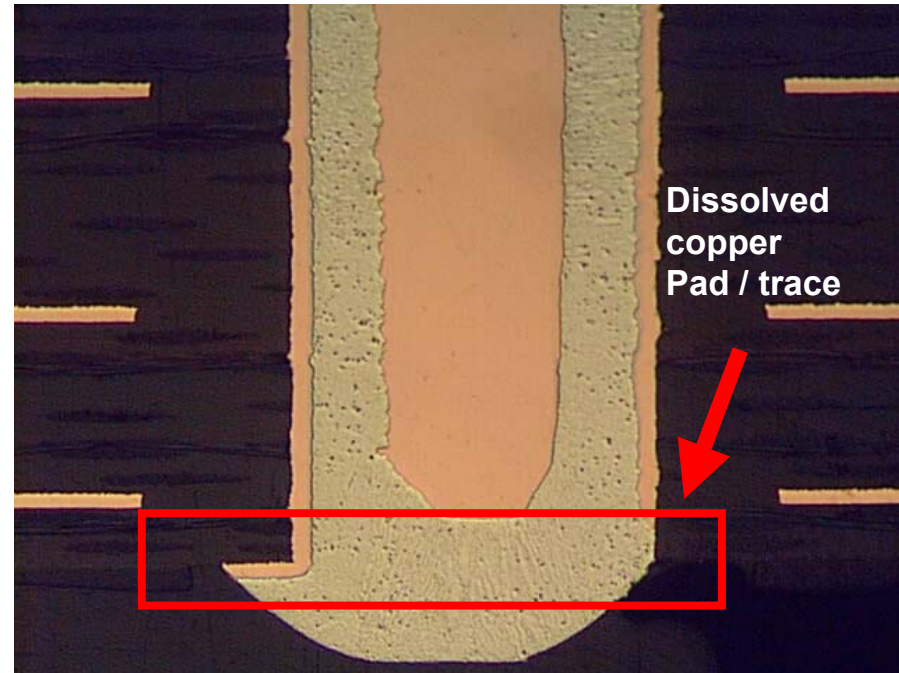
- **BGA Socket and FCBGA Rework: IBM, Intel (Development work)**
- **Chair: Alan Donaldson (Intel)**
  
- **Timeline: October 2005 to January 2007**

#### **NEMI Payette board**

- **Board redesign (add FCBGA and BGA socket) :**
- **Board assembly:**
- **Initial development:**
- **Experimental and optimization:**
- **Rework:**
- **ATC testing:**

## Mini-Pot Results Showing PCB Copper Dissolution of Reworked PDIP16 Solder Joint (SnAgCu, NiAu board, 135 mil thick) on NEMI Payette board

- **Challenge**
  - Simulate current production process
  - Remove and replace a PDIP without board preheat
- **Rework Observations**
  - Achieving sufficient hole fill resulted in the copper pad/trace dissolution on the bottom-side



**Cross-section View of Solder Joint (274°C)**

Total time in mini-pot= 60sec

Enough time to dissolve nickel layer

## **(4) Lead-free mini-pot connector rework development and optimization**

**Previous work covered only DIP16 on NEMI Payette. Extension to other connector components (DIMM, Centronics connector).**

**Also considering different land pattern options (teardrop, solder mask over pad), hole to pin area ratios**

**Mini-pot equipment: AirVac, Wenesco, Spencor Tecnic**

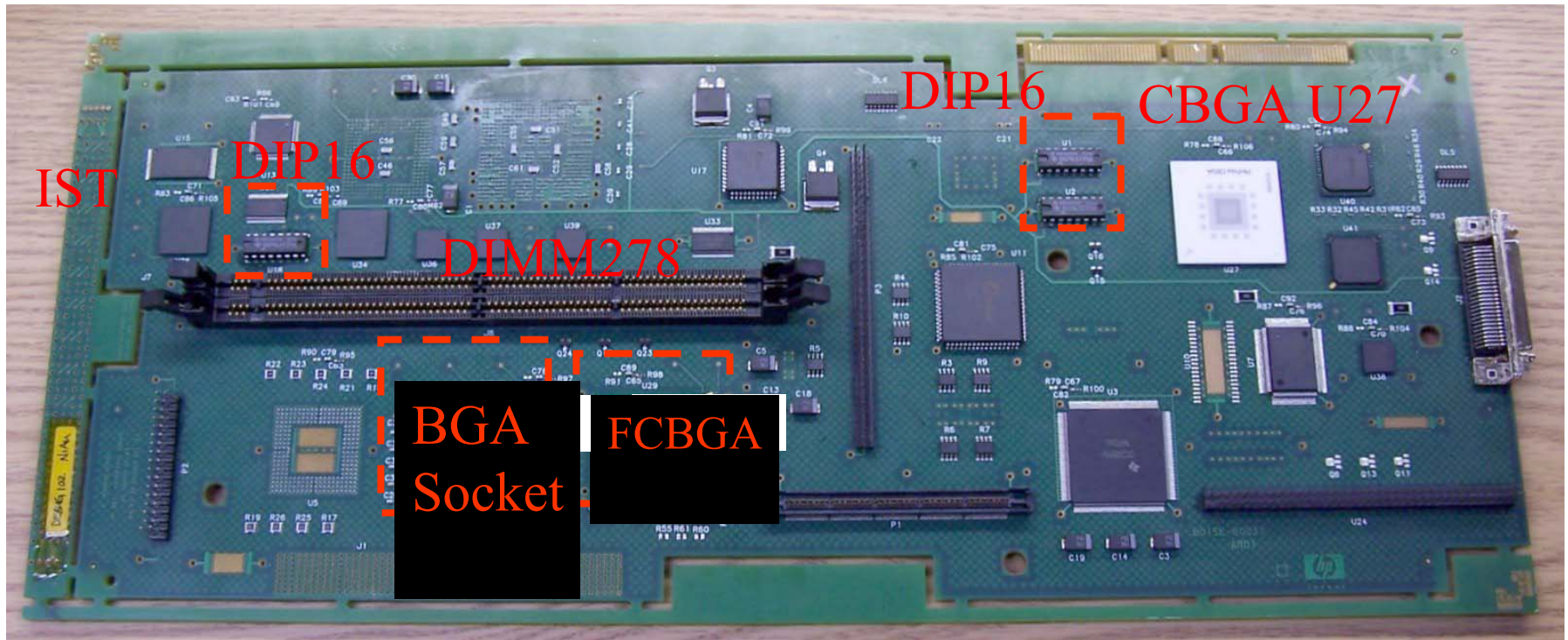
**Collaboration work with NEMI lead-free wave project group using Phase 1 NEMI wave board**

## **4) Mini-pot Rework Timelines and Milestones**

**Original Timeline: Sept 2005 to Jan 2007**

**2 board types: NEMI Wave Phase 1 (Initial development), NEMI Payette redesign**

- Initial development:**
- Experimental and optimization:**
- Assembly:**
- Rework:**
- ATC testing: 6 months**



- Daisy chain DIMM278 connector socket for reliability testing
- Add IST/ CITC coupon on left hand side
- Add CAF coupon

## **5) Reliability Testing/Failure Analysis Timelines and Milestones**

**Failure Analysis (Cross-section/ SEM): (IBM for FCBGA)**

**Time zero, 1<sup>st</sup> fail, End of test**

**Moire:**

**CSAM:**

**ATC (6 months): 0 to 100C**

**Bend testing:**

- Concentrate on lead-free rework on OSP boards of 125mil thickness**
- Only rework FCBGA, uBGA, BGA socket, DIP, DIMM components**
  
- Timeline: Sept 2005 to March 2007**

## **NEMI Rework Optimization Project**

**Goal to deliver by July 2007 lead-free rework solutions for BGA socket, large I/O FCBGA and through-hole connectors, understand / improve rework machine accuracy and repeatability and reduce rework heat into adjacent components and the board.**

**More detailed presentation in Feb. 2007 (IPC APEX)**

## **Members**

- **Solectron, Jabil, Celestica, Sanmina-SCI, Plexus, Foxconn, LACE Technologies**
- **Cisco, Alcatel, SUN, HP**
- **Endicott Interconnect, TI, Tyco, Intel, IBM**
- **Indium, Kester, Senju**
- **O.K. Industries/Metcal, ERSA**

## **Participants in certain parts of project**

- **SRT/VJ Technologies**
- **AirVac**
- **ECD**
- **Wenesco**
- **Spencor Technic**
- **Cookson**